Effect of High Performance SiGe HBT Design Parameters on the Minimum Gate Delay of an ECL Inverter

Chafia Yahiaoui
Laboratoire de Communication dans les Systèmes Informatiques (LCSI)
Ecole Nationale Supérieure d'Informatique (ESI), Algiers, Algeria
Email: c_yahiaoui@esi.dz

***Abstract*—In this paper, we focus on ECL inverter delay analysis through approximate analytical equations. We highlight its dependence on design parameters of SiGe HBT device as well as on electrical parameters. The advantage of this approach is to correlate the physical device parameters to the dominant time constant of this ECL gate. The simulated results show that good performances were derived from well-balanced SiGe HBT characteristics achieved through the fully-self aligned SiGe base structure with a fast forward transit time and low collector capacitance. Strict control at all stages of the technological process in the development of the device, allows the control of all these factors, and it will be possible to optimize the switching performance.**

***Index Terms*—SiGe, high-speed devices, HBTs, ECL inverter, Silicon, Germanium**

I. Introduction

It has been pointed out by Kroemer [1] that heterojunction bipolar transistor (HBT) promises great speed performance for integrated circuits. The main HBT advantages for digital applications can be summarized as follows:

- The removal of the injection holes in the collector in the saturated logic.
- Collector and emitter interchangeability, involving the improvement of ECL circuits delay.
- Better control of offset voltage which is an important parameter in digital and mixed signal applications [2].

II. Electrical Parameters

A. Offset Voltage VCEoff

The offset voltage is the lower limit of collector-emitter voltage saturation which is partly due to the difference between junction surfaces and also due to the dissimilarity in electrical characteristics between emitter-base and collector-base. This discrepancy increases collector-emitter voltage saturation $V_{CE\ (sat),}$ which in turn increases the static power consumption ($V_{CE(sat)}$. I_C).

Manuscript received October 14, 2012; revised February 26, 2013.

It has been investigated [3]-[5] that a careful design of base-emitter junction can eliminate high offset voltage in HBT which is due to an insufficient Germanium (Ge) concentration at base-collector junction and also due to device processing. It has been demonstrated that the offset voltage observed in strained SiGe layer devices can be caused by preferential accumulation of defects at the base-collector junction (closest to the substrate). This phenomenon happens when thickness base exceeds its critical value. The offset voltage varies considerably with the thickness of SiGe base layer as shown in Fig. 1.

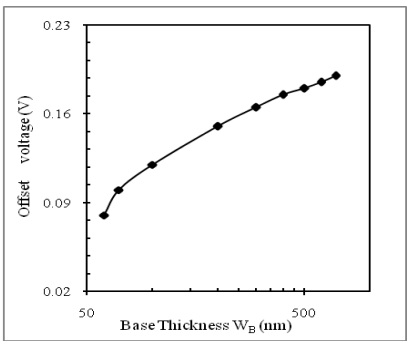

Figure 1. Offset voltage V_{CEoff} verus base thickness W_B

An analytical expression of the offset voltage is given in equation (1) [5].

$$V_{CEoff} = \frac{kT}{q}\ln\frac{A_C}{A_E} + \frac{kT}{q}\ln\frac{1}{\beta} + \Delta E_C + R_E I_B \qquad (1)$$

ΔE_C : Conduction band gap energy

A_E (A_C) Emitter (Collector) intrinsic region area

R_E Emitter resistance

I_B Base Current

β Current gain

B. Propagation Time τpd.

In order to analyze ECL gate delay, we consider the propagation time τpd which is a figure of merit that we envisage to optimize. This parameter depends on frequency performance (cutoff frequency f_T) through ideal transit time τ_F (in forward-active operation).

doi: 10.12720/ijeee.1.1.23-25

In this work, we have developed analytical expressions defined from SiGe HBT device for the six circuit constant time which restrict switching performance: R_{BX} C_{CX}, R_L C_{CX}, R_{Bi} C_{JE}, R_{Bi} C_{CX}, R_{Bi} C_D and R_{Bi} C_{BC}.

Where:

C_{CX}: collector extrinsic capacitance,
R_{BX}: extrinsic base resistance,
R_L: load resistance,
R_{Bi}: intrinsic base resistance,
C_{JE}: emitter junction capacitance,
C_D: diffusion capacitance,
C_{BC}: Collector-base capacitance.

Consequently, optimizing ECL gate delay requires the reduction of these terms. In our study, we use the global expression [6] given in equation (2), where a weighted sum of various terms has been introduced in order to take into account all parameters which affect the propagation time τpd.

$$\tau_{pd} = \sum K_i R_i C_i + K_j \tau_F \qquad (2)$$

ECL gate delay is also affected by the logic swing V_L [7].

III. Circuit Design

The block diagram of the ECL gate inverter is shown in Fig. 2**.** It consists of a differential pair loaded by an emitter-follower pair to reduce the loading effect of the following stage which speeds up the regeneration process, and increases the output voltage swing.

In ECL technology, the operating current through a load resistance defines the maximum speed of the cell. The large load resistance (R_1, R_2 and R_3) will increase the recovery time, whereas a small will limit the output swing and degrade the performance.

The SiGe HBT technology used is from self-aligned double-mesa process [8], in order to reduce the capacitance C_{CX}. An additional advantage associated with this technology is the reduction of R_{BX}. We have used the methodology exposed previously and we have implemented it in ELDO circuit simulator. This tool offers a set of data structure and subroutines, while all the standard features of the C-language are available

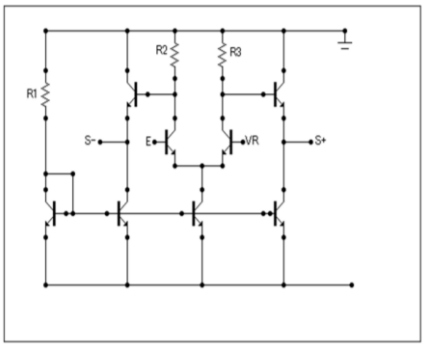

Figure 2. Block diagram of ECL gate

Typical electrical characteristics, geometry and doping parameters are summarized in Table I and Table II.

TABLE I. Summary of the SiGe HBT Parameters

Emitter finger width Emitter finger lengths	0.2 µm 20.0 µm
Extrinsic base finger width Extrinsic base finger length	0.2 µm 20.0 µm
Base-collector intrinsic region area Base-collector extrinsic region area	20.0 µm² 80.0 µm²

TABLE II. Typical SiGe HBT Characteristics

Description	Parameters	Values
Ge concentration	% Ge	35
Base sheet resistance	Rsi (Ω/□)	600
Base thickness	W_B (nm)	40
Collector thickness	W_C (nm)	100
Emitter doping	N_{dE} (cm^{-3})	$3.0\ 10^{18}$
Collector doping	N_{dC} (cm^{-3})	$3.0\ 10^{17}$
Base doping	N_{aB} (cm^{-3})	$4.0\ 10^{19}$
Maximum gain	β_{max}	550
Cutoff frequency	f_T (GHz)	73
Maximum frequency	f_{max} (GHz)	55

IV. Results and Discussion

A. Influence of the base thickness and doping concentration

SiGe ECL gate delay depends strongly on the base thickness and doping concentration (see Fig. 3).

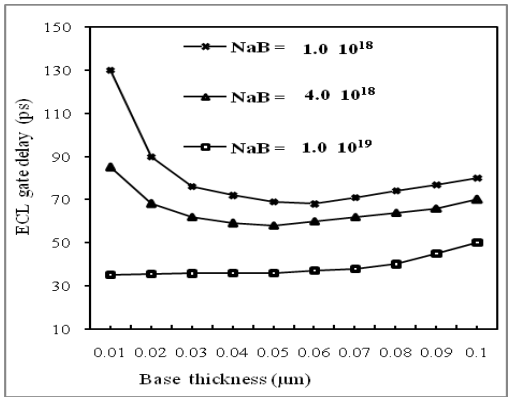

Figure 3. ECL delay versus base thickness for different values of base doping concentration N_{aB}

The emitter doping profil and base thickness have been optimized for a minimum delay. The Ge concentration equal to 35 %, ensures sufficient gain (see Table II).

A minimum ECL gate delay-time of 35 ps was reached. The optimization of the gate delay is obtained for a specific value of base doping concentration, which is a compromise between high base resistance with low base thickness and high transit time with large base thickness.

B. Influence of voltage swing V_L

This parameter is firstly set at the value equal to 800 mV. The ECL delay falls when the collector current I_C increases beyond 1 mA (see Fig. 4), due to the low load resistance required for this value of V_L.

This delay reached a minimum of 34.5 ps at I_C=5mA, when load resistance decreases but this, induced an increase in diffusion capacitance.

For V_L equal to 400 mV, the delay reached 18 ps, but this minimum occurs at a low value of collector current (I_C=4mA). Indeed for this logic swing, the load resistance is half that required for V_L equal to 800 mV.

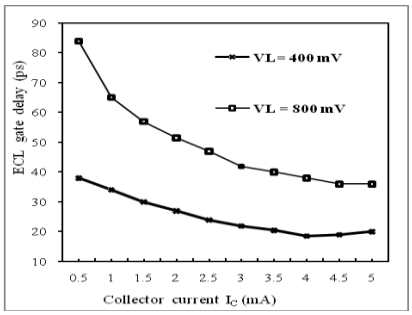

Figure 4. ECL gate delay versus collector current for two values of logic swing V_L

C. Reducing Device Dimensions

In this section, we based the analysis on geometry and technological parameters, according to the collector current. We firstly reduced emitter finger below 1µm, with V_L = 400 mV. We observed, a significant improvement in the gate delay when the emitter finger is reduced from 1 to 0.5 µm, it consequently decreases the delay time from 16 ps to 13 ps at I_C = 5 mA (see Fig. 5). When this parameter is equal to 0.2 µm, a small decrease (<1 ps) is raised at high levels of collector current, however a significantly degradation is observed at low values.

This behavior can be explained by considering the dominant circuit constant time (R_L C_{CX}).

When the emitter area A_E is reduced, the collector current is also reduced, consequently a greater load resistance is required to generate the given logic swing.

The load resistances may be reduced by increasing collector-current with emitter finger, which does not imply that ECL gate delay can be improved indefinitely by reducing them. Indeed, it is undesirable for ECL gate to operate at high currents levels due to high injection effects that degrade the forward transit time.

However as the extrinsic base R_{BX} is kept constant, the capacitance C_{CX} is not reduced in the same proportions.

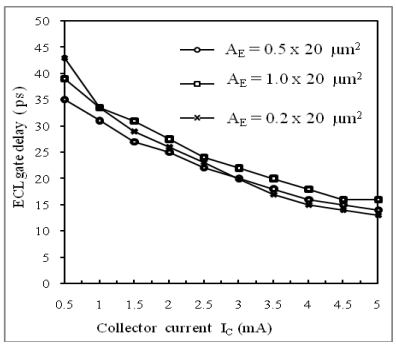

Figure 5. ECL delay versus collector current for different values of emitter area A_E and with a logic swing V_L=400 mV

For Ic=5mA, the constant time (R_L C_{CX}) became less significant, it implies an improvement of ECL gate delay for emitter finger equal to 0.2 µm, consequently, a minimum gate delay equal to 12.5 ps is obtained.

V. Conclusion

This analysis showed that a simple SiGe ECL inverter delay is affected by the choices made in design topology, voltage swing, and load resistance in addition to the influence of the transistor. A correlation between SiGe ECL inverter delay to a simple figure of merit based on base resistance, collector capacitance and forward transit time is done and a good compromise gives a minimum gate delay equal to 12.5 ps.

References

[1] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," in *Proc. of IEEE*, vol. 70, no. 1, pp. 13-25, Jan 1982.

[2] H, J. Jeon, Y. B. Kim, and M. Choi, "Offset voltage analysis of dynamic latched comparator," in (MWSCAS), pp. 1-4, April 2011.

[3] J. He, S. Y. Zhan, D. G. Chen, and R. L Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," *IEEE Trans on Circuits and Systems*, vol. 56, pp. 911-919, 2009.

[4] J. R. Hayes, F. Capasso, R. J. Malik, A. C. Gossard, and W. Wiegmann, "Elimination of the emitter/collector offset voltage in heterojunction bipolar transistors," *Electron Devices Meeting*, 1983, vol. 29, pp. 686-688.

[5] B. Mazhari and H. Morkoc, "Effect of collector‐base valence‐band discontinuity on Kirk effect in double‐heterojunction bipolar transistors," in *Applied Physics Letters*, 1991, vol. 59, pp. 2162-2164.

[6] E. F. Chor, A. Brunnschweiler, and P. Ashburn, "A propagation-delay expression and its application to the optimization of polysilicon emitter ECL processes," *IEEE Journal of Solid State Circuits*, vol. 23, no. 1, pp. 251-259, 1988.

[7] J. B. Kuo, T. S. Yang, R. W. Dutton, and B. A. Wooley, "Two-dimensional transient analysis of a collector-up ECL inverter," *IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8 , no. 10, pp. 1038–1045, 1989.

[8] A. Gruhle, H. Kibbel, and E. Kasper, "53 GHz-fmax Si/SiGe heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 11, 1992.

Chafia Yahiaoui received the Engineering degree in electronics and telecommunication from Polytechnic National school, Algiers, Algeria in 1984, and the Ph.D. degree from the University of Paris XI, Paris, France, in 1995. Her doctoral research concerned compact modeling of SiGe HBT and device design and simulation. In 1999, she joined the high school (ESIEA) in Paris, France where she was involved in the design of SiGe HBT high-speed integrated circuits. Her research interests are also in the field of RF circuits. Since 2006, she returned to Algeria where she joined the Department of communications and computer Engineering, of the Ecole Superieure d'Informatique (ESI) in Algiers, where she is currently a teacher and lecturer. Her research interests are in the field of telephony and voice over IP, SIP Protocol and 4G mobile: WiMAX, LTE and LTE-advanced standard