A Power and Area Efficient 8-Channel Neural Signal Front End for Biomedical Applications

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***Abstract*—We present a novel architecture of an ultralow-power and low-area neural signal front-end architecture for telemetry powered Brain Machine Interface (BMI) implanted microchip. Power and chip area are considered two of the most critical parameters in designing neural front ends. The proposed architecture shows better performance as compared to existing designs. The architecture consists of a preamplifier as a gain stage, analog multiplexer for serialization of analog signals and a gain-programmable and band-tunable filter. The filter yielded a midband gain of 40dB ranging from 200Hz to 6KHz; its input referred noise was calculated as 5.2μVrms and a power consumption of 6.2μW. The circuit level design is implemented in 0.5μm CMOS technology with 2.8V supply. The paper discusses architectural and circuit level design and presents a comparison of this work with state of the art architectures.**

***Index Terms*—biomedical, telemetry, neural, filter, implant, LFP, spikes.**

I. Introduction

Neural data recording has attracted interest of neuroscience community for the past several years. The recorded neural data not only helps monitor and diagnose brain related disorders but also provides promising solutions for treating ailments such as Parkinson's disease, epilepsy and seizures. It also enables us to build efficient prosthetic devices for amputated persons [1].

Conventionally neural data is recorded using implanted microelectrode arrays which are connected to external module for amplification and recording of data thru wires and connectors. The wires coming out of patients body present a whole host of problems: i) transcutaneous connecting wires provide a path for infection ii) while the data is being recorded the patient can't move iii) neural signals are extremely weak and external noise and other interferences can easily corrupt these signals. To cater for all the aforementioned problems the trend is to use wirelessly powered implantable modules for brain machine interface (BMI) systems. Fig 1 shows an overall diagram of such a BMI system.

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One of the most critical parts of BMI systems is the neural signal amplifier which has to be low-noise and low-power. Neural Amplifier is supposed to take input from microelectrodes, purify and amplify the neural signal and finally sends it to Analog to Digital Convertor (ADC) for digitization and further processing as shown in Fig 3 .Local Field Potentials (LFPs) and spikes are commonly re corded neural signals. LFPs result from synchronous firing of many neurons near the electrodes and are 1mV to 50mV in amplitude, ranging from 100 mHz to over 100Hz. Ionic or charge imbalances on the surface of the neuron cell membrane generate an electrochemical signal from membrane towards the extracellular space, called a spike. Spikes are 5uV to 100uV in amplitude and range from 250Hz upto 5 KHz.

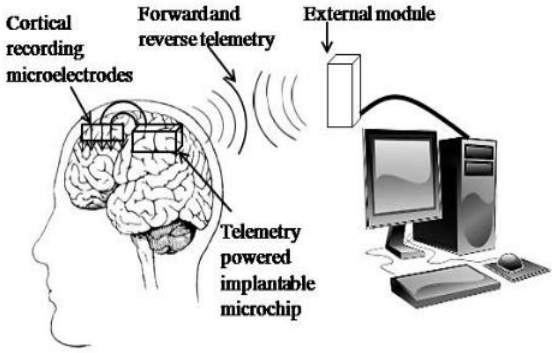

Figure 1. Brain machine interface system

Next generation telemetry powered implanted neural recording systems must be ultralow-power with low input referred noise, both of which have inverse relation and this tradeoff is expressed as Noise Efficiency Factor (NEF). Harrison's [2] landmark architecture can record multiple biomedical signals, but is extremely power hungry. Many neural amplifier designs [3-5] consume a lot of power (>100uW) in order to achieve low input referred noise. This can cause serious power problems when we are dealing with electrodes of order of 100 or 1000. Designs [6, 7] which can achieve better power performance are inefficient in terms of area and noise. The tradeoffs between these critical parameters are evident from Fig 2.

We propose a novel architecture of neural amplifier which is efficient in terms of area and power. This novel design, therefore, is best suited for systems with large

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number of electrodes. While existing designs report separate power-hungry and under-performing neural amplifiers for each electrode, we suggest to use power and area efficient preamplifiers with each electrode, multiplex the data from preamplifiers and use one super performing gain programmable and band tuneable high pass filter to record both spikes and LPFs. The downside of this architecture is the stringent requirement placed on settling time of the super-performing amplifier (which in above designs was only faced by MUX) or the speed of each component in general. However, by properly designing the amplifier architecture for the required settling time, we can save a considerable amount of power.

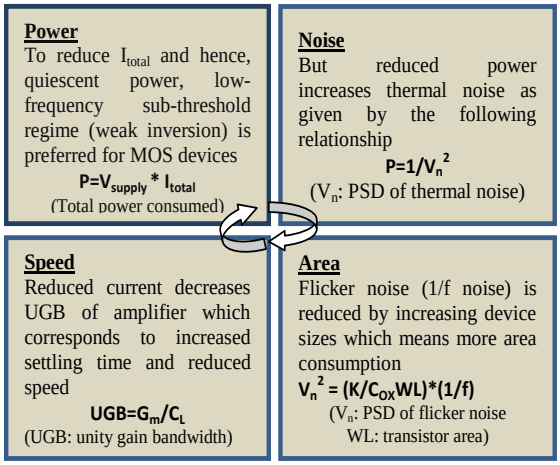

Figure 2. Neural amplifier design trade-offs

II. System Architecture

The proposed wirelessly powered BMI system consists of an implant module, an external controller and a wireless interface. The block level diagram of overall neural front end system for the implanted module is shown in Fig. 3.

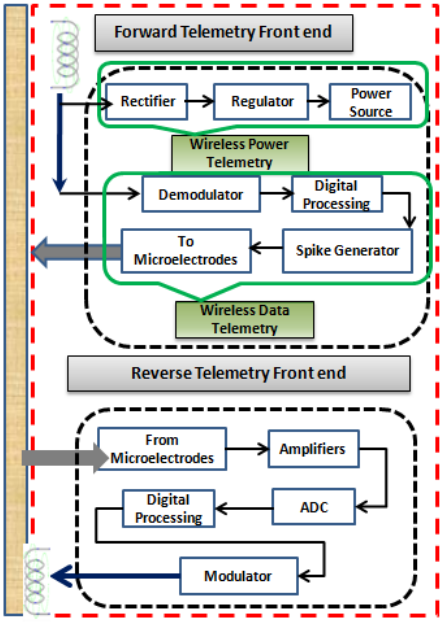

Figure 3. System architecture of implanted chip

Data transmission from external module to implant is called forward telemetry and from implant to external module is called the reverse telemetry. Comparison of complete BMI architectures with wireless power and data telemetry is detailed in Table I

TABLE I. Comparison of Work of Leading Research Groups in Telemetry Powered Neural Recording and Stimulation Systems

	Number of Channels	Carrier frequency, modulation scheme, and data rates for FDT	Carrier frequency, modulation scheme and data rates for RDT	Amplifier Gain, low/high cutoff frequencies	Size	Power dissipation	IC Technology employed
[8]	64/64	FSK 8MHz/4MHz 2Mbps	OOK 70MHz to 200MHz 2Mbps	60dB, 100Hz to 9.1KHz	1.4cm by 1.55cm	14.4Mw @1.8V	AMI06
[9]	100/100	ASK 2.64MHz	FSK 433MHz	60dB, 300Hz,5KHz	NA	13.5mW @ 3V	0.5µm 3M2P CMOS
[10]	16/16	13.56MHz	NA	43dB,100Hz, 7.5KHz		12 mW	AMIS 0.5-micron
[11]	128/128	NA	NA	40dB,104Hz,10K	8.5mm^2	10mW	0.35um CMOS
[12]	4/4	50MHz to 1GHz, PWM FSK	50MHz to 1GHz, PWM FSK	NA	NA	NA	0.5um for implant
[13]	NA	OOK 15Kbps to 300Kbps	25MHz 1Mbps to 5.8Mbps	NA	1.5mm by 1.5mm(each transceiver)	100uW in implant, 2.5mW in external module	AMI 0.5um CMOS
[14]	128/128	UWB Transmission (employing OOK and PPM)	UWB Transmission (employing OOK and PPM)	40dB 0.1 to 200Hz 2KHz to 20KHz	8.8mm by 7.2mm	6Mw @ 3.3V	0.35um 4M2P CMOS
[15]	7/7	NA	FM 94-98 MHz	43.7dB Few to KHz	2.1cm * 2.1cm * 0.16cm	2.05mW @ 3V	1.5µm 2P2M

III. Neural Amplifier Architecture

The proposed neural recording amplifier architecture, as seen in Fig 4, is highly power efficient as it uses only one filter-amplifier stage for all the channels instead of using a separate gain and filter stage for each channel. Currently front end architectures employ separate under-performing amplifiers and filters for each electrode and multiplex their data before ADC [8], [9], [11], while there are some in which an entire ADC is allocated to each channel [14]. Although, these architectures are quite fast and thus help achieving high transmission rates, they

have to pay the price in terms of area and power consumption. The preamplifiers in the proposed design are high input impedance common source amplifier to pick the noise corrupted signal once the DC offset has been removed. The architecture is based on the concept that seven out of eight electrodes measure spikes while only one will measure the LFP. The data is measured sequentially .i.e. at a particular instant of time only one electrode will be allowed to pick data. The data obtained from the electrodes is multiplexed and sent to a band pass filter with variable gain and bandwidth control. The system adjusts its bandwidth and gain to measure spikes/LFPs as instructed accordingly thru the control signals.

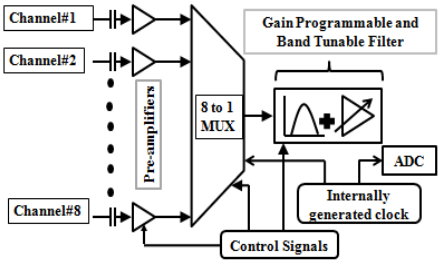

Figure 4. Block level diagram of proposed neural front end architecture

IV. Circuit Level Implementation

Ideally a neural amplifier should provide high gain over a limited BW. It should be capable of eliminating the DC offset from the electrodes, which can be as large as 1V. High gain and the least possible power consumption are required. High gain means an increased settling accuracy, and it also decreases the gain error. Nominal closed loop gain should be around 40 to 50dB while the open loop gain must be around 80dB. Generating low pass cut-off frequency in extremely low frequency range (for LFP) demands a high time constant for the circuit of band pass filter and this is achieved by using pseudo-resistors in feedback topology [2].

Fig 5 shows the proposed filter-amplifier architecture. It consists of a gain stage followed by band tuneable filter stage. The capacitive feedback sets the mid-band gain and the low cut-off frequency is adjusted by V_{tune}. Gain and the high-pass cut-off frequency are given in (1) and (2) respectively.

$$A = \frac{C_{in}(total)}{C_{feed}(total)} \tag{1}$$

$$f_H = \frac{1}{2\pi R_{out} C_c} = \frac{G_m}{2\pi A C_c} \tag{2}$$

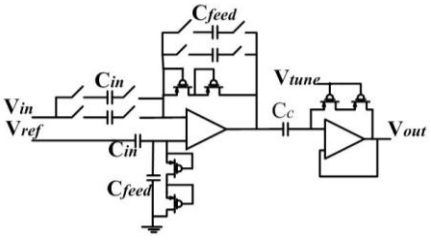

Figure 5. Band-tuneable and gain-programmable filter-amplifier

In our design we have used folded cascode (Operational Transconductance Amplifier) OTA, shown in Fig. 6. The folded cascade OTA is essentially a modified version of the one presented in [6]. Most of the transistors in this OTA are operating in "subthrehold regime" instead of "field effect regime". A MOSFET operating in subthreshold regime acts like a BJT which has much higher transconductance efficiency. At low frequencies where power is a critical, we can operate MOSFETs in subthreshold regime since unlike in field-effect regime there is no direct current flowing between source and drain which effectively helps us to minimize the static power consumption.

Inversion Coefficient (*IC*) is the parameter describing the region of operation of a MOSFET. For subthrehold region of operation of MOS, *IC* must be less than 0.1. *IC* is given as

$$IC = \frac{I_D}{I_S} \tag{3}$$

where I_D is the drain current and I_S is the moderate inversion characteristic current given by (4)

$$I_S = \frac{2\mu C_{ox} U_T^{\,2}}{\kappa} \frac{W}{L} \tag{4}$$

where U_T is the thermal voltage and κ is the subthreshold gate coupling coefficient with a typical value of 0.7. With these values known we can now easily calculate tranconductance [17] in subthreshold regime as given in (5)

$$g_m = \frac{\kappa I_D}{U_T} \frac{2}{1+\sqrt{1+4.IC}} \tag{5}$$

Analog design challenges are explained in [16] which were taken care of while designing this OTA.

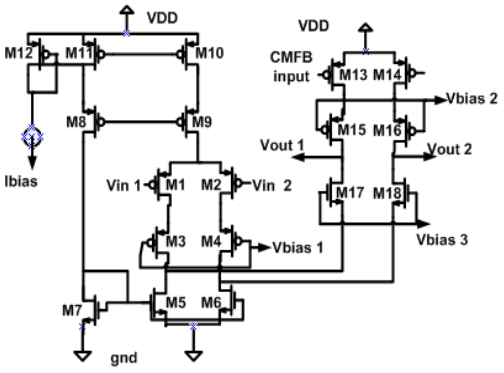

Figure 6. Folded cascade filter-amplifier used in proposed filter-amplifier (Common Mode Feedback Circuit is not shown in the figure)

V. Layout Results and Comparison

A. Noise Performance

The noise-power trade-off in Fig. 2 is mathematically expressed as noise efficiency factor(NEF) shown in (6).It's theoretical limit, when the two input differential

PMOS are the only source of thermal noise and the flicker noise is ignored, is 2.9 as calculated in [17].

$$NEF = V_{in,rms}\sqrt{\frac{2I_{total}}{\pi U_T 4kTBW}} \quad (6)$$

Practically, flicker noise and the input thermal noise can be reduced by increasing the input differential device sizes and its trans-conductance efficiency (g_m/I_D) respectively. Fig. 7 shows a plot of input referred noise with the bias current of our filter amplifier (2.2uA).

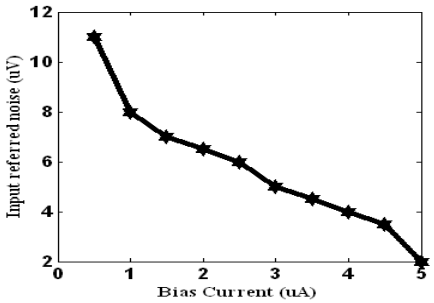

Figure 7. Noise variation of filter amplifier with current

B. Speed

Considering the highest neural signal frequency of 7kHz, we set sampling frequency of 20kHz. Since the outputs of 8 channles have to be multiplexed, this translates to a channel scan time requirement of 6.25us for each channel. This implies that every channle will collect data for 6.25us after every 50us. Layout results show the settling time of our filter amplifier lies well within this specificaitons.

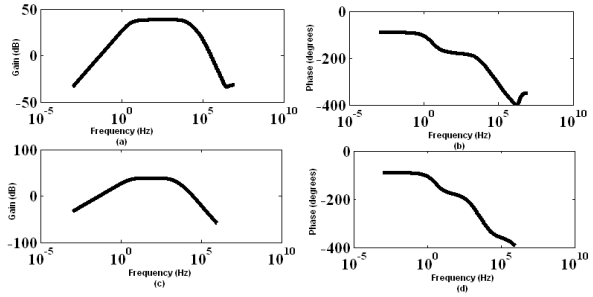

Figure 8. (a) & (b) bandwidth and phase of filter when configured for recording spikes. Fig. 8. (c) & (d) bandwidth and phase of filter when configured for recording LFPs

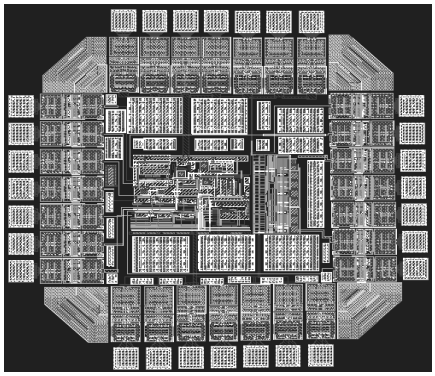

Figure 9. Layout of the whole system

C. Gain and Bandwidth

Fig. 8 shows gain magnitude and phase response of our filter-amplifier configured for both spike (of 50uV amplitude cantered at 1 KHz) and LFP (of 5mV amplitude, centered at 100Hz) recording. The gain of capacitive feedback and bandwidth configuration for filter-amplifier shown in Fig 5 were adjusted accordingly. Fig. 9 shows layout of designed neural amplifier and SAR ADC.

D. Comparison Chart

Table II provides a comparison of critical parameters of neural signal amplifier proposed till date with our proposed design. Current and power consumption figures for other architectures are scaled up for 8 channels as our filter-amplifier is configured to record data for 8 channels, unlike others. Current consumption shown for the proposed work includes current of filter amplifier (2.2µA) and all 8 preamplifiers (8*0.5µA) which equals 6.2uA. This comparison clearly shows our novel architecture has saved considerable amount of power and area. Fig 10 graphically shows the power utilized by our design is quiet less when compared with existing architectures.

TABLE II. COMPARISON OF MEASURED CAHRACTERISTICS WITH STATE OF THE ART NEURAL AMPLIFIER ARCHITECTURE

	Process (µm)	No. of channels	Gain (dB)	Power (µW)*	NEF	BW
[18] 09	0.18	NA	36	90	3.6	up to 10K
[19] 09	0.35	256	34	33.6	4.6	
[3] 10	0.35	128	33	102	5.55	10-5K
[6] 11	0.18	32	49-49	43.2	4.4-5.9	350-11.7K
[4] 11	0.18	NA	39.4	63.36	3.35	up to 7.2K
[5] 12	0.5	NA	62	32	3.3	100-7K
This work	0.5	8	40	17.36	5.2	200-9.6K

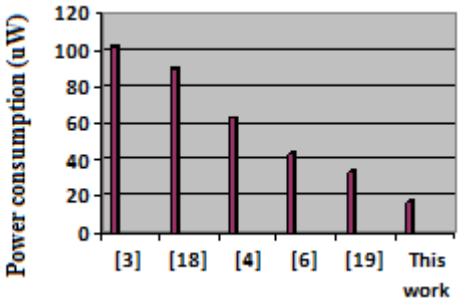

Figure 10. Power consumption comparison

VI. CONCLUSION

Novel neural signal amplifier architecture was presented and implemented in 0.5um technology. The proposed architecture is low noise and sub-threshold regime operation makes it power efficient. The details of neural recording and wireless telemetry were also discussed and a comparison of research work in this field was compiled. Comparison clearly indicates that our

work is power and area efficient and uses a relatively less expensive technology. This neural front end currently deals only with 8 channels and will be improved for up to 32 channels.

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