

Comparison of Total Ionizing Dose Effects for Floating and Tied Body SOI nMOSFETs

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Abstract—The comparison of total ionizing dose (TID) effects for floating body (FB) and tied body (TB) partially depleted (PD) SOI nMOSFETs is presented. The TB device shows enhanced back-gate threshold voltage shift under OFF bias condition. The simulation results indicate that, under OFF bias condition, the electric field lines distributed in the buried oxide (BOX) basically turn up from the drain to the substrate for FB device, while they largely turn up from the drain to the body with higher efficiency of charge trapping for TB device. It is further confirmed by the distinct simulated potential in the body region and strength of the electric field in the BOX.

Index Terms—total ionizing dose, threshold voltage shift, charge trapping, PD SOI nMOSFET

I. INTRODUCTION

Silicon-on-Insulator (SOI) technology provides many advantages over their bulk Si counterparts[1], in particular, better resistance against transient ionizing effects like Single Event Upsets (SEU) or Latch-up in the harsh environment[2]. In the last decade, several foundries, IDT vendors and IP companies have added SOI CMOS to their offerings to reap performance benefits driving costs for SOI CMOS down[3]. However, radiation sensitivity to charge that is trapped in the buried oxide and shallow trench isolation (STI) renders the TID responses of SOI transistors a great concern[4-8].

In this paper, the TID effects for FB and TB PD SOI nMOSFETs have been investigated. The enhanced back-gate threshold voltage shift under OFF bias condition is observed for TB device. By performing device simulation, it is found that the distinct electric field distributed in the BOX is responsible for the larger threshold voltage shift for TB device.

II. DEVICE AND EXPERIMENTAL PROCEDURE

The devices used in this work were fabricated in a 0.13 μm PD SOI CMOS process, using the STI for isolation scheme, on UNIBOND[®] wafers from SOITEC. The top silicon film and buried oxide thickness are 100 nm and 145 nm, respectively. Devices with external body contact (T-shaped) and floating body were used to investigate the TID effects. Core NMOS devices ($W/L=10 \mu\text{m}/0.13 \mu\text{m}$

and $W/L=10 \mu\text{m}/0.5 \mu\text{m}$) and I/O device ($W/L=10 \mu\text{m}/0.5 \mu\text{m}$) were selected as samples in our study.

⁶⁰Co γ -rays were used as the radiation source. During irradiation, ON ($V_G=V_{dd}$, other terminals grounded) and OFF ($V_D=V_{dd}$, other terminals grounded) states were the bias conditions. The dose rate was typically around 100 rad(Si)/s, and all devices were subjected up to 500 krad(Si) for core devices and up to 300 krad(Si) for I/O device.

All current-voltage measurements were carried out using an HP-4156 Parameter Analyzer. Unless the contrary is indicated, the drain bias was kept in the linear operating regime ($V_D=100 \text{ mV}$) for all measurements, and the substrate (V_{BG})/gate bias (V_{FG}) was grounded for front-gate/back-gate current-voltage measurements. Time between two irradiation steps was controlled within half an hour.

III. RESULTS AND DISCUSSIONS

A. Experimental Results

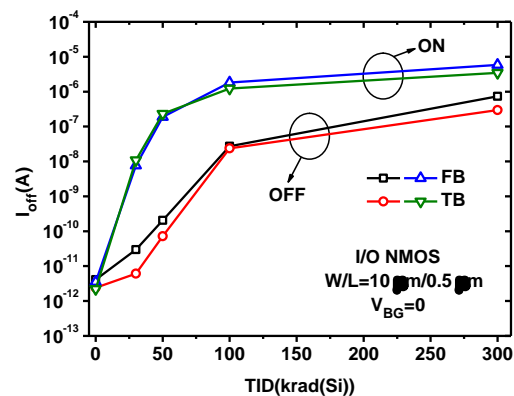


Figure 1. Comparison of the off-state leakage current under ON and OFF bias conditions for I/O FB and TB devices.

Fig.1 shows the comparison of the front-gate off-state leakage current ($I_{ds}@V_{FG}=0$) under ON and OFF bias conditions for I/O FB and TB devices. It can be seen that I_{off} increase with incremental TID for both devices, which is mainly due to turn-on of the parasitic transistor formed by the STI oxide and the body. For either FB device or TB device, the larger I_{off} under the ON bias condition is caused by the more intense electric field across the STI oxide, resulting in more trapped positive charges

compared to the OFF bias condition[9]. Under the same bias condition, the enhanced I_{off} degradation for the FB device is expected to originate from the extra parasitic leakage path by contrast with the TB device.

The back-gate threshold voltage shift (ΔV_{Tb}) under OFF bias condition for core FB and TB devices is illustrated in Fig. 2. It is clear that, for devices with the same dimensions, the FB device exhibits smaller ΔV_{Tb} than the TB device. For devices with $W/L=10 \mu\text{m}/0.13 \mu\text{m}$, at 500 krad(Si), ΔV_{Tb} has reached to -12.7 V for the TB device, while it is only -5.1 V for the FB device. The same trend can be observed for devices with $W/L=10 \mu\text{m}/0.5 \mu\text{m}$.

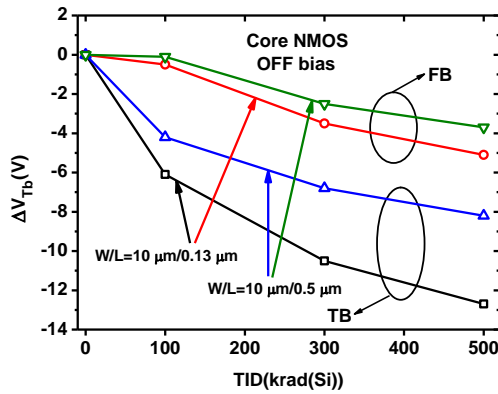


Figure 2. Comparison of the back-gate threshold voltage shift under OFF bias condition for core FB and TB devices.

B. Simulation and Discussions

To better understand the influence of body contact schemes on the radiation responses under the OFF bias condition, 2D and 3D simulations have been performed, using the process and device simulation tool from Silvaco^[10] Technology Computer Aided Design (TCAD). The process parameters were provided by the foundry. Fig.3 illustrates the constructed 3D T-shaped SOI core NMOS, and the locations of the body contact, gate, source, drain and STI are labeled.

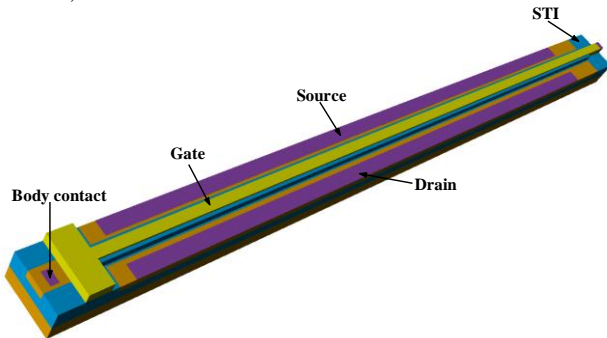


Figure 3. The 3D structure of simulated T-shaped SOI core NMOS.

Fig. 4 and Fig. 5 show the 2D graphical representation of electric field lines distributed in the BOX under OFF bias condition for the TB and FB devices, respectively. In Fig. 4, two components of the electric field lines at the drain terminal can be found, one is turning up from the drain to the body and the other turning up from the drain to the substrate. The part turning up from the drain to the

body will push the radiation-induced positive trapped charge toward to the interface between the body silicon and the BOX. By contrast, in Fig. 5, the electric field lines mostly turn up from the drain to the substrate, which tends to push the positive trapped charge down, therefore, causing smaller back-gate threshold voltage shift as shown in Fig. 2.

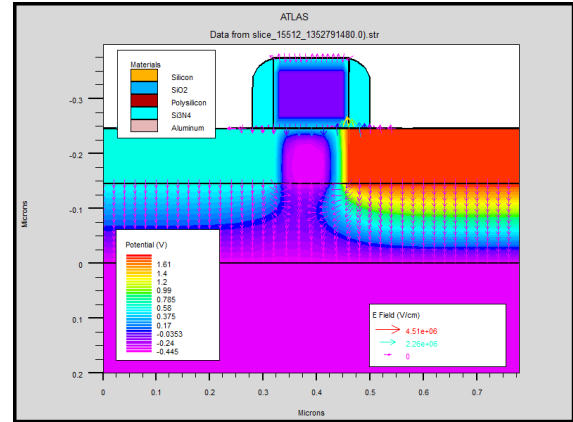


Figure 4. The 2D graphical representation of electric field lines distributed in the BOX under OFF bias condition for the TB device.

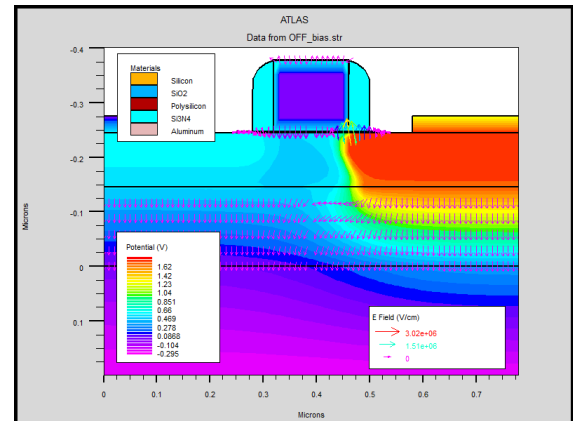


Figure 5. The 2D graphical representation of electric field lines distributed in the BOX under OFF bias condition for the FB device.

To clarify the distinct electric field lines distributed in the BOX, the simulated body potential along the channel length (X direction) at the middle depth of the body region under OFF bias condition for the core FB and TB devices is shown in Fig. 6. The positive body potential in the whole body region can be observed for FB device. The elevated body potential is attributed to the impact ionization induced by the large drain voltage, supplying majority carriers to charge the body. This means the positive potential promotes the electric field lines terminated at the substrate whereas the relative negative body potential of the TB device inclines to terminate the electric field lines at the body terminal.

Fig. 7 also shows the simulated electric field strength (E_y) along the depth (Y direction) at the middle region of the BOX under the same bias condition for both devices. For FB device, the positive E_y in the whole region of the BOX demonstrates the positive trapped charge seems to be pushed down to the bottom region of the BOX layer, attenuating the influence of the charge on the back-gate

threshold voltage shift. Reversely, E_Y is divided into negative (in the upper region) and positive values (in the lower region) by dash line for TB device. The positive E_Y distributed in the whole region of the BOX coincides with that as depicted in Fig. 5 for the FB device. The positive and negative E_Y distributed in the upper and lower region of the BOX contribute to the two components of the electric field mentioned in Fig. 4 for the TB device.

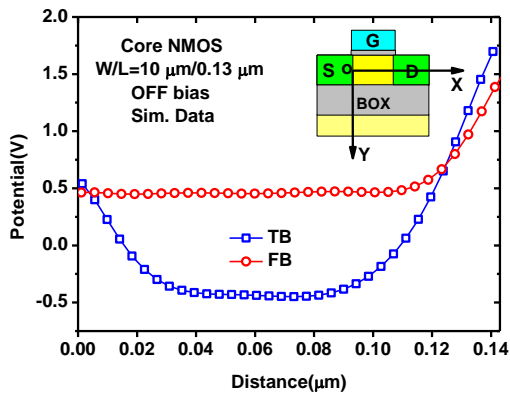


Figure 6. The simulated body potential along the channel length (X direction) at the middle depth of the body region under OFF bias condition for the core FB and TB devices.

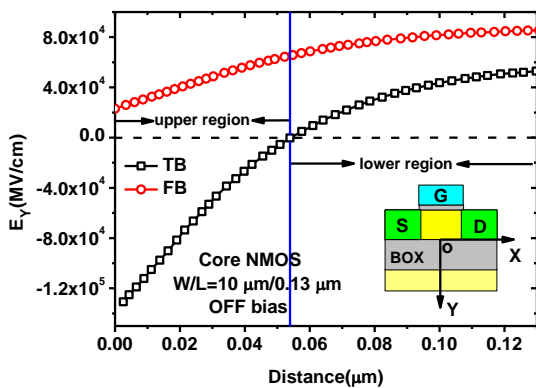


Figure 7. The simulated electric field strength (E_Y) along the depth (Y direction) at the middle region of the BOX under OFF bias condition for the core FB and TB devices.

IV. CONCLUSION

The comparison of TID effects for FB and TB PD SOI nMOSFETs is analyzed and discussed. The enhanced back-gate threshold voltage shift for the TB device under OFF bias condition is further confirmed by the device

simulation, which is related to the distinct electric field distributed in the BOX layer.

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