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A Reliable, Process-Sensitive-Tolerant Hybrid Sense Amplifier for Ultralow Power SRAM

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***Abstract*—A novel ultra high speed, compact and least sensitive to process variation, hybrid sense amplifier is designed for ultra low power SRAM. Precisely sized current mode circuit (CMC) is designed to provide differential current from bit-lines. We eliminate the global sensing stage to save silicon area and sized the output buffers to achieve full logic swing at the output of proposed sense amplifier. The proposed design improves the sensing delay and shows excellent tolerance to process variations as compared to best published latch type sense amplifier. Extensive post layout simulation results based on 45nm standard CMOS technology have verified that 38.8% reduction in sensing delay and 83.6% reduction in power dissipation is achieved compared to the best published designs under similar cell current (I_{cell}) and bitline capacitances. The total power delay product is 0.22fJ. Furthermore, the new design can operate down to a supply voltage of 0.6V. These attribute of the proposed sense amplifier makes it judiciously appropriate for the use in the contemporary wireless sensor SRAM macro, which continuously pine for ultra low power and high-speed characteristics. In addition, the proposed design exhibits low sensitivity to bitline and dataline capacitance, capacitance mismatch.**

***Index Terms*—SRAM, read/write static noise margin, CMC, power, speed, sense amplifier, CMC.**

I. INTRODUCTION

Scaling worsens transistor leakage and performance variation due to statistical fluctuation during the process fabrication and short channel effects. Therefore the conventional SRAM design presents increasing challenges and competition. Low voltage memories are crucial components of state-of-the art VLSI/ULSI systems. Thus low voltage SRAM have been extensively researched and developed for rapidly growing market of Tabs, PDA and medical equipments. Although the components becomes faster when evolving to deep sub-micron technologies signal delay over long interconnects constitute a major bottleneck in achieving higher circuit speed. The key to low-power in the SRAM is to reduce the signal swings on the high capacitance bit-lines [1], [2]. Sense amplifier is the most critical circuits in the periphery of CMOS memory [3]-[6]. The performance of sense amplifier strongly affects memory access time, and overall memory power dissipation [3]. As with other integrated circuits (IC's) today CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to sense amplifier in memories [7]. So increased memory capacity usually comes enhanced bit line parasitic capacitance [8]. This increased bit-line capacitance in turn slows down voltage sensing and makes bit-line capacitance swings energy expensive resulting in slower and more energy hungry memories. Due to their great importance in memories performance sense amplifier have a very large class of circuits. The need for increased memory capacity, higher speed and lower power consumption has defined a new operating environment for future sense amplifiers. As memory size increases sense amplifier design faces serious design challenges. 1) Decreasing memory-cell area to integrate more cells on single chip reduces the current that drives the heavily loaded bit-line. This cause an even small voltage swing on the bit-lines; 2) Decreased supply voltage reflects in smaller read static noise margin (RSNM) and write static noise margin (WSNM). This in turn affects sense amplifier reliability [9].

This paper is organize as follows section II discusses the conventional voltage latch sense amplifier, Voltage/current mode SA [10] and proposed design. Section III describes the designed work and its operation. In section IV we represent impact of process variations on sensing, read failure and layout of proposed design. Section V discusses the results and comparison. Finally section VI concludes the paper.

II. THE PROPOSED SENSE AMPLIFIER

A commonly used latch sense amplifiers are classified as (1) latch type sense amplifier shown in Fig. 1 [7], is commonly used due to its advantages of low power dissipation and high speed. However, latch type SA's are vulnerable to sensing failure, which is referred to as the parametric failure caused by malfunction of the sense amplifier due to insufficient sensing margin against the input offset voltage [11]. (2) Voltage/current mode sense amplifier [10]. The parasitic resistance of a metal or poly silicon line has a significant influence on the signal propagation delay over the interconnect line from local to global sensing stage, this increase the sensing delay. So in proposed hybrid mode SA we eliminate the global sensing stage to compact the design and chip area. Proposed sense amplifier with read cycle only memory

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system is shown in Fig. 2. It consists of a symmetrical structure of a four pMOS transistors (P2-P5), which configure current mode circuit (CMC). A CMC is essential a linear, current buffer that ties the bitline to a known voltage and realize a virtual short circuit across the complementary BLs, i.e. $V_{BL}=V_{BLB}$, input to CMC has a form of current and output current creates a charge variation at the intermediate nodes C,D. Which results in a sufficiently large output voltage by precisely sized pair of inverter (P6, P7, N1, N2). Here CMC eliminates the bitline equalization circuit due to virtual short circuit at node A, B this property makes it insensitive to the bitline capacitance. Transistors P0 and P1 are used to pull the bitlines close to supply voltage to attain memory cell stability and soft error immunity. Two nMOS (N3, N4) transistors forms data line discharge mechanism to precharge datalines capacitance C_{DL} and C_{DLB} to nearly ground potential.

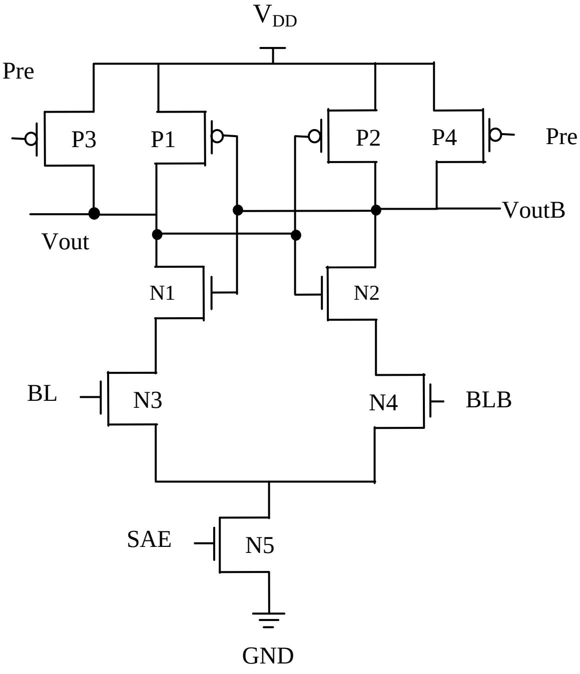

Figure 1. Conventional voltage latch sense amplifier.

III. SIMULATION SETUP & TIMING PATH

The operation of the sense amplifier shown in Fig. 2 has two phase namely standby and sense signal amplification phase. In the standby phase, CS signal is kept 'high' and discharge signal (DSC) is 'high' to precharge the dataline capacitances to gnd via transistors N3.N4. During standby C, D are at low potential (near Vth). Two output inverters are also in cutoff mode and no DC current flows except sub threshold current.

In the sensing phase WL and CS signals goes 'high' and 'low' respectively, memory cell at the upper is selected. As a result BL will drop to a lower level than V_{DD} during a read access and generate differential current signal as input to CMC. Because memory cell draws current I_{cell}, right hand leg of sense amplifier must pass more current than left hand leg results in a charge variation at the intermediate node C, D. Precisely sized output buffer will sense voltage at C and D and amplify it to a full CMOS logic level. Since no differential discharging of bitline capacitance is required to sense cell data, these signals propagate almost instantaneously to CMC. Simultaneously discharge signal turn off N3 and N4 allowing DLs voltage to change freely according to cell data and charge the C_{DL} and C_{DLB}. Precharge (gnd) time of nMOS devices N3-N4 is crucial here especially at near threshold. For lower V_{DD} precharge time of N3 and N4 piling up and degrades sensing delay. As number of column increases DL capacitances C_{DL} and C_{DLB} increases in this case size of N3-N4 plays major role to discharge the datalines capacitances.

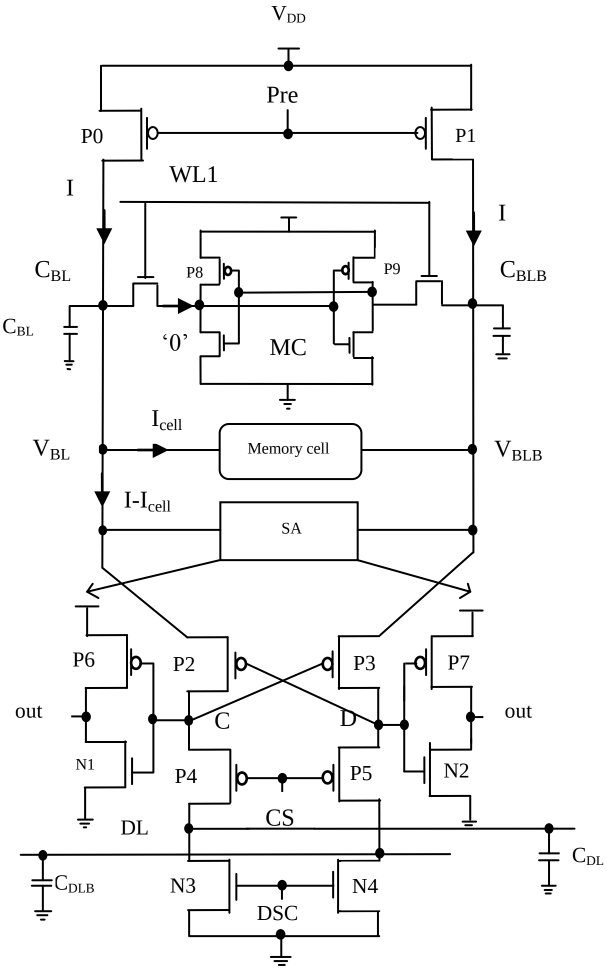

Figure 2. Schematic of proposed hybrid sense amplifier with read only memory system.

IV. IMPACT OF PROCESS VARIATION & SENSING FAILURE ANALYSIS

Impact of V_{th} variation, channel length (L) mismatch and width (W) mismatch on the failure probability of sense amplifiers is dominating on nanoscale in circuit design. With large V_{th} mismatch, failure probability of sense amplifiers increases drastically and functional yield goes down. A latch based sense amplifiers [7] are designed to be symmetric but with the process variations it becomes asymmetric. If the difference in voltage at bitlines, formed due to process variation, is sufficient to overcome bit differential voltage developed the sense amplifier may latch incorrect signal. A typical memory chip contains large number of sense amplifiers and if some sense amplifiers malfunction then it causes loss of functional yield. Hence it is necessary to design robust sense amplifier that have lower failure probability against process variations. We shown Failure probability of latch sense amplifier is more than the proposed design. In this work, we have presented simulation results for the voltage latch sense amplifier and proposed design. This section shows superiority of the proposed sense amplifier design with voltage latch counterpart in terms of the sensing failure and design yield. We design both topologies on same technology i.e. 45nm to make fair comparison.

Fig. 3 shows circuit characteristic of latch sense amplifier for V_{th} distribution (3σ) obtained by Monte Carlo simulation of 1000 samples. It can be observed that out of 1000 samples latch type sense amplifier have lower functional yield and higher failure probability. Similarly Fig. 4 shows for the proposed design that all the samples yield correct result. The proposed design is more insensitive to the V_{th} variation. Fig. 5 shows layout view of proposed design and referenced design. Layout of both topologies is optimized to achieve less silicon area, multi fingering concept is exploited to reduce gate resistance.

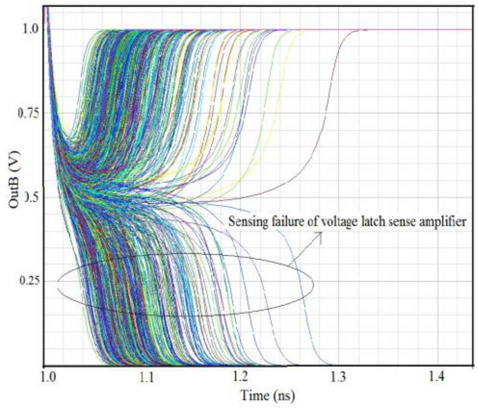

Figure 3. Output characteristics for V_{th} distribution (3σ) obtained by Monte Carlo simulation for 1000 iterations for voltage latch sense amplifier.

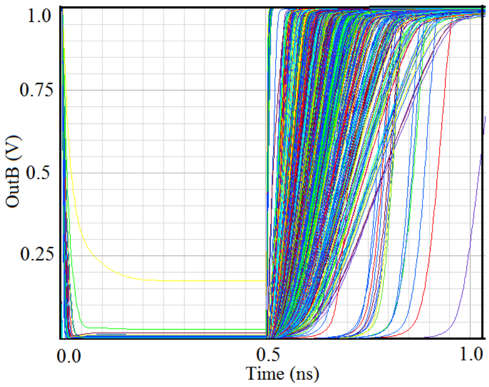

Figure 4. Output characteristic of proposed sense amplifier for V_{th} distribution (3σ) obtained by Monte Carlo simulation for 1000 iterations.

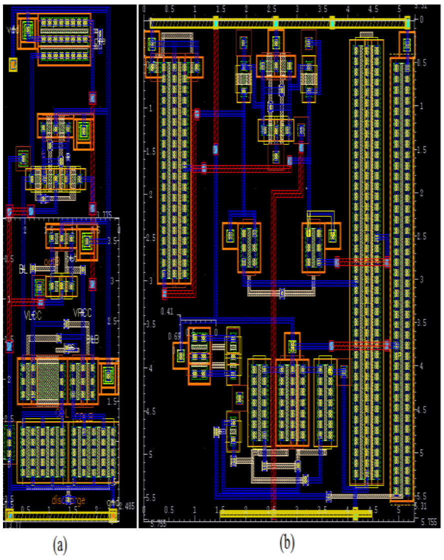

Figure 5. Layout of proposed (a) and referenced (b) sense amplifiers with read only memory system.

V. SIMULATION RESULS & PERFORMANCE EVALUATION

Delay is a most mature performance parameter for SRAM. Here proposed design extensively has been optimized and simulated using cadence Spectre on a 45nm technology node, balancing the tradeoff of speed and power. We optimized layout of SA with 6T memory to diminish parasitic and chip area. The proposed SA active area is the smallest among the (see Table I) published designs. All transistors in the three designs have a constant channel length (L) of 45nm and optimized channel widths to make fair comparison. Simulation results for both design shows proposed design exhibits lower sensing delay of 96ps at 1V and operating frequency is 1GHz with $C_{BL}=C_{BLB}=100fF$ and $C_{DL}=C_{DLB}=100fF$, simulation setup is common to all designed SA's.

TABLE I. COMPARISION SUMMARY OF TWO DESIGNS FOR $C_{BL}=100fF$ AND $C_{DL}=100fF$ AT 45NM CMOS TECHNOLOGY NODE AND 1GHZ OPERATING FREQUENCY

Design	Sensing Delay (ps)	Power Dissipation (µW)	Area on Chip (μm^2)	Power delay Product (fJ)
Proposed	96	2.38	6.48	0.228
[10]	157	14.53	16.38	2.281

Fig. 6 shows sensing delay distribution of proposed design with power dissipation at various supply voltage for $C_{BL}=C_{BLB}=100fF$ and $C_{DL}=C_{DLB}=100fF$. To account effect of parasitic in memory array having more number of columns and increased number of rows, we simulated both design with respect to variation in bitline capacitances (C_{BL}, C_{BLB}) and dataline capacitance (C_{DL}, C_{DLB}) from 100fF to 3pF, as shown in Fig. 7 and Fig. 8 Compare technique [10] can operate lower down up to 0.9V and proposed design can work up to near threshold 0.6V as shown in Fig. 6. It is shown that our design insensitive to C_{BL} and C_{DL} variation in terms of delay and power dissipation, manifested by the extremely low change in characteristic. Table-I summarizes the comparison of the designs, proposed design occupies the smaller active area than other designs. All transistors are obtained from circuit optimization to achieve minimum power delay product.

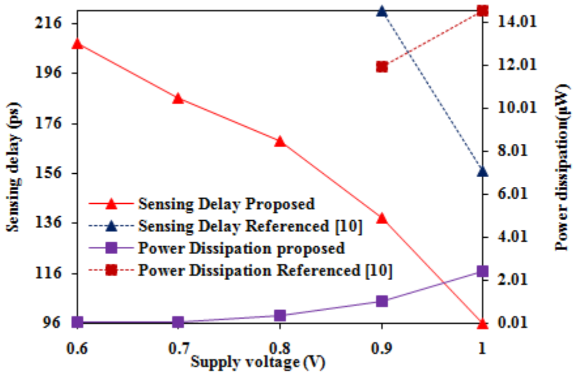

Figure 6. Sensing delay, power dissipation at various supply voltage for C_{BL}'s $=C_{DL}$'s=100fF.

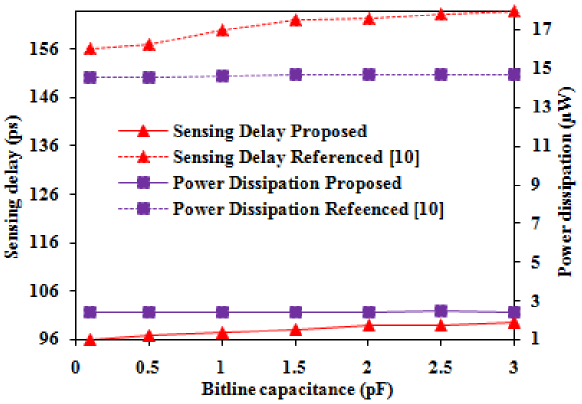

Figure 7. Sensing delay and power dissipation Vs bitline capacitance at 1V and 1.0GHz, for $C_{DL}=C_{DLB}$=100fF.

As temperature increases leakage current increases and dominates the standby power dissipation. Fig. 9 shows leakage current characteristic of both designs, proposed design has less leakage current in nA.

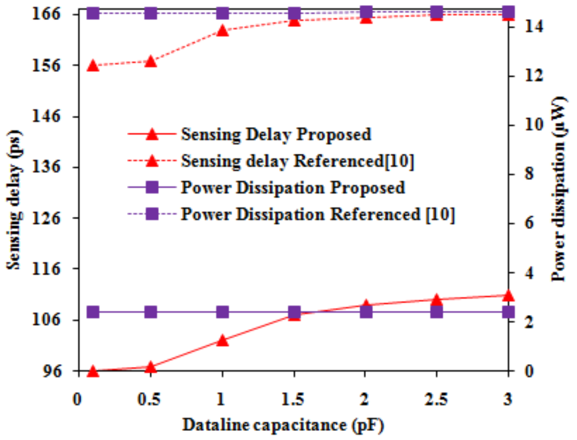

Figure 8. Sensing delay and power dissipation Vs dataline capacitance at 1V and 1.0GHz, for $C_{DL}=C_{DLB}$=100fF.

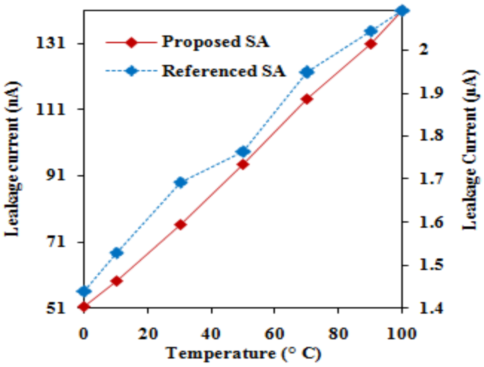

Figure 9. Leakage current Vs temperature at $C_{BL}=C_{DL}$=100fF at 1V supply voltage and operating frequency 1GHz.

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