A 6.5-μV/°C Offset Drift Compensation Technique for Dynamic Comparator

Daiki Tabira and Kenichi Ohhata
Department of Electrical and Electronics Engineering, Kagoshima University, Kagoshima, Japan
Email:k-ohhata@eee.kagoshima-u.ac.jp

***Abstract*—The offset drift of a dynamic comparator was analyzed using a simple model in order to clarify the offset drift mechanism. We found that it was possible to nullify the offset drift component due to size variability by controlling the gate common voltage (V_{com}). We conducted experiments to validate our estimations by using a test chip fabricated in 180-nm CMOS technology. Consequently, we found that the amount of variability of V_{TH} and W/L could be extracted from the measured offset voltage. Moreover, the offset drift was reduced to 6.5 μV/°C by controlling the temperature dependence of V_{com}.**

***Index Terms*—offset drift, comparator, analog-to-digital converter, CMOS analog circuits**

I. Introduction

Digital calibration has attracted a great deal of attention as a power reduction technique for analog-to-digital converters (ADCs) [1]−[5]. This technique drastically reduces the power of the comparator because it compensates for the offset voltage of the comparator; therefore, no preamplifier is required, and the comparator can be composed of small MOS transistors.

Digital calibration is divided broadly into two categories, that is, background and foreground calibration. In background calibration, the calibration is performed in every cycle. For example, the ADC of Chung et al. [5] performs the conversion operation in the first half of the cycle and the calibration in the second half. The comparator dissipates relatively large power in this ADC because the comparator needs to operate twice in a cycle. The ADC of Figueiredo et al. [2] has two fine ADCs that alternately repeat calibration and conversion; however, this ADC requires a large chip area.

In the foreground calibration, calibration is performed intermittently. This is generally done in the power-on sequence. Once the calibration is performed, the comparator operates in the normal mode; thereby, the issue of background calibration is solved. However, it is known that the offset voltage increases when the temperature changes after the calibration. The effective number of bits (ENOB) is reported to change by ±0.15 bit in a 6-bit ADC when the temperature varies in the range of 125°C after the calibration [1]. This suggests that the foreground calibration is effective in the case of 6-bit resolution; however, it generates unacceptable error in the case of 8-or-more-bit resolution.

The mechanism of the offset drift on the temperature change was analyzed using a simple model then a drift compensation technique was proposed. Moreover, the feasibility of the offset drift model and the effectiveness of the drift compensation technique were verified using a test chip fabricated in 180-nm CMOS technology.

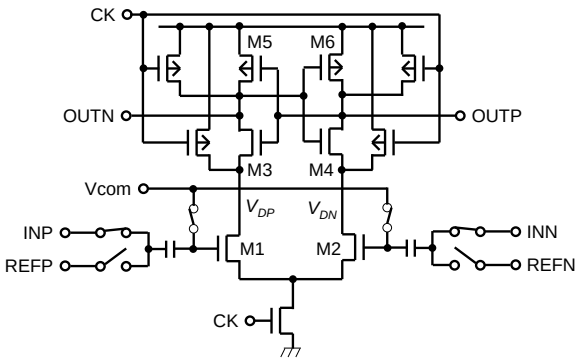


Figure 1. Schematic of stacked dynamic comparator.

II. Analysis of Offset Drift in Comparator

A schematic of a stacked dynamic comparator that is commonly used in ADCs and SRAMs [6, 7] is shown in Fig. 1. It is comprised of an input differential pair (M1 and M2) and a latch circuit (M3−M6). The difference between an input signal (*INP* and *INN*) and a reference voltage (*REFP* and *REFN*) is amplified by the input differential pair, then converted to digital signals (*OUTP* and *OUTN*) by the latch circuit. The power dissipation of this circuit is very small because no DC current flows. In the reset phase (*CK* = 0), the output node and the drain of the input differential pair (V_{DP} and V_{DN}) are precharged to V_{DD}. When the *CK* rises to V_{DD} and the phase shifts to the comparison phase, the differential pair is activated. The differential pair pulls down V_{DP} and V_{DN} to the *GND*. The pull down rates depend on the gate voltages of M1 and M2, so the voltage difference between V_{DP} and V_{DN} are generated according to the difference between the input signal and the reference voltage. The difference between V_{DP} and V_{DN} is latched by the latch circuit, and thus, the digital output signals are output. The input differential pair can be considered an amplifier using capacitive load.

Manuscript received January 23, 2013; revised March 13, 2013.

doi: 10.12720/ijeee.1.1.44-47

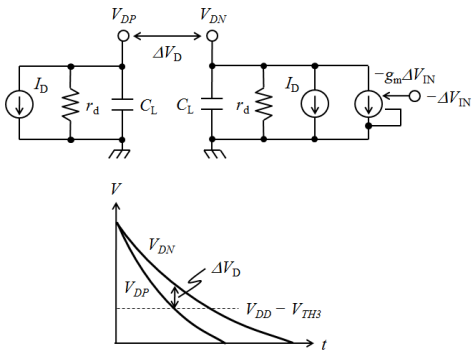


Figure 2. Equivalent circuit of amplifier.

An equivalent circuit of the amplifier is shown in Fig. 2, where C_L is the parasitic capacitance at V_{DP} and V_{DN}, and I_D, g_m and r_d are the drain current, transconductance and drain resistance, respectively. In this case, the gate voltage of M2 is lower than that of M1 by ΔV_{IN}. The latch circuit is activated when the voltage of V_{DP} reaches $V_{DD} - V_{TH3}$; therefore, the voltage difference of ΔV_D is generated. Thus, the voltage gain of the amplifier is expressed as

$$G = \frac{r_d V_{TH3} g_m}{r_d I_D + V_{DD}} = \frac{V_{TH3} g_m}{I_D (1 + \lambda V_{DD})} \quad (1)$$

where λ is the channel length modulation coefficient. The gain is about three to five for 180-nm CMOS technology. Therefore, the offset voltage from the latch circuit is small. The simulated offset voltage breakdown of the stacked comparator is shown in Fig. 3. As expected from the equivalent circuit, the offset contribution from the latch circuit is negligible, and the offset of the differential pair is dominant. Therefore, we made an offset drift model focusing on the input differential pair.

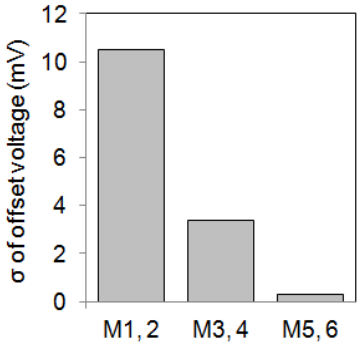


Figure 3. Breakdown of simulated offset voltage.

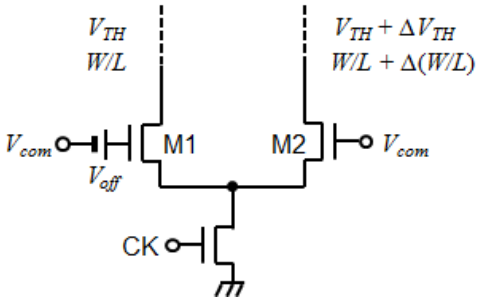


Figure 4. Differential pair and considered mismatch.

Let us consider the situation shown in Fig. 4 in order to analyze the offset voltage of the input differential pair (M1 and M2). The various mismatches in M1 and M2 cause the offset voltage. We consider the mismatch of the threshold voltage and the transistor size (W/L). Here, we assume the drain current is expressed as

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})(1 + \lambda V_{DS}), \quad (2)$$

taking into consideration the velocity saturation and the channel length modulation effect. The offset voltage of this model is expressed as

$$V_{off} = -\Delta V_{TH} + (V_{com} - V_{TH}) \frac{\Delta(W/L)}{(W/L)}, \quad (3)$$

where V_{com} is the common gate voltage (see Fig. 1) that determines V_{GS} of M1 and M2. Therefore, the temperature coefficient of the offset voltage is expressed as

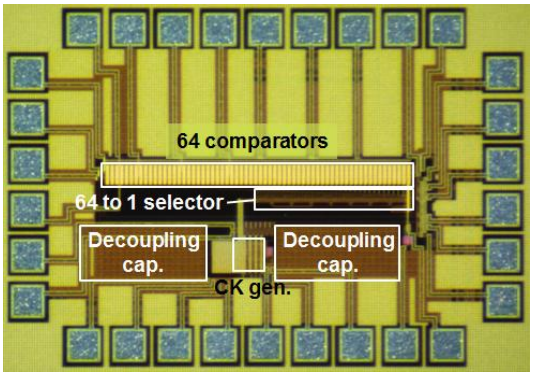
$$\frac{dV_{off}}{dT} = -\frac{d\Delta V_{TH}}{dT} + \left(\frac{dV_{com}}{dT} - \frac{dV_{TH}}{dT} \right) \frac{\Delta(W/L)}{(W/L)}. \quad (4)$$

Equation (4) indicates that the dependence of the offset on the temperature is determined by $d\Delta V_{TH}/dT$ and $(dV_{com}/dT - dV_{TH}/dT)$ because $\Delta(W/L)$ is independent from the temperature. The temperature coefficient of the offset deviates randomly because ΔV_{TH} and $\Delta(W/L)$ deviate randomly. This means that the offset drift cannot be compensated for collectively because the offset voltage in each comparator has different temperature dependence. However, if we design the temperature coefficient as $dV_{com}/dT = dV_{TH}/dT$, the 2nd term of (4) can be nullified. In this case, the temperature coefficient can be reduced to

$$\frac{dV_{off}}{dT} = -\frac{d\Delta V_{TH}}{dT}. \quad (5)$$

III. Experimental Results

With our model, the offset drift is determined by the temperature dependence of ΔV_{TH}, V_{com}, and V_{TH}. Moreover, the offset drift can be reduced by appropriately controlling the temperature dependence of V_{com}. We conducted some experiments in order to validate these estimations using a test chip.



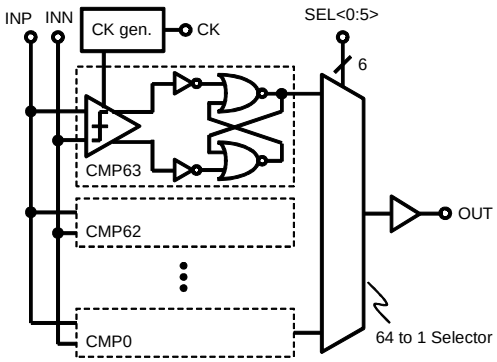


Figure 5. Photomicrograph and a block diagram of the test chip fabricated using 180−nm CMOS technology.

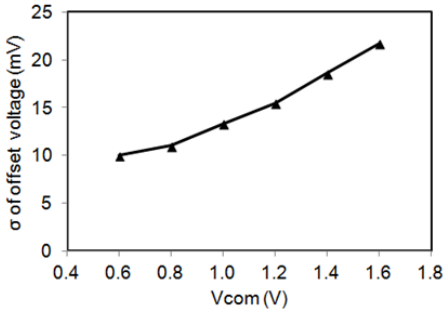


Figure 6. Measured standard deviation of the offset voltage dependence on the gate common level.

Fig. 5 shows a photomicrograph and a block diagram of the test chip fabricated using 180-nm CMOS technology. The test chip was composed of 64 comparators with the set-reset latches, a 64 to 1 selector, and a clock generator. The area of the comparator was 56 × 12.4 μm. The supply voltage was 1.8 V, and each comparator consumed 25 μW at an operating frequency of 100 MHz. The measured standard deviation of the offset voltage dependence on the gate common voltage (V_{com} in Fig. 1) is plotted in Fig. 6. The standard deviation of the offset voltage was approximately 10 to 20 mV and increased as V_{com} increased. This can be explained by considering (1). Higher V_{com} increases I_D; however, g_m is almost constant due to the velocity saturation effect. Therefore, higher V_{com} reduces the gain. This increases an offset contribution from the latch circuit (M3−M6). The measured offset distribution at V_{com} = 1.0 V is shown in Fig. 7(a). The measured distribution was approximately considered to be a Gaussian distribution. Equation (3) suggests that we can obtain ΔV_{TH} and $\Delta(W/L)/(W/L)$ separately by measuring the dependence of the offset voltage on V_{com} as shown in Fig. 7(b). Here, ΔV_{TH} and $\Delta(W/L)/(W/L)$ can respectively be obtained from an intercept and a slope of the graph that plots the offset vs. $V_{com} - V_{TH}$. The measured ΔV_{TH} and $\Delta(W/L)/(W/L)$ are shown in Fig. 7(c) and (d). The standard deviation of ΔV_{TH} and $\Delta(W/L)/(W/L)$ were 10.0 mV and 1.9%, respectively. The distribution of $\Delta(W/L)/(W/L)$ leaned towards positive because of an imbalance of the parasitic capacitance in the comparator due to the asymmetric layout. The standard deviation of ΔV_{TH} was approximately 1/1.4 of that of total offset voltage. This means that the contribution of ΔV_{TH} and $\Delta(W/L)/(W/L)$ to the offset voltage were approximately equal. As mentioned above, the offset components (ΔV_{TH} and $\Delta(W/L)/(W/L)$) can be extracted separately using our model, and this information can contribute substantially to reducing the variability in miniaturization of MOS transistors.

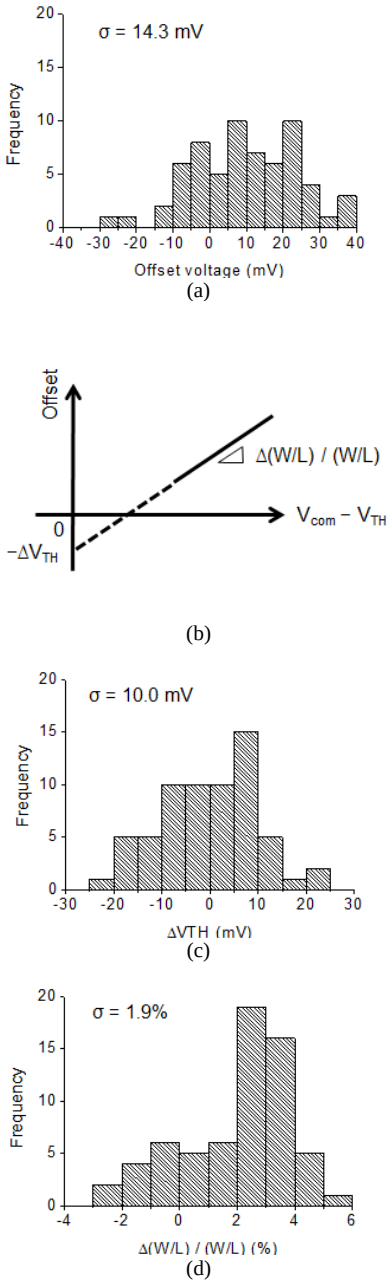


Figure 7. Measured offset distribution, (b) Extraction of ΔV_{TH} and $\Delta(W/L)/(W/L)$, (c) ΔV_{TH} distribution, (d) $\Delta(W/L)/(W/L)$ distribution.

The measured dependence of the offset drift on V_{com} is shown in Fig. 8. The offset drift (ΔV_{off}) was defined as the offset voltage difference between 100 and 25 ℃. The offset voltages at 25 ℃ were measured when V_{com} = 1.0 V. Then the offset voltages at 100 ℃ were measured changing V_{com} = 0.9 to 1.0 V. The offset drift strongly depended on V_{com}. The minimum value was obtained at V_{com} = 0.96 V which corresponds to dV_{com}/dT = 0.53

mV/℃. This temperature dependence is approximately equal to dV_{TH}/dT as expected from our model. The obtained offset drift was 0.49 mV (6.5 μV/°C) which is sufficiently small to use in 8-bit resolution ADCs.

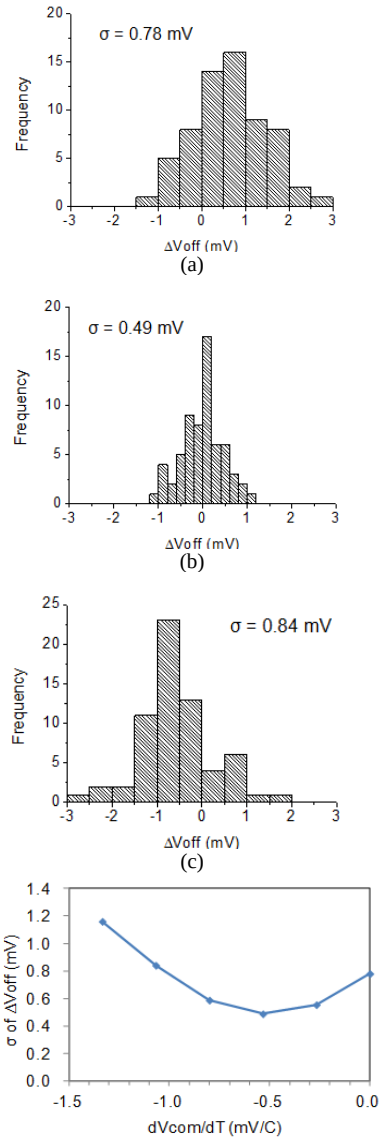


Figure 8. Measured Vcom dependence of the offset drift. (a) V_{com} = 1.00 V@25 ℃ –> 1.00 V@100 ℃, (b) V_{com} = 1.00 V@25 ℃ –> 0.96 V@100 ℃, (c) V_{com} = 1.00 V@25 ℃ –> 0.92 V@100 ℃, (d) Standard deviation of the offset drift vs. V_{com}.

IV. Conclusion

The foreground calibration technique is very useful to achieve a low-power and precision comparator. However, the offset drift prevents the widespread use of this technique. We applied a simple model to analyze the offset drift in order to clarify its mechanism and proposed a technique to compensate for the offset drift. The analytical results indicated that the offset drift component due to size variability could be nullified by controlling the gate common voltage. We conducted experiments to validate the estimation by using a test chip fabricated in 180-nm CMOS technology. Consequently, we found that it was possible to extract the amount of the variability of V_{TH} and W/L from the measured offset voltage. Moreover, we were able to reduce the offset drift to 6.5 μV/°C by controlling the temperature dependence of the gate common voltage.

Acknowledgment

This research was funded by the Semiconductor Technology Academic Research Center (STARC). The test chip in this study was fabricated in the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation. The authors would like to thank N. Kano, K. Ono, J. Naka, and O. Kobayashi for their valuable technical advice.

References

[1] C. Y. Chen, M. Le, and K. Y. Kim, "A low power 6-bit flash adc with reference voltage and common-mode calibration," in *Dig. Symp. VLSI Circuits*, June 2008, pp. 12-13.

[2] P. M. Figueiredo, P. Cardoso, A. Lopes, C. Fachada, N. Hamanishi, K. Tanabe, and J. Vital, "A 90nm CMOS 1.2V 6b 1GS/s two-step subranging ADC," in *Tech. Dig. ISSCC*, Feb. 2006, pp. 568-569.

[3] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. V. Weide, "A 480-mW 2.6-GS/s 10-b 65-nm CMOS time-interleaved ADC with 48.5-dB SNDR up to Nyquist," in *Tech. Dig. ISSCC*, Feb. 2011, pp. 180-181.

[4] Y. Asada, K. Yoshihara, T. Urano, M. Miyahara, and A. Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s subranging ADC," in *Proc. Tech. Papers A-SSCC*, Nov. 2009, pp. 141-144.

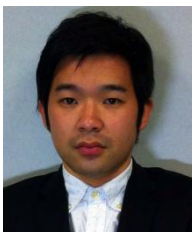
[5] Y.-H. Chung and J.-T. Wu, "A 16-mW 8-Bit 1-GS/s subranging ADC in 55 nm CMOS," in *Dig. Symp. VLSI Circuits*, June 2011, pp. 128-129.

[6] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, pp. 523-527, Apr 1993.

[7] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1148-1158, July 2004.

Kenichi Ohhata received a B.S. in physics from Nagoya University, Nagoya, Japan, in 1983, and a Ph.D. from Hosei University, Tokyo, Japan, in 2000. In 1983, he joined the Hitachi Device Engineering Co., Ltd., Chiba, Japan. Since then, he has been engaged in the research and development of high-speed bipolar and BiCMOS SRAMs and high-speed analog and digital ICs for communication systems. In 2004, he joined the Department of Electrical and Electronics Engineering, Kagoshima University, Kagoshima, Japan, as an Associate Professor. His current research interests include high-speed analog-to-digital converters and analog LSIs for high-speed optical communication systems.

Dr. Ohhata is a member of the Institute of Electronics, Information and Communication Engineering of Japan, and IEEE.



Daiki Tabira received the B.E. degree in electrical and electronics engineering from Kagoshima University, Kagoshima, Japan, in 2012. He is currently working toward the M.E. degree. He has been engaged in research on high-speed and low-power CMOS analog-to-digital converters since 2011.