Design of C-Band High Speed Pulsed Power Amplifier for Pulsed RADAR Applications

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***Abstract*—This paper describes the design and development of a narrow band two stage high speed Solid State Pulsed Power Amplifier (SS-PPA) working at 7.23 GHz frequency. The amplifier is designed by using commercial packaged PHEMTs. A pulse aggregate card has been developed to provide modulated pulsed bias. At room temperature, the PPA provides 17.58 dB gain yielding 26.58 dBm peak output power for 9 dBm input driving power. The measured rise and fall time of the final prototype is obtained as 25.0 ns and 19.2 ns respectively at 90 ns Pulse Width (PW) with 30 kHz Pulse Repetition Frequency (PRF). We report a description of the design of the amplifier along with an account of its performance made through a comparison of simulated and measured results with desired target specifications.**

***Index Terms*—pulsed RF, switching speed, pulse repetition frequency, distributed matching networks**

I. Introduction

The generation of high speed medium to high power microwave pulses is fundamental to the operation of various systems including pulsed radar [1-5], high speed communication systems [6, 7], medical electronics [8, 9]. Solid state power amplifier (SSPA) is often considered to be the best way to generate microwave power for next generation radar because of its wide operational bandwidth and high reliability than vacuum tube [10]. Recently Cobham Sensor System [11] developed an X-band 17 W pulsed amplifier module of variable PW with less than 40 ns rise/fall time. A design study carried out by Yi and Hong [12] used LDMOS FET to develop L-band 100 W PPA with reported rise/fall times of 28.1/26.6 ns respectively. However, most of the reported PPAs using hybrid technology offer higher switching time. But, in moving target indicator (MTI) and tracking radar applications, short pulses with low pulse repetition frequency (PRF) are desired to avoid ambiguities in range (no multiple time-around echoes) [13]. Thus high speed pulse power amplifier (PPA) with very low duty cycle is one of the important components in the transmitter chain of the pulsed radar front-end.

The design and performance of a two stage high speed and low duty factor solid state pulse power amplifier working at 7.23 GHz ± 100 MHz frequency to be used for radar transmitters has been described in this paper. The PPA is designed and fabricated by hybrid microwave integrated circuit (MIC) technology. This output signal can be frequency multiplied (x13) to obtain W-band (94 GHz) pulse tracking radar signal.

The PPA design begins with the selection of topology to meet overall gain and power followed by selection of proper active device for the frequency band of interest, pulse bias technique, stability analysis, matching circuits, circuit simulation and optimization etc. Advanced Design System (ADS-2008, update 2) provided by Agilent Technologies has been used for design, simulation and optimization of the amplifier. Circuit envelope simulation with distributed matching networks is used for designing the two stage amplifier. Finally the results are obtained from measurements using Agilent Technologies' PSG series signal generator (E8257D), PSA series spectrum analyzer (E4446A) and P-series power meter (N1911A).

II. Amplifier Design

A. Amplifier Design Topology

Since a single device cannot provide the required gain and power, then a solution implying a driver stage becomes mandatory, passing to a single-ended two-stage amplifier topology and the stages are cascaded to improve overall gain. Fig. 1 shows the energetic schematic representation of the two stage amplifier. The driver stage amplifier produces 20 dBm linear pulsed power from 9 dBm continuous wave (CW) input driving power and the power stage produces 27 dBm peak power; thereby adding 7 dB gain. The driver stage is matched to achieve maximum power gain, while the output stage is optimized for providing required output power level and efficiency.

The design parameters for the PPA are given in Table I.

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TABLE I. DESIGN SPECIFICATIONS

Parameters	Specifications
Operating Frequency	7.23 GHz
Band Width	200 MHz
Peak Output Power	27 dBm
Input Driving Power	(7-9) dBm
Pulse Width	(80-120) ns
Rise/Fall Time	≤10 ns
Pulse Repetition Frequency (PRF)	30 kHz

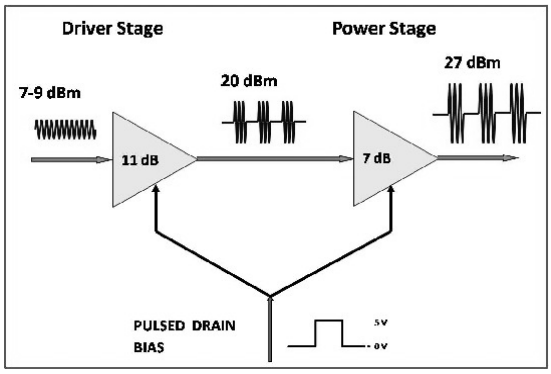

Figure 1. Energetic schematic representation of two stage pulse power amplifier.

B. Active Device Selection

Power amplifiers are characterized by parameters such as power compression, intermodulation distortion (IMD), power added efficiency (PAE) etc. At microwave frequencies, the most popular active device employed for this purpose is metal semiconductor field effect transistor (MESFET). However, for high speed pulsed power amplifier with narrow pulse width and small rise/fall times, the device cut-off frequency has to be high. It requires small gate length that translates to smaller channel thickness, and thereby, to higher doping in order to conserve drain-source current (Ids) performance. But it inevitably yields lower breakdown voltage and lower power density [14, 15], and thus puts limitations on use of MESFET for narrow pulse width applications. On the other hand, active channel and doping layer are physically separated in a pseudomorphic high electron mobility transistor (PHEMT) giving rise to higher cut-off frequency. PHEMTs, are therefore, mostly used for high speed, high efficiency and high frequency (millimeter wave) applications [16, 17].

For this design, RFMD's packaged PHEMTs (FPD6836P70 and FPD1500DFN) have been chosen [18]. This selected surface mountable, low parasitic packaged depletion mode AlGaAs/InGaAs Schottky Barrier gate PHEMTs are optimized for high frequency, high speed and low noise applications. The devices provide 22 dBm and 27 dBm power at 1 dB gain compression respectively for V_{ds} = 5 V and I_{ds} = 50% Idss (corresponding V_g = -0.45 V). The nonlinear and external package parasitic parameters of active devices are included in TriQuint TOM3 Scalable Nonlinear FET Model in ADS for simulation works.

C. Pulsing Technique for PHEMT Amplifiers

With an applied CW RF drive, pulsed output from a solid state pHEMT amplifier can be obtained in one of the following two ways:

- Switching the gate voltage between a low negative voltage, which results in efficient RF power amplification, and a higher negative voltage near the pinch off voltage, which effectively turns off the drain current (gate pulsing technique).
- Switching the drain voltage between the levels needed for efficient power amplification and zero volts (drain pulsing technique).

However, in gate pulsing technique, the lack of ideal gate control and pinch off causes leakage in off state leading to significant output power. On the other hand, in pulsed drain operation, due to high currents being switched, switching speed is somewhat lower. For the specified pulse width of the proposed PPA, drain pulsing technique is adopted as it is more efficient, provides simpler biasing circuit and offers high peak power [19].

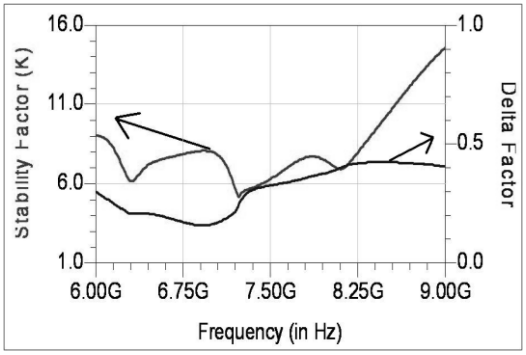

Figure 2. Rollett's stability factor (k) and delta (Δ) factor.

D. Stability Analysis

The stability of the individual stages has been intensively studied using different methods. First the conditions in Rollett's stability factors have been checked for both the stages (K>1, Δ<1). Besides, the pHEMT devices operating at class 'A' mode might present the parametric oscillations during the switching phase of the power amplifier [20]. A transient analysis of this amplifier is also carried out to detect these oscillations and the amplifier is found to be stable. Fig. 2 illustrates the stability analysis in pulsed mode indicating unconditional stability of the amplifier in the frequency range of interest.

E. Impedance Matching Networks

Since both the pHEMTs are unconditionally stable for the frequency band of interest, any source and load impedance will result stable operation.

The driver stage is simultaneous conjugate matched to achieve maximum available power gain [21]. From the s-parameters provided in the data sheet, the calculated source (Γ_{MS}) and load (Γ_{ML}) reflection coefficients (the corresponding impedances) at 7.25 GHz are Γ_{MS} = 0.484<-172.9 (17.4-j2.7 Ω) and Γ_{ML} = 0.297<112.3

(34.7+j20.9 Ω) respectively. This source and load impedances are matched to characteristic impedance (50 Ω) by using distributed microstrip lines as matching elements.

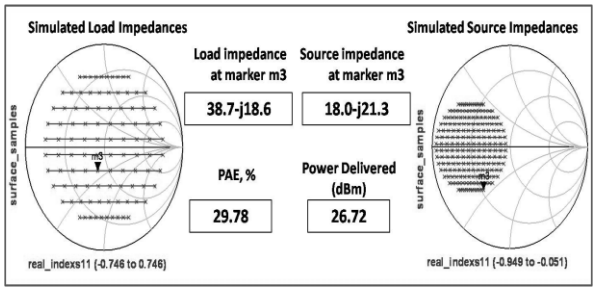

Figure 3. Simulated load and source impedance for maximum power and gain for power stage .

For the second (power) stage, the output side is matched to obtain maximum power and input side is conjugate matched to obtain maximum gain. This is accomplished by load and source pull technique [22, 23]. Using this technique in ADS software, as shown in Figure. 3, simulated load and source impedances for power stage are obtained as (38.7-j18.6) Ω and (18.0-j21.3) Ω respectively for 26.72 dBm delivered power with 29.78% PAE.

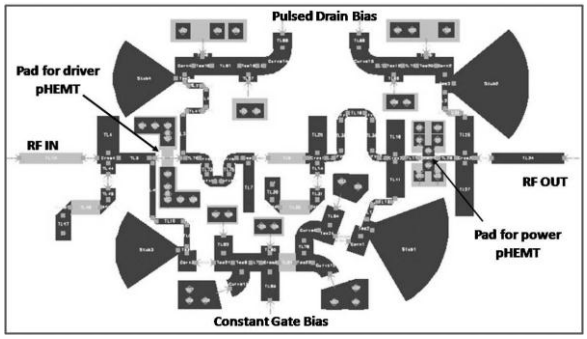

Figure 4. Layout of final two stage amplifier.

F. Simulated Results

The layout of the two stage amplifier including the input and output matching networks implemented with distributed microsrip line is shown in Fig. 4. Stages are cascaded by first matching them to characteristic impedance (50 Ω) and then connecting the matched stages in series. The bias decoupling network is designed by using a quarter wavelength 100 Ω transmission line and radial stub. A 30 Ω resistor is included in gate bias decoupling circuit to limit the gate current in order to prevent breakdown.

Fig. 5 shows the electromagnetic co-simulation results of the layout with vendor components. From the simulation results, 27.34 dBm peak output power is obtained for 8 dBm driving power with pulse width 100 ns and rise (fall) time 10 (12) ns. Further, the simulated input and output return losses, as illustrated in Figure. 6, are greater than 20 dB and 10 dB respectively in the frequency band.

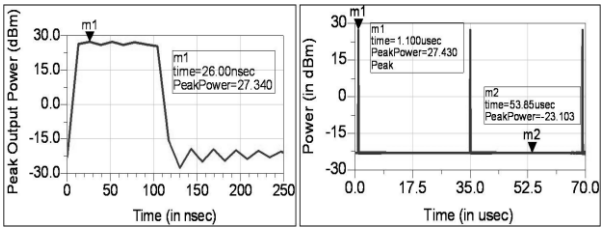

Figure 5. Simulated peak power of a single pulse (a) pulse-train (b) two stage amplifier for 8 dBm driving power.

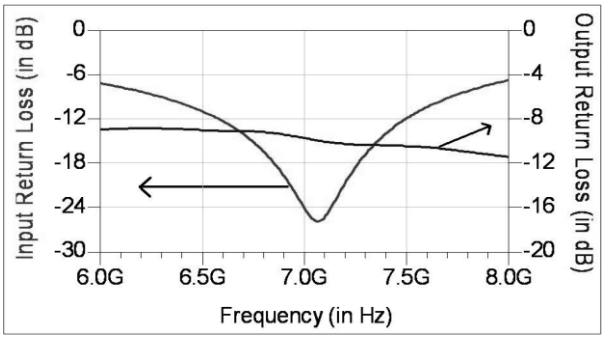

Figure 6. Simulated input and output return loss.

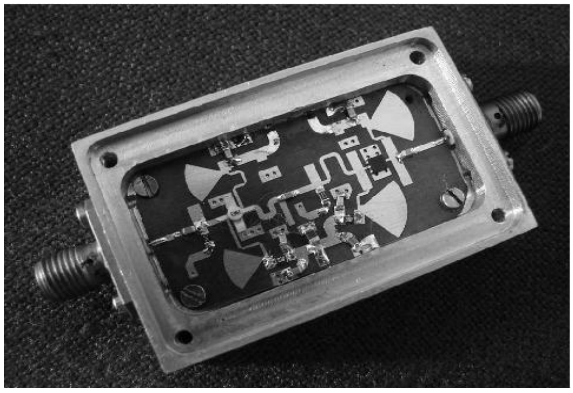

Figure 7. Prototype two stage amplifier housed in aluminum box.

III. Fabrication and Assembly

The circuit is designed and fabricated on Rogers RT/Duroid 5880 [24] double layer substrate material for its low dielectric loss at high frequency. The substrate material (10 mil thickness) possesses dielectric constant of 2.2±0.02 and both side copper cladded (thickness 35 μm). The fabricated two stage prototype amplifier mounted in aluminum box is shown in Fig. 7. Active devices (PHEMTs) are bonded with the circuit by using silver filled conductive epoxy (H20E from Epoxy Technologies). All other discrete components and 50 Ω SMA connectors are soldered directly on the substrate.

IV. Pulse Aggregate

To ensure the proper sequence of voltage application for depletion mode PHEMTs and also to provide pulsed drain modulation, a pulse aggregate card (Fig. 8) has been developed. It is designed to handle a pulse of width (80 ns-1 μs) with (20 μs-1 ms) pulse repetition interval (PRI).

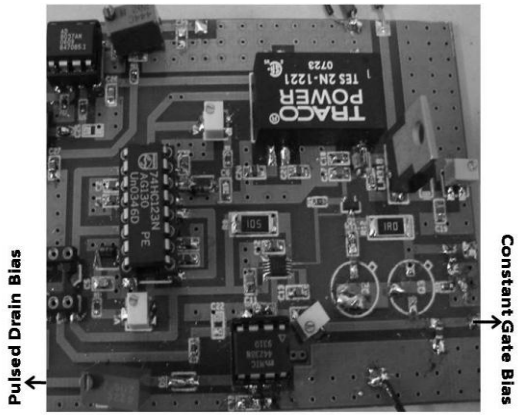

Figure 8. Pulse aggregate card.

V. Measurement and Results

The test and measurement of driver (first) stage amplifier (designed and developed separately) was carried out first [25]. The prototype amplifier has been first tested for stable bias point by applying bias voltages only. Once stable bias point is achieved, CW RF drive is applied to the input from signal generator. Fig. 9 illustrates the line spectrum of pulsed RF output signal for 8 dBm CW input power for the driver stage.

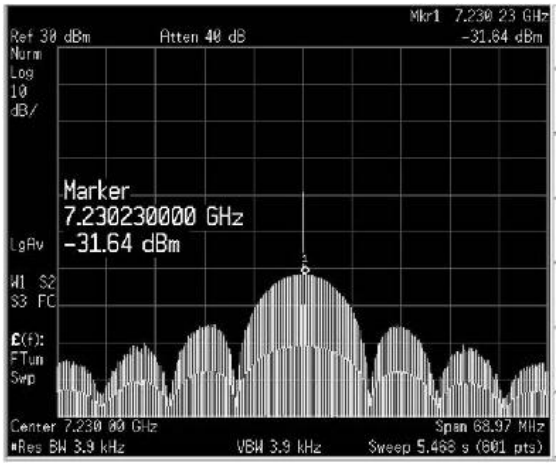

Figure 9. Line spectrum of driver stage for 8 dBm input power.

The line spectrum is the actual Fourier representation of pulsed RF signal in frequency domain. Here each spectral component when fully resolved represents a fraction of the pulse power [26], and the approximate peak power calculated from the main lobe power is 18.31 dBm (for 8 dBm input power).

The above power calculation does not take the cable loss of 0.36 dB (at 7.23 GHz) into consideration. The RF power during off state is -9.14 dBm indicating more than 27 dB peak-to-leakage power ratio.

Once the driver stage is set to perform satisfactorily, the final two stage amplifier has been subjected to testing and measurements by using Agilent Technologies' P-series power meter (N1911A). Fig. 10 indicates that the modulation pulse width to the drain terminal of the amplifier is about 100 ns with rise (fall) time of 18.5 (8.5) ns indicating the switching speed of pulse aggregate card.

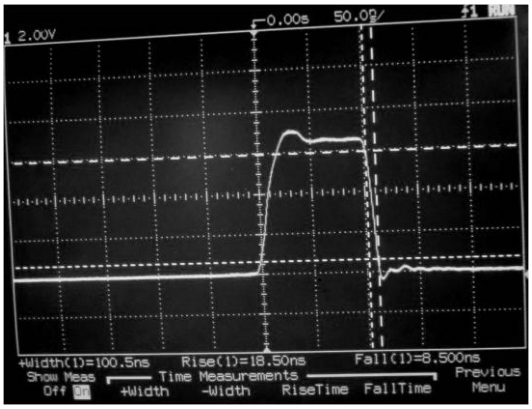

Figure 10. Modulation control pulse.

As shown in Fig. 11, 26.58 dBm peak power (15.95 dBm average power) is obtained for 9 dBm input power. The amplifier draws 26 mA average drain current from 5 V supply leading to PAE of approximate 24%. The RF power during off state is -16.37 dBm, indicating high isolation. The rise and fall times are measured as 25.0 ns and 19.2 ns respectively for pulse width of 89.8 ns with PRF of 30 kHz. This higher rise/fall time is mainly due to the underperformance of the pulse aggregate card.

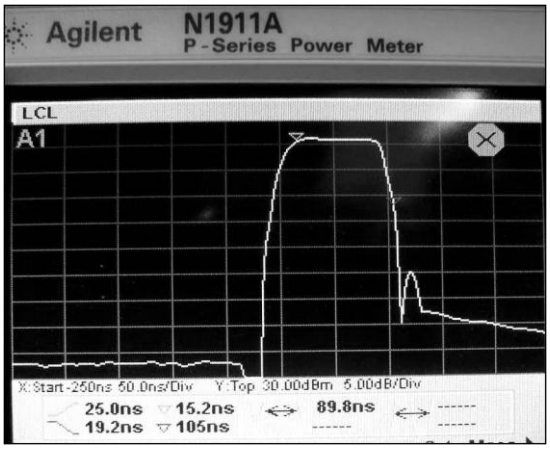

Figure 11. Measured pulse profile and rise/fall time of the prototype amplifier with peak power of 26.58 dBm.

Table II summarizes the practical results obtained from the prototype PPA along with the simulation results for the sake of comparison. The desired specifications of the PPA are also included to assess its performance.

TABLE II. Comparison Of Simulated And Measured Result With Target Specifications

Parameters	Specifications	Simulated Results	Measured Results
Operating Frequency	7.23 GHz	7.23 GHz	7.23 GHz
Band Width	200 MHz	200 MHz	200 MHz
Peak Output Power	27 dBm	27.34 dBm	26.58 dBm
Input Driving Power	(7-9) dBm	(7-9) dBm	(7-9) dBm
Pulse Width	(80-120) ns	(75-1000) ns	(80-250) ns
Rise/Fall Time	≤10 ns	10/12 ns	25/19.2 ns
Pulse Repetition Frequency (PRF)	30 kHz	(1-50)kHz	(1-50) kHz

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