Design and Automatic System Verification of Digital Baseband for UHF RFID Tag

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Abstract—**This paper presents the design and automatic system verification of digital baseband for Ultra High Frequency (UHF) radio frequency identification (RFID) tag, which is complied with a modified ISO 18000-6C protocol. Module-reuse approach and low power techniques are applied in the digital baseband to reduce the power consumption. And a novel verification strategy is discussed, which decreases the verification cycle greatly via function test mode and coverage test mode, and generates testcases automatically by using coverage-driven random-based approach. The strategy has many merits, such as a hierarchical architecture for reuse, inspecting low power design though assertion, locating bugs accurately, and linking C++ via direct programming interface (DPI). The tag chip is designed in a 0.18um CMOS process with a size of 89234 um^2. Simulation results verify the efficiency of the proposed methods.**

Index Terms—**RFID passive tag baseband, automatic system verification, coverage-driven random-based approach, SystemVerilog, DPI**

I. INTRODUCTION

UHF RFID technology has drawn a swirl attention because of its wide applications in many fields recently, such as passport, food safety, and production tracing, etc. [1]. As a technology utilizing wireless radio waves to transmit, identify, trace and confirm numerous objects, RFID is applied to identify articles or people fast, accurately, and inexpensively [2]. Based on power source, RFID would be classified into two types-active and passive. The passive tag is powered by Radio Frequency (RF) wave emitted from a reader, while the active tag has to work with a embed battery [3, 4]. It is crucial to design low power circuits for the tag, especially a low power digital baseband, for that the operating distance of the passive tag is highly dependent on the power consumption.

In this paper, our UHF RFID tag conforms to a modified protocol that is similar to but securer than ISO 18000-6C [5], for introducing a more complex encoding mode relative to Pulse Interval Encoding (PIE) in ISO 18000-6C and more complicated commands management. Different from PIE which encodes one bit one time, the encoding mode of forward link, truncated pulse position encoding (TPP), encodes two bits one time with more security [6].

Comparing with [7], the design provides a novel low-power cost architecture, in which central controller is the vital part. The central controller manages the other components' activity to reducing power consumption of overall system. Besides several advanced low power design techniques are adopted to reduce both dynamic power dissipation and static power cost. As well as, module-reuse approach decreases the chip area.

Furthermore, as an inevitable part of digital design process, verification turns into a bottleneck affecting high-spread digital design [8]. Ref. [9] proposed a full verification with an automatic stimuli generation. Whereas, the proposed verification environment is fully automated and broadly exploitable, that is supported by both its testcases generation mode and automatic testbench architecture.

The features of the proposed automatic verification strategy are: the application of coverage-driven random-based approach [10], function test mode and coverage test mode, hierarchical architecture, locating bugs accurately, assertion inspecting low power design, DPI. The proposed assertion concerns about the performance, not just about functional behavior [11]. DPI offers an easier way to interface with C and C++ [12], which are the programming languages of our reference model (RM).

The rest sections are organized as follows: Section 2 gives an overview of the design of RFID tag. Section 3 details the input stimulus generation and the automatic verification strategy. The project results are described in Section 4. Section 5 concludes the paper at last.

II. IMPLEMENTATION OF DESIGN

The proposed tag system, as shown in Fig. 1, consists of antenna, analog section, Multi-Time Programming (MTP), and digital baseband. Antenna receives signal from reader, then the signal would be demodulated by analog front end. With regard to the digital baseband, our design implementation has 7 modules: Center_ctl, Clk_gen, TX, RX, CRC (Cyclic Redundancy Check), Rnd_gen, MTP_intf, shown in Fig. 1.
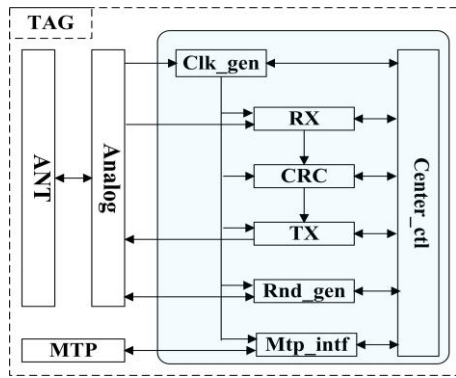
Figure 1. Architecture of the tag system.

As system manager, Center_ctl coordinates and controls the communication between other parts, taking into account the low power consumption with clock gating. Clk_gen, the clock generator, generates different kind of clock, such as system clock, clock for decoding, and clock for encoding, to meet the requirements of different modules of the clock and low power consumption. RX, the receiver, receives and decodes the signal from reader. TX, the transmitter, supports both FM0 (bi-phase space encoding) and Miller encoding method. CRC, as a reusable module, doesn't only check the received data, but also calculates CRC for TX. Rnd_gen, the random generator, interacts with analog section to obtain random number. The digital baseband accesses MTP through MTP_intf.

Command process controlled by Center_ctl is divided into four working states, depicted in Fig. 2. The initial state of command process is waiting command state, in which the tag detects and decodes the signal from reader. Based on the received command and tag-state, related operations are taken in handling command state. The following state is replying state if tag needs to transmit data to reader according to previous state. Or the state is completing state, in which most signals and registers of TX and RX are reset.
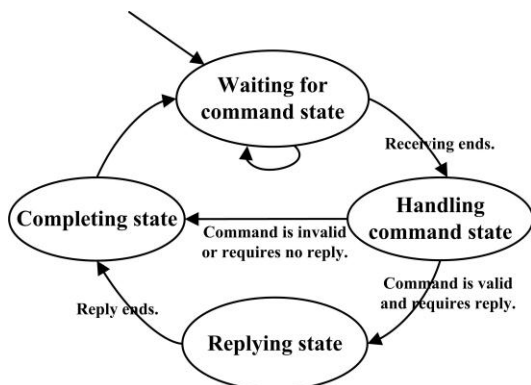

Figure 2. Four working stages for command process

The advanced low power design approaches adopted in our proposed system could be characterized into 3 directions. The details would be elaborated:

- Power Management with Clock Gating

Center_ctl generates the enable signal for each sub-module to activate or deactivate them based on the working state. Thus sub-modules are only active when they are required, in another way, lots of power consumption is saved. Moreover, reuse registers for storing received data and transmitted data reduce area and power dissipation, but the tough to control the reuse should be balanced.

- Low Operating Frequency

A relatively high frequency sampling clock is required to measure Trcal, but the overall response time described by the specification is less than 20ms, a large value. It is possible to reduce power consumption if we divide thedriving clock into three clocks with different frequency, clk_detect (measurement), clk_data (controlling) and clk_encode (encoding). In this way, most of the logic gates are driven by a slower clock.

Forward link, reader-to-tag communication, applies the TPP encoding mode with two transfer rates. While, backward link, tag-to-reader communication, supports both FM0 and Miller encoding method which is directed by the Query command and preamble transmitted by reader. Moreover, BLF (backscatter link frequency) of tag is determined by DR (divide ratio) from Query command and TRcal from preamble as shown in (1).

$$BLF = DR/TRcal. \qquad (1)$$

- Lower Operating Voltage

Though the voltage the system applies in 0.18um process normally is 1.8V, it is possible to reduce the supply voltage further as the internal clock frequencies are not high. For dynamic power dissipation is proportional to the square of operating voltage and static power dissipation is also proportional linearly to operating voltage. After our chip is manufactured, the operating voltage drops to 1.0V without is functionally errors. Thus the lower operating voltage reduces the power consumption effectively.

III. VERIFICATION STRATEGY

The goal of our simulation-based verification is to uncover all design bugs and improve efficiency of the whole progress. As tag is a finite state machine (FSM) shown in Fig. 3, the internal state of the tag directly determined by the received command sequence.
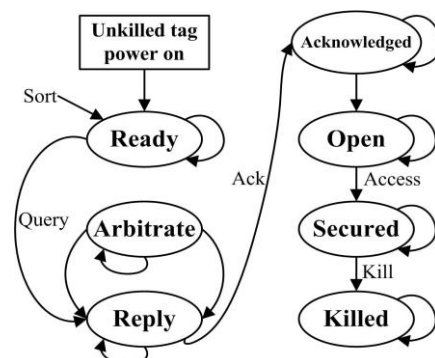

Figure 3. State diagram of our tag.

In the case of an incorrect state, the tested commands could not aim at desired cases for DUV's wrong

operating path. Some states and large test corners could not be achieved if DUV is stimulated by a set of large commands previously, for that many bugs usually contain in DUV in early days [13]. Nevertheless, the proposed verification strategy solves this problem, which meets the requirements of the whole design flow.

A. Testcases Generation

- Two testcase-generate modes

To alleviate the problems above, this paper proposed a method to generate command sequences in two testcase-generate modes, function test mode and coverage test mode.

In function test mode, a command sequence that drives DUT to achieve the desired state would be generated after configuring the testbench. In the protocol, the internal FSM of tag has Ready, Arbitrate, Reply, Acknowledged, Open, Secured, and Killed. There are most concerns about configuring arguments and transference of states to hit corners.

On the other hand, when coverage test mode is selected, a sequence with a large number of random commands would exist. As the sequence could be one instance of an infinite possible set, some metric helps us to elevate the length (the number of commands). Considering the fact that tag-state the more frequently changes, the more case corners are covered, the command sequences tend to make the tag transfer to different states frequently in this mode. An iterative method is applied to generate the shorten length. This mode gets its maximum value only if function test mode has been fulfilled already and most of bugs have been removed.

- Coverage-driven random-based approach

It is an important task of developing verification environment, to collect functional coverage measurements and implement functional coverage models. Functional coverage is used at all times during the process of generating testcases, for that it records the characteristics or symptom in tested command sequences and internal status of DUV. Regarding DUV as a black box, commitment about design specification and functional coverage reports guides random testcases generator that can be constrained.

In addition, a command sequence contains not only the RFID applicable commands, but also invalid commands, which may have wrong CRC arguments, illegal operands, or are nonexistent ones. But the low possibility of meaningless commands is noticed in constraint. On the other hand, the operation of some commands relates to both tag-state and preceding command. For instance, tag received valid Kill command will be killed only if tag-state is Open and preceding commands are Access command that makes tag has kill privilege, so do write, read, erase command. And Access command is executed combining with Get_rn command. This kind of commands will be generated as a united body more often than as an independent one. In order to simulate the RFID tag working environment, some arguments of commands will be confirmed after tag has transmitted response data pack (RDP) such as handle argument.

B. Automatic Testbench Architecture

The testbench is configured firstly according to the test target. Then DUT is tested automatically in verification environment, containing sequence generation, driving, receiving, and comparison. Verifying tag starts from sequencing commands generation and ends at incorrectness emerging or the termination of the test cycle.

Furthermore, the advantage of the proposed automatic architecture fulfilled in SystemVerilog is a reusable hierarchical architecture, locating bugs accurately, assertion inspecting low power design, applying DPI, all would be detailed in the following.

- Reusable hierarchical architecture

This overall testbench architecture consists of various components which depart into 5 layers: test layer, scenario layer, functional layer, command layer, signal layer, shown in Fig. 4. After configuring Test only, design will be test under a desired environment. Thus hierarchical structure provides a more flexible and reusable way to adjust the verification plan.
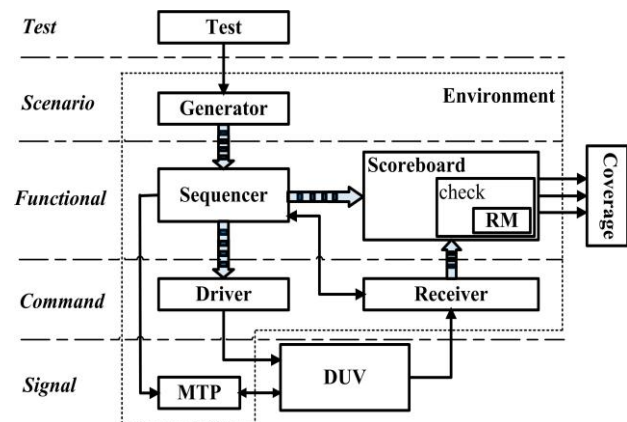

Figure 4.   Layered testbench for tag automatic verification.

Generator introduces test programs exploiting an internal command library that describes the constitution of the valid commands, as well as some invalid commands with error code or illegal arguments. The scheme configured in Test guides Generator to produce a sequence of commands towards the test target depending on coverage-driven random-based approach.

Sequencer manages the work flow of the other components by controlling transaction flow. Owing to the features of RFID system, it doesn't only send commands sequence with assistant stimuli to Driver and Scoreboard sequentially, but also instructs Receiver to decode in correct decode-mode, extracts handle argument from Receiver and configures data storage in MTP. As another component of functional layer, Scoreboard collects the stimuli to send to RM. Utilizing the C++ RM via DPI provides an automatic method to generate expected data for compare.

At command level, the DUV's inputs are driven by Driver which supports TPP encode mode in two transfer rate. While, The DUV's output drives the Receiver that could decode the signal in FM0 or miller mode and

groups the decoded data and other signals together into mailbox transmission.

At the bottom, the signal layer contains DUT, MTP and the signals that connect each other and to upper layer. MTP is a VIP (verification IP) provided by the foundry along with technology library. The initial data in MTP storage will be configured as it is manufactured.

At last, functional coverage is an essential component to provide statistics of information about command sequence, command arguments, DUV output gathered by scoreboard. According to the functional coverage report, we can adjust constrained random testing (CRT) which can be applied to generate pseudo-random input stimulus for DUV.

- Locating bugs accurately

An approach to locate bugs is proposed, even the design is considered as a black box. For the reason that some important internal signals, such as tag-state and receiver_en, are outputted for testing, we can understand the internal information of the system clearly. Combining with the comparison between the output critical signals and expected value, bugs can be located effectively when mismatches appear.

- Assertion inspecting low power design

Assertion based verification is suited for checking temporal relationships of synchronous signals and the control logic. Aiming at the power management with clock gating in Center_ctl, assertions about enable signals are put forward. According to the implementation, the respective enable signals controlling sub-modules are determined FSM in Center_ctl. They, the assertions about FSM and enable signals, don't only helps to make sure that the state transition occurs correctly, but also to check the validity of low power design.

- Applying DPI

In this strategy the RM written in C++ is connected to testbench via DPI, so that an automatic comparison appears which is between simulation results and expected results offered by RM. Distinguished from PLI (programming language interface) used in [11], [12], DPI has less overhead and makes C routines be used as just another SystemVerilog routine in Scoreboard. No matter in terms of developing time, or in the simulation time, DPI shows the superiority in verification period.

IV. EXPERIMENTAL RESULTS

As our protocol dictates, there are 16 mandatory commands and 3 optional commands implemented in our project. Under TSMC 0.18 μm process, the tag chip with better performance than [13] is shown in Fig. 5, and the information of the design is presented in TABLE I. The design takes resource reused and considers low power. It can handle a -20%~20% data rate variation in both decoding and encoding and BLF ranges from 80 KHz to 640 KHz.

A prototype of the proposed verification approach is developed in SystemVerilog, and RM is designed in C++ which contains approximately 2500 lines C++ code. The verification strategy exploits Modelsim SE 10.0b for

simulating RTL and getting coverage figures. Some of the simulation results are shown in Fig. 6, (a) shows the wave about communication between tag and reader, and (b) shows a sample of a report partly.

In this work, the verification strategy is in a serious need of a mechanism that could generate testcases automatically to achieve the goal that all the critical corner cases could be hit almost. We desire maximum statement coverage and functional coverage chosen as out verification metric. Towards the end of the project, we achieved the coverage of 100 percent with a set of 2700 commands. Comparing with some customary approaches, the proposed verification strategy is more flexible, suitable and practical in design cycle of outstanding performance in testcases generation, testbench architecture, and verification flow path.
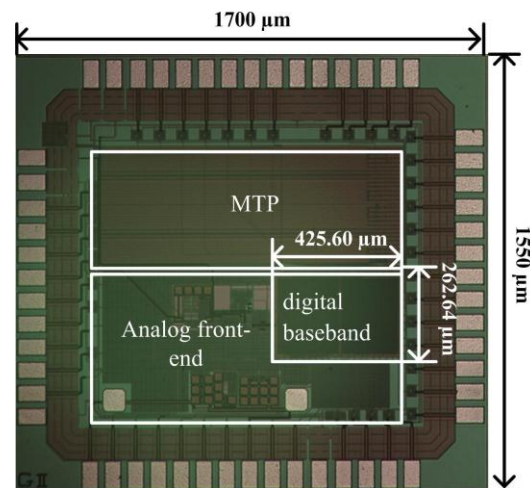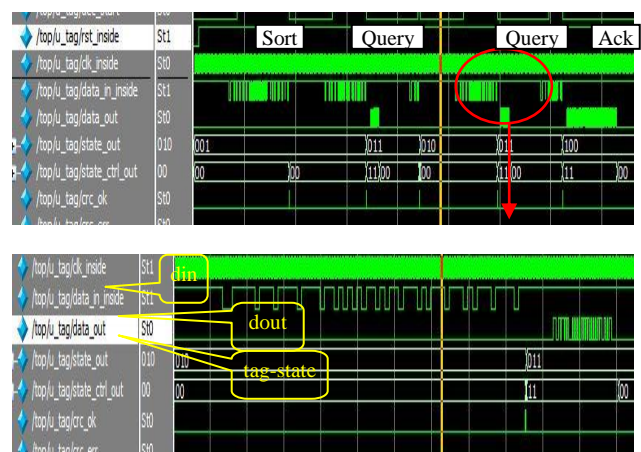

Figure 5.   The chip of UHF RFID tag digital baseband.

TABLE I.   SOME INFORMATION OF TAG DESIGN.

total standard cell area	89234 um^2
chip size	1 width 456, height 263, area 119928
chip ratio	66.8%
total dynamic power	11 1.6uw

(a) Part wave of tag ports

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46: Get_RN(16'b0000011000101011)(state=Opens)
    RM:101 1 0 0 00 0000 1 0 1 1 0 1 1 1  0010110000101011000001100010101101000
47: Access(4'b0011,16'b0010110000101010,16'b0000011000101011)(state=Opens)
    RM:010 1 0 0 00 0000 1 0 1 1 0 1 1 1  100001100000011000101011100001010001
    Error state    model: 010 design: 110
    Error response model: 10000110000001100010101110000101001101101 design:00000
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(b) A sample subset of a report

Figure 6.   Simulation results

V.   CONCLUSION

This paper presents the design and verification strategy of digital baseband for UHF RFID tag. Module-reuse approach and low power techniques are applied in the digital baseband to reduce power consumption. Automatic system verification with a novel testcases generation method is proposed, which applies two test modes and coverage-driven random-based technique. Besides, the testbench has been developed in SystemVerilog with a hierarchical structure which makes an easier access and reuse of the components. In order to collect complete coverage time-efficiently and locate design bugs, our approach focuses on a way to locate bugs accurately, assertion of clock gating, and DPI. The performance of our strategy has been evaluated on the selected metric and reducing development cycle. Future research directions include getting rid of redundant commands from testcases and how to improve convergent speed of verification.

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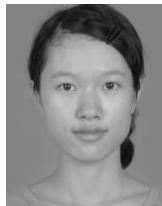
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