FPGA Implementation of SVPWM Technique for Seven-Phase VSI

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***Abstract*—This paper presents the performance investigation of FPGA implementation of SVPWM technique for seven-phase voltage source inverter (VSI). Seven-phase voltage source inverters are dominantly used to supply the seven-phase drives which are used for high power applications. In the SVPWM technique a large space vectors are detailed. A voltage source inverter with the proposed SVPWM is simulated in Matlab/Simulink. The performance of the 7-phase VSI is analyzed in terms of fundamental voltage and THD. In the proposed work, SVPWM algorithm is described in high-speed integrated circuit hardware description language coding and implemented in an XILINX Spartan 3A FPGA processor. The selection of zero and active space vector sequence are discussed and the possibilities of realization on FPGA are analyzed.**

***Index Terms*—FPGA, switching techniques, THD, voltage source inverter**

I. Introduction

Multi-phase VSI are becoming as a front end converter for multi-phase drive applications, such as ship propulsion, electric aircraft, and electric/hybrid electric vehicles etc. The multi-phase inverter circuit topology uses two switches connected in series as one inverter pole. The number of inverter poles depends on number of phases. For example, a three-phase inverter will have three inverter arms whereas a seven-phase inverter will have seven inverter arms. Conventional PWM technique adapted for conventional three phase VSI which can be extended for multi-phase VSI also. The most widely used PWM techniques for multi-phase inverters are the carrier-based SPWM and SVPWM [1]-[18]. The SPWM schemes are more flexible and easy to implement [1]-[3]. However the output waveforms contain more harmonics resulting in reduced fundamental component and efficiency. To achieve the better output voltage, the several space vector pulse width modulation (SVPWM) techniques are discussed. The SVPWM technique for the multi–phase induction machine has been widely reported in [4]-[8]. SVPWM technique for Asymmetrical six-phase and five-phase VSI are discussed in [9]-[16]. These issues are extension of three phase VSI. The SVPWM technique with seven phase voltage source inverter is discussed in [17], [18]. In this paper different combinations of switching techniques are analyzed. Only limited issues are available for SVPWM technique used in digital platform. Many issues related to SVPWM technique is implemented using the DSP platform. The DSP executes instructions sequentially and it requires more time for processing. The new software of field-programmable gate array (FPGA) is compute instructions parallel and it requires less time to execute [19]-[22]. The FPGA comprises thousands of logic gates, some of which are grouped together as a configurable logic block (CLB) to simplify higher level circuit design. The interconnections of the gates are defined by external RAM or ROM. The simplicity and programmability of FPGA design as the most favorable choice for prototyping an ASIC. The advent of FPGA technology has enabled rapid prototyping of digital systems.

In this paper FPGA implementation of SVPWM technique for seven-phase VSI is developed. An attempt is made in this paper for various simulation results are obtained for seven-phase inverter at different modulation indices for both in Matlab/Simulink and FPGA environment. The effectiveness of this method is investigated in terms of percentage increase of fundamental voltage and THD.

II. Power Circuit of Seven-Phase VSI

The power circuit of seven-phase VSI is shown in Fig. 1. The circuit consists of 7 half-bridges, which are mutually displaced by $2\pi/n$ degrees to generate the *7*-phase voltage waves. The input dc supply is obtained from a single phase or *3*-phase utility power supply through a diode-bridge rectifier. The voltages V_a, V_b, V_c, V_d, V_e, V_f and V_g are the inverter pole voltages connected to load terminals. It is seen that the switching states of each pole should be combined with each other pole to create the required 7-phase output voltages. The phase voltages of the inverter and modulation index are as given in the expressions (1) & (2). The Modulation Index (MI) is the control parameter of the inverter which adjusts the

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output voltage of the inverter according to the amplitude of the reference waveform. It is defined as the ratio of magnitude of the reference to magnitude of the carrier signals.

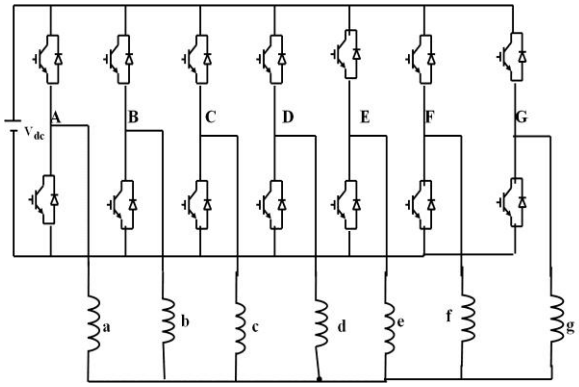


Figure 1. Power circuit diagram of seven-phase VSI

$$
\begin{aligned}
V_{aN} &= \frac{n-1}{n}V_a - \frac{1}{n}(V_b+V_c+V_d+V_e+V_f+V_g)\\
V_{bN} &= \frac{n-1}{n}V_b - \frac{1}{n}(V_a+V_c+V_d+V_e+V_f+V_g)\\
V_{cN} &= \frac{n-1}{n}V_c - \frac{1}{n}(V_a+V_b+V_d+V_e+V_f+V_g)\\
V_{dN} &= \frac{n-1}{n}V_d - \frac{1}{n}(V_a+V_b+V_c+V_e+V_f+V_g)\\
V_{eN} &= \frac{n-1}{n}V_e - \frac{1}{n}(V_a+V_b+V_c+V_d+V_f+V_g)\\
V_{fN} &= \frac{n-1}{n}V_f - \frac{1}{n}(V_a+V_b+V_c+V_d+V_e+V_g)\\
V_{gN} &= \frac{n-1}{n}V_g - \frac{1}{n}(V_a+V_b+V_c+V_d+V_e+V_f)
\end{aligned}
\tag{1}
$$

$$
M = \frac{V_{ref}}{V_{tri}} = \frac{Peak\ value\ of\ V}{0.5V_{dc}} \tag{2}
$$

The d_1-q_1 plane for seven-phase VSI, SVPWM using large space vectors and FPGA implementation of SVPWM algorithm are discussed detail in the following sections.

III. D_1-Q_1 Plane for Seven-Phase VSI

In a seven phase system the inverter space vectors are seven-dimensional space. A space can be decomposed into three two-dimensional sub-spaces (d_1- q_1, d_2-q_2 and d_3-q_3) and one single dimensional sub space (zero-sequence). The problems in the d_2-q_2, d_3-q_3 and zero sub-spaces are extensively reported in [15]. Therefore, in order to generate pure sinusoidal output voltages, SVPWM technique must synthesize fundamental component in the d_1-q_1 plane. In the proposed work, only the d_1-q_1 plane for different space vector is considered. Fig. 2 shows the d_1-q_1 plane for seven-phase VSI. In a seven-phase system the inverter space vectors are two-dimensional space as expressed in (3).

$$
Vref = \sqrt{\frac{2}{7}}\begin{bmatrix} 1 & \cos\alpha & \cos 2\alpha & \cos 3\alpha & \cos 4\alpha & \cos 5\alpha & \cos 6\alpha \\ 0 & \sin\alpha & \sin 2\alpha & \sin 3\alpha & \sin 4\alpha & \sin 5\alpha & \sin 6\alpha \end{bmatrix} \tag{3}
$$

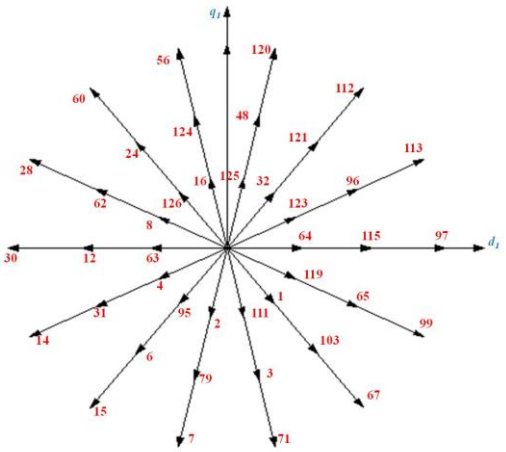


Figure 2. d_1-q_1 plane of seven-phase VSI

where α=2*pi/n

Thus d_1-q_1 plane can be visualized as being composed of three different space vectors, each plane can be divided into 14 sectors. In the proposed work, a large (outer-most) space vector is considered. This is the simplest extension of a three-phase SVPWM and only the outer most plane is considered in order to generate output voltages, based on the reference space vector. The large space vectors are discussed detailed in the following sections.

IV. SVPWM Using Large Space Vectors

In this section, the outer-most of large space vectors in d_1 –q_1 plane is considered. The input reference voltage vector is synthesised from two active vectors and zero space vectors respectively. The switching times are calculated by using the reference space vector $V_{ref,}$ magnitude of the larger plane and sector *(sec)* number respectively. The switching time sequence of active and zero space voltage vectors are derived from the expressions (4) & (5).

$$
\begin{aligned}
t_{al} &= \frac{|\bar{V}_{ref}|\sin(\sec\pi/7-\theta)}{|\bar{V}_l|\sin\pi/7}t_s\\
t_{bl} &= \frac{|\bar{V}_{ref}|\sin(\theta-(\sec-1)\pi/7)}{|\bar{V}_l|\sin\pi/7}t_s
\end{aligned}
\tag{4}
$$

$$
t_0 = 1/2(t_s - t_{al} - t_{bl}) \tag{5}
$$

Fig. 3 shows the phasor diagram for large space vectors of seven-phase VSI. Here, t_{al} and t_{bl} correspond to times of application of large space vectors. In sector 1, t_{al} is the time of application of the voltage space vector V_{97}, while t_{bl} is the time of application of the voltage space vector V_{113}. t_0 and t_{127} is the time of application of zero voltage vectors of V_0 and V_{127}. For odd sectors, the sequence of the switching period is *(t_0 t_{al} t_{bl} t_{127} t_{bl} t_{al} t_0)*, while in even sectors it is *(t_0 t_{bl} t_{al} t_{127} t_{al} t_{bl} t_0)* respectively. The maximum possible fundamental peak voltage of large space vector is V_{max}=*0.642*V_{dc}. The switching time sequence for large space vectors of sector 1 is shown in Fig. 4. It is seen that in one complete full cycle (t_s) has

divided into two half cycles ($t_s/2$). In the first half of the switching time sequence is zero space vector (t_0), two active space vectors (t_{al} t_{bl}) and zero space vector (t_{127}) respectively. The second half of the switching time sequence is a mirror image of the first cycle.

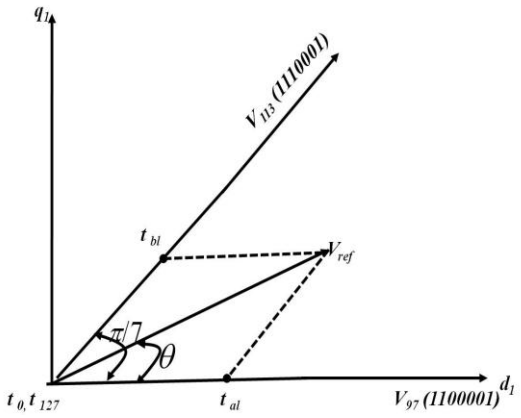


Figure 3. Phasor diagram of large space vector (sector 1)

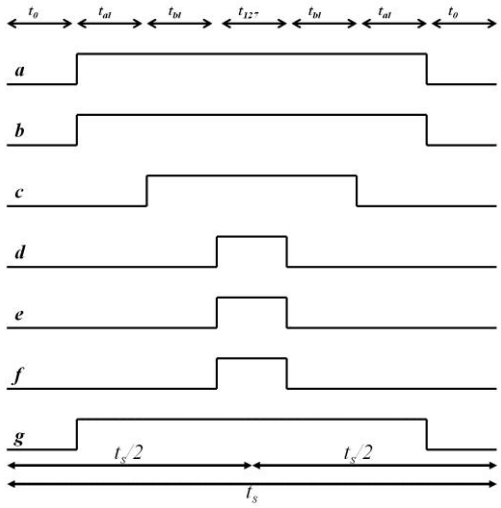


Figure 4. Switching time sequence of large space vectors (sector 1)

V. FPGA Implementation of SVPWM Algorithm

The SVPWM algorithm for 7-phase VSI has been implemented in FPGA. Table I shows the software version and target device utilized for this algorithm. This FPGA, belongs to the Spartan-3A DSP family from XILINX, has the basic Configurable Logic Blocks (CLBs) and flexible Look-Up Tables (LUTs). CLBs has high data storage capacity and hence perform a wide variety of logical functions. FPGA allows a great degree of freedom in the implementation of SVPWM algorithm and reduces the total amount of hardware needed and keeps the final cost at a reasonable point. The instructions are done with a 20-MHz clock, which is sufficient to achieve a real-time operation of the algorithm.

The general high speed integrated circuit hardware description language (VHDL) is employed for SVPWM algorithm coding. The steps involved in FPGA implementation of SVPWM algorithm are listed below:

- Determine the 7-phase reference voltages with symmetrical phase displacement.
- Transform 7-phase to 2-phase.
- Find the normalised reference vector from the 2-phase transformation.
- Identify the sectors in d_1-q_1 plane.
- Determine the switching time calculation for different space vectors (t_{al}, t_{bl}, t_0).
- Find the switching time sequence for odd and even space vector for large space vectors.
- Determine the modulating signals.
- Determine the high frequency carrier signals (10 KHz).
- Compare modulating signals with high frequency carrier signals.
- Turn on upper switches if mod≥car, turn on lower switches if mod≤car.

TABLE I. Software Version and Target Device

Product Version	ISE:12.1 (WebPack) - M.53d
Target Family	Spartan-3A DSP
Target Device	xc3sd1800a
Target Package	fg676
Target speed	-4
Tool Flow	ISE
Synthesis tool	XST (VHDL/Verilog)
Simulator	Modelsim-SE VHDL

VI. Simulation Results

The seven-phase inverter is simulated with the above said switching schemes and the results are observed. The switching frequency of the VSI is chosen as 10 kHz and the fundamental frequency is set to 50 Hz. The simulation parameter of seven-phase VSI is shown in appendix. The simulation results of the SVPWM, FPGA implementation of SVPWM are discussed in the following sections for different modulation indices.

A. Matlab/Simulink Simulation Results for SVPWM Technique with Seven-Phase VSI

The 7-phase VSIs is simulated with the pulses obtained by SVPWM technique. Fig. 5 shows the switching time period of t_{al}, t_{bl} and t_o respectively. Fig. 6 shows the resultant modulating signal for a modulation index of 0.85. The output phase voltage and its spectrum are shown in Fig. 7. It is seen that the output fundamental rms value is 0.4476 p.u. (0.633 p.u. peak) and THD is 47.08%. The adjacent and non-adjacent line-to-line voltages are shown in Fig. 8 to Fig. 10. From Fig. 8 it seen that the adjacent line-to-line voltage (a to b) rms is 0.3884 p.u. (0.5493 p.u. peak) and THD is 94.52%. The

non-adjacent line-to-line voltages (a to c) rms is 0.6999 p.u. (0.9898 p.u. peak) and THD is 40.72%. The non-adjacent line-to-line voltages (a to d) rms is 0. 8727 p.u. (1.234 p.u. peak) and THD is 35.32% respectively. From the simulation results the seven phase VSI has three pairs of line-to-line voltages. It is seen that the maximum line-to-line voltage of $1.9497V_p$ is obtained in the non-adjacent side (a to d).

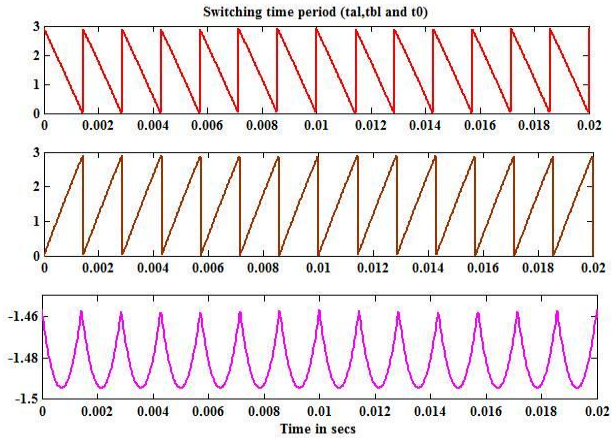


Figure 5. Time period for t_{al}, t_{bl} and $t_{o.}$

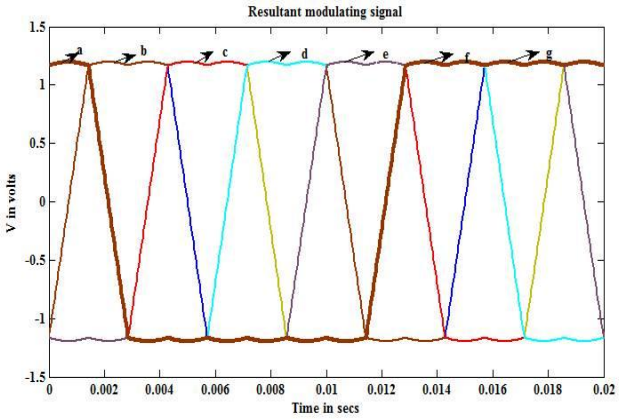


Figure 6. Resultant modulating signal for seven phase VSI

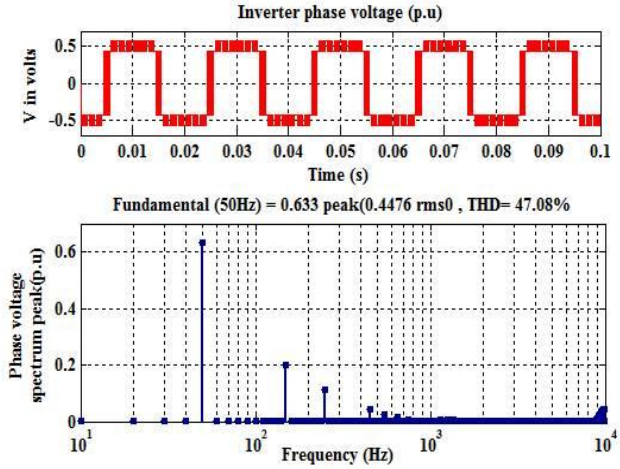


Figure 7. Phase voltage and its spectrum for MI-0.85

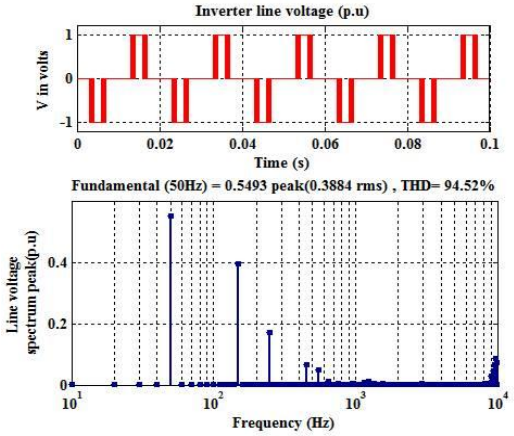


Figure 8. Adjacent line voltage (a to b) and its spectrum for MI-0.85

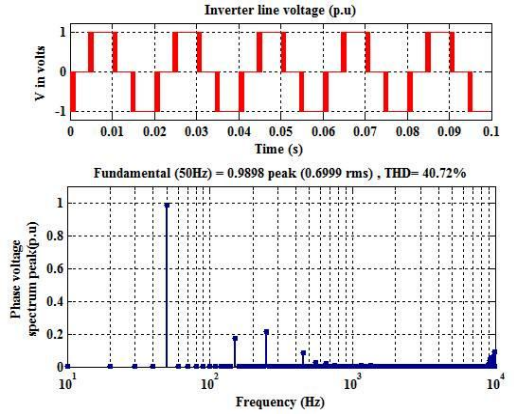


Figure 9. Non-adjacent line voltage (a to c) and its spectrum for MI-0.85

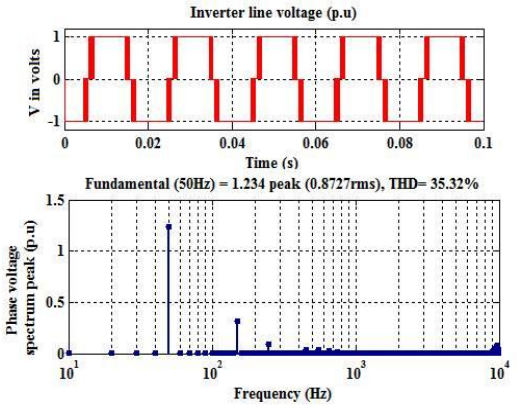
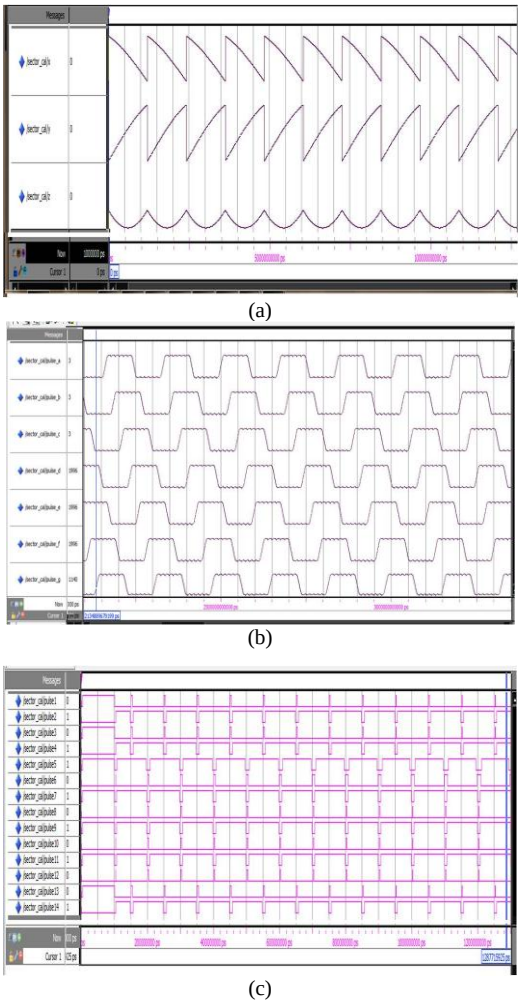


Figure 10. Non-adjacent line voltage (a to d) and its spectrum for MI-0.85

B. *Simulation Results of SVPWM in FPGA*

Fig. 11 shows the 7-phase VSI is simulated with the SVPWM pulses obtained by FPGA environment. Fig. 11 (a) shows the results switching time period of t_{al}, t_{bl} and t_o respectively. Fig. 11 (b) shows the resultant modulating signal for a 7-phase VSI. Fig. 11 (c) shows the switching pulses obtained from FPGA. In the real time implementation the switching pulses are used to activate the 7-phase VSI.



(a) (b) (c)

Figure 11. FPGA implementation SVPWM results

C. Comparison of Fundamental Voltage and THD for Different MI

Table II shows the percentage increase of fundamental voltage (phase voltage and line-to-line voltage) for different modulation indices. It is noted that the fundamental voltage is marginally high and also the increase in voltage reduces with decreasing modulation index. The non-adjacent line-to-line voltage and phase voltage maximum of 0.8727 rms and 0.4476 rms is achieved for modulation index is 0.85. It is seen that the THD reduction is observed for increasing modulation index. A minimum THD of 35.32% and 47.78% is obtained at non-adjacent line-to-line voltage and phase voltage respectively. Fig. 12 shows the variation of THD and fundamental voltage for different modulation index is 0.2 to 0.85.

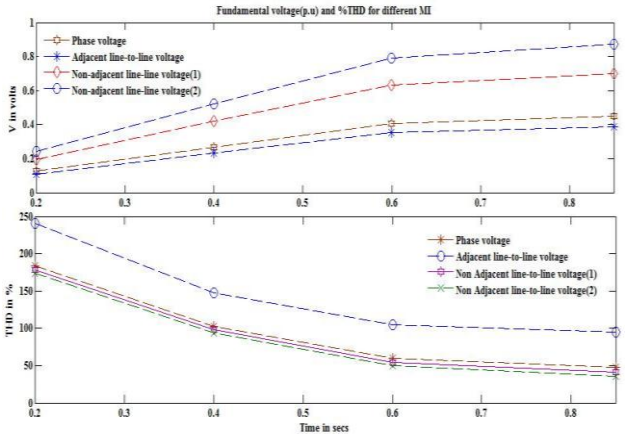


Figure 12. Fundamental voltage and THD for different MI

TABLE II. INCREASE IN FUNDAMENTAL VOLTAGE AND REDUCED THD FOR DIFFERENT MI

Sl.no	MI	Vp (Phase voltage)		V_L (Adjacent line voltage)		V_L (Non-adjacent line voltage of a to c)		V_L (Non-adjacent line voltage of a to d)	
		rms(p.u)	THD in %	rms(p.u)	THD in %	rms(p.u)	THD in %	rms(p.u)	THD in %
1	0.2	0.1252	183.85	0.1082	241.08	0.1957	178.32	0.1957	175.03
2	0.4	0.268	102.38	0.2324	147.5	0.4188	97.75	0.5218	94.12
3	0.6	0.4053	59.51	0.3517	104.8	0.6339	54	0.7903	49.65
4	0.85	0.4476	47.78	0.3884	94.52	0.6999	40.72	0.8727	35.32

VII. CONCLUSION

This paper presents the FPGA implementation of SVPWM switching technique for seven-phase VSI. From the simulation results the fundamental voltage is marginally high and also the increase in voltage reduces with decreasing modulation index. The non-adjacent line-to-line voltage and phase voltage maximum of 0.8727 rms and 0.4476 rms is achieved for modulation index is 0.85. The THD reduction is observed for increasing modulation index. A minimum THD of 35.32% and 47.78% is obtained at non-adjacent line-to-line voltage and phase voltage respectively. The SVPWM technique is easily implemented in the SPARTAN-3A FPGA processor. Based on the results FPGA can function well with different space vectors.

APPENDIX

PARAMETERS OF THE 7-PHASE VSI

Parameters	Values
DC voltage	*1 p.u*
Fundamental frequency	*50Hz*
Switching frequency	*10KHz*
Modulation index(MI)	*0.2 to 0.85*
Number of phases(n)	*7*

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