The Application of a Nanostructured Material in the Fabrication of a P-I-N Diode Chip

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***Abstract*—This research focuses on the integration of conventional silicon electronics with Nanostructured materials for an improved efficiency in the detection of photons applied in Fibre Optic Communications. The PIN starting material, intrinsic region thickness and packaging technology determines the diode performance. Nanostructured materials are processed using different techniques such as ion beam sputtering, layer-by-layer deposition, Nano Milling/Etching System, spin casting, ion beam deposition etc. This research utilizes the unique effects of the wide range of phenomena offered by Nanostructured materials such as plasmonic enhancement of absorption, ultraviolet light absorption, generation of multiexciton, charge storage in surface and interface traps, and size–based spectral tuning, to improve the functions of the intrinsic region of the P-I-N diode. The traps extend the lifetime of non-circulating carriers thereby increasing gain. The presence of an introduced external electromagnetic field shifts free conduction electrons. Other achieved advantages include a very negligible package parasitic effect, negligible contact resistance, and a package inductance on the order of 0.01nH for the P-I-N diode.**

***Index Terms*—PIN diode, nanostructure, nanoparticles, plasmon resonance, scattering**

I Introduction

In this research the efficiency in the detection of photons using a P-I-N Diode (Positive Intrinsic Negative Diode) applied in Fibre Optics Communication has been enhanced by integration of the conventional silicon electronics with Nanostructured materials as shown in Fig. 2.

Basically, when a P-I-N diode is in the forward bias mode, holes and electrons are injected from the P and N regions into the intrinsic region. These charges do not recombine immediately due to the width of the intrinsic region. Consequently, a finite quantity of charge always remains stored and leads to a lowering of the resistivity of the intrinsic region. Also, the quantity of the stored charge Q, depends on the recombination time, and the forward bias current I_F described in the equation:

$$Q\ (\text{Coulombs}) = I_F \tag{1}$$

The resistance of the intrinsic region under forward bias R_S is described in the equation:

$$R_S\ (\text{Ohms}) = \frac{W^2}{(\mu_N+\mu_P)Q} \tag{2}$$

where W is the intrinsic region width μ_N is electron mobility, and μ_P is hole mobility as shown in Fig. 1 below.

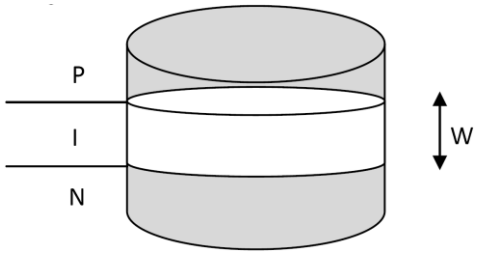

Figure 1. P-I-N chip outline

This research utilizes the unique effects of the wide range of phenomena offered by Nanostructured materials such as plasmonic enhancement of absorption, ultraviolet light absorption, generation of multiexciton, charge storage in surface and interface traps, and size – based spectral tuning, to improve the functions of the intrinsic region of the P-I-N diode [1], [2], [3], [4].

II Material Structure and Layout Design

A. Nanotechnology

Nano-silica particles are divided into two categories with reference to their structure namely the Porous particles or P-type and the Spherical particles or the S-type. The p-type nano-silica is characterized by a number of nano porous with the pore rate of 0.611ml/g. However the P-type ultraviolet reflectivity is >85% while the S-type is >75%. Silicon Oxide Nanoparticles ranges between 15-20nm with a white colour. Gold nanoparticles have unique optical properties which makes it suitable for photosensitive detectors [5], [6], [7]. Gold nanoparticles support surface plasmons. Through ionic interaction, nanoparticles were integrated into a silicon substrate. The characterization of the nanoparticles can be achieved through various techniques such as Transmission Electron Microscopy (TEM), Zeta potential, Dynamic Light Scattering (DLS), Solution pH, and Ultra Violet Visible Spectroscopy.

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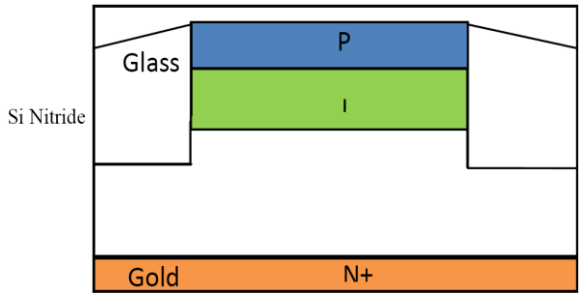

Figure 2. P-I-N chip technology

The epitaxial layer fabricated by Molecular BeamEpitaxi has been used in this study. The Responsivity of a photodetector related the electric current I_p flowing in the device circuit to the optical power P incident on it is described by:

$$Ip = \eta e\Phi = \eta eP/\hbar\nu \equiv RP \quad (3)$$

where η = quantum efficiency; $\hbar$ = planks constant; ν = frequency of the photon; and Φ = mean photon flux.

The photoresponse of a photodiode results from the photogeneration of electron hole pairs through band to band optical absorption. The threshold photon energy of a semiconductor photodiode is the bandgap energy (e.g.) of its active region. The photogenerated electrons and holes in the depletion layer are subject to the local electric field within the layer. The electron/hole carriers drift in opposite directions. This transport process induces an electric current in the external circuit [8] as shown in Fig. 3.

B. Surface Plasmon Resonance

Generally, surface plasmons refer to various waves that propagate along the surface of a conductor. Actually, by altering the structure of a metal's surface, the properties of surface plasmons with respect to their interaction with light can be modified to achieve the desired results [9], [10]. It is therefore possible to achieve light trapping and avalanche multiplication through forming a wavelength - scale texture on the substrate and then depositing nanoparticles to generate large even photocurrent [11], [12], [13]. One way of achieving greater light absorption is the use of scattering from noble metal nanoparticles excited at their surface Plasmon resonance. The foundation of this process is based on the principles that Raman scattering can be increased by orders of magnitude through the use of metal nanostructures [14], [15], [16]. It has been demonstrated that an enhancement in the photocurrent of a factor of 20 could be achieved for a 170nm thick silicon-on-insulator photo-detector at a wavelength of 850nm using silver nanoparticles on the surface device [17]. Also, the use of gold nanoparticles achieved enhancement of 80% at wavelength of 60nm [18].

The tunable photo-physical attributes of metal nano-particles can be illustrated with a point dipole model describing the absorption and scattering of light as follows:

$$C_{scattering} = \frac{1}{6\pi}\left(\frac{2\pi}{\lambda}\right)^4 |\alpha|^2 \quad (4)$$

$$C_{absorption} = \frac{2\pi}{\lambda} I_m \quad [\alpha] \quad (5)$$

where α is the polarizability of the particle given by:

$$\alpha = 3V\left[\frac{\epsilon_p/\epsilon_m - 1}{\epsilon_p/\epsilon_m + 2}\right] \quad (6)$$

where V = particle volume
ϵ_m = dielectric formation of the embedded medium.
ϵ_p = dielectric function of the particle

However, at the point when the particle polarizability will be very large is referred to as Surface Plasmon Resonance, given by:

$$\epsilon_p = -2\epsilon_m \quad (7)$$

Consequently, smaller nanoparticles offer light absorption without any scattering losses, whereas larger nanoparticles offer strong light scattering along with absorption. Au nanoparticles offer the desired properties. As gold is a non-magnetic metal, the surface Plasmon wave is polarized as a result of its electromagnetic surface propagation phenomenon. So this condition will create an enhanced evanescent wave with electric field components in all spatial orientation. Surface Plasmon Resonance occurs when the wave vector for the phonon and Plasmon are equal in magnitude and direction for the same frequency of the transmitted waves [19]. Actually, the wave vector and energy match induces a resonant absorption of energy through the light evanescent wave field causing a Plasmon excitation to Surface Plasmon Resonance [20], [21], [22], [23], [24].

The following conditions guided the geometry of the chip: Increasing the width of the depletion layer (where the generated carriers can be transported by drift) increases the area available for capturing light. Increasing the width of the depletion layer reduces the junction capacitance and also the Resistor Capacitance (RC) time constant. However, the transit time increases with the width of the depletion layer. Reducing the ratio between the diffusion length and the drift length of the device results in a greater proportion of the generated current being carried by the faster drift process [25][26][27], [28][29][30]. Consequently, for an optical signal that has a wavelength λ_s in the range $\lambda_{th}>\lambda_s>\lambda_c$, the quantum efficiency and the Responsivity can be optimized. The Responsivity is linearly proportional to both the quantum efficiency η and the free – space wavelength λ. So, for $\eta = 1$, $\lambda = 1.24\mu m$, R = 1A/W.

Furthermore, the photoluminescence intensity of Au nanoparticles were also sampled as shown in Fig. 4 and Fig. 5, and observed that the large photoluminescence enhancement is due to the localized enhancement of semiconductor optical absorption through the excitation of surface Plasmon resonances in proximate metal nanoparticles [31][32][33][34][35][36]. The desired improved transmission of electromagnetic radiation is as a result of the forward scattering of surface Plasmon

polariton modes of Au nanoparticles of 50-100nm [37], [38][39][40].

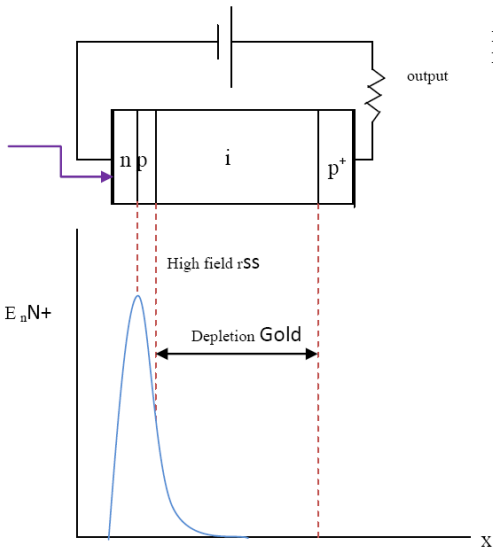

Figure 3. Enhanced absorption of photons at the intrinsic region leading to a more efficient generation of photocurrent.

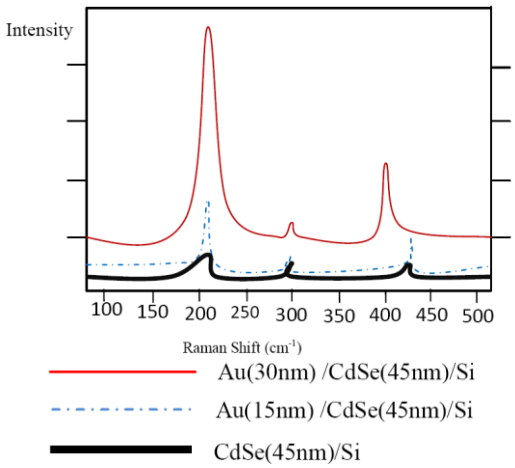

Figure 4. Effect of raman shift showing Au nanoparticles with strong surface enhanced Raman intensity at 30nm.

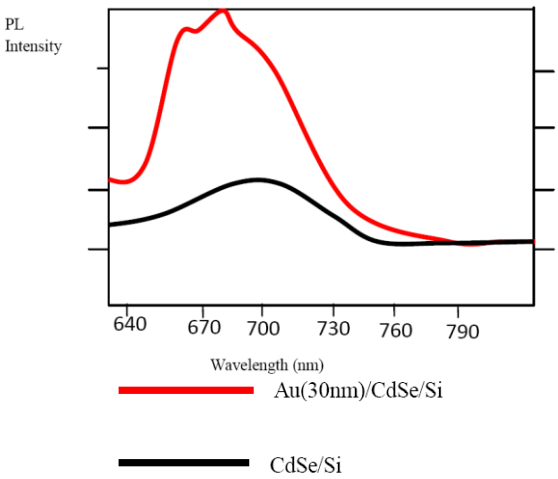

Figure 5. Illustrating the photoluminescence spectra of the nanoparticles on silicon embedded medium at room temperature.

III Fabrication

As described in Fig. 6, the Ohmic contact layers are produced with Pd/AuGe/Au with dimensions 25nm/55nm/80nm respectively.

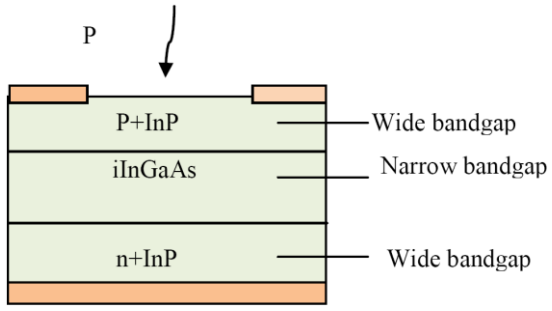

Figure 6. P-I-N Chip heterojunction fabrication

Electron Beam technique was applied in the deposition of Pd and Au metals while AuGe were deposited by thermal evaporation process.

IV Results

Resistance of the PIN diode versus DC current is shown in Fig. 7.

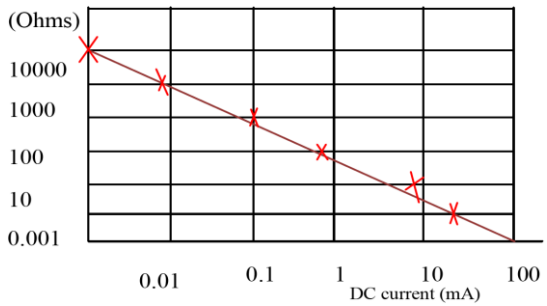

Figure 7. Resistance of a PIN diode versus DC current

The properties of the fabricated P-I-N Diode chip are described in Table I below.

TABLE I. The Properties of the Fabricated PIN Diode Chip.

Spectral response	700 – 2000nm
Peak response	0.55 A/W @ 1200nm
Rise/fall time	0.01 ns
Diode capacitance	0.2 pF (typ)
NEP @ 1200 nm	1.0×10^{-15} W/ $\sqrt{Hz}$
Dark current	0.5nA (typ) 1.0nA (max)
PD Active diameter	0.1 mm
Bandwidth	1 GHz (min)
Damage threshold	100 mW CW
Bias (reverse)	12V battery
Coupling lens	0.8”Diameter ball lens
Coupling efficiency	98% (typ) from both single and multi modefibres over full spectral response.

It was observed that the nanoparticles created traps that extended the lifetime of non-circulating carriers which increased the total gain and thus the efficiency of the PIN diode chip. Also, fractal aggregates of metallic nanoparticles under localized surface Plasmon induces

higher enhancement of local field amplitudes compared to single particles.

V CONCLUSION

The application of nanostructured material in the fabrication of a P-I-N Diode apart from increasing gain also achieved the reduction in parasitic effects of resistance and inductance by 95%.

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