A Highly-Integrated Low-Power 10Gbps OOK Receiver for mm-Wave Short-Haul Wireless Link in CMOS 28nm

Junlei Zhao, Kambiz Hadipour, Andrea Ghilioni, Matteo Bassi, Andrea Mazzanti, and Francesco Svelto
University of Pavia, Pavia, Italy
Email: {junlei.zhao, kambiz.hadipourabkenar, andrea.ghilioni, matteo.bassi, andrea.mazzanti, francesco.svelto}@unipv.it

Abstract—This paper presents a 50GHz wireless receiver for 10Gbps on-off keying (OOK) modulated signals designed in 28nm CMOS. An in-depth analysis indicates that the energy detector has a substantial impact on the receiver performance and should be properly taken into account in the link budget. The work covers the design of a novel 50GHz broadband low noise amplifier and its co-design with envelope detector and limiting amplifier. The extracted simulation results show that the receiver is able to detect a 10Gbps signal at 10cm distance with a BER of $10^{-12}$ while consuming only 70mW from 1V power supply.

Index Terms—receiver, OOK, mm-wave, envelope detector, Limiting amplifier, CMOS

I. INTRODUCTION

The complexity of electronic systems is increasing continuously. The amount of data elaborated grows on daily basis, while the trend of distributed and high-performance computing is leading to the development of new systems with demanding requirements. Multi-core/multi-node computers necessitate a huge number of short-range I/O interfaces with tens of Gbps bandwidth capability. However, wired connections such as backplanes have limited bandwidth, heavily limiting the mechanical design flexibility and raising the costs of materials and assembly. In this context, the concept of a wireless chip-to-chip connection becomes very attractive, promising high flexibility and versatility [1].

The mm-wave frequency range, nominally located between 30GHz and 300GHz is of great interest in this framework [2]-[3]. The spectrum is very broad and still unpopulated, allowing allocating bandwidths several GHz wide, leading to multi-Gbps communication speed even with very simple modulation techniques [4]-[6]. Moreover, with a wavelength of less than 10mm, the size of the antenna turns out to be very compact, fitting into the IC package or the chassis of small devices, allowing miniaturization with respect to current wired solutions [7].

Though mostly oriented to digital applications, deep sub-micron silicon CMOS technology lends itself to implementing analog functions at high frequencies: for each step of minimum gate length reduction, a corresponding increase in $f_T$ is achieved, being in excess of 450GHz for 28nm [8]. The System on Chip (SoC) approach for an entire analog transceiver in the mm-wave range becomes thus very attractive.

In this paper we address the realization of the signal detection into a wireless On-Off Keying (OOK) receiver for 10Gbps communications with 50GHz carrier frequency. Section II describes the architecture of the receiver and the link budget analysis, while section III details the main building blocks. Section IV describes simulation results, and conclusions follow.

II. ARCHITECTURE AND LINK BUDGET

The complete architecture of the receiver is shown in Fig. 1. The 50GHz OOK-modulated signal is collected by the off-chip patch antenna and delivered to the single-ended Low-Noise Amplifier (LNA). Bondwires in a ground-signal-ground (GSG) configuration are employed to connect the antenna to the LNA input, allowing covering distances of several mm with negligible signal loss. The output of the LNA is fed to the Envelope Detector (ED), which performs power detection. Since the structure of the ED requires a differential input, an on-chip balun has been interposed to properly convert the single-ended output signal of the LNA. A dummy ED is connected to the second input of the Limiting Amplifier (LA) to improve the power-supply rejection ratio (PSRR). The LA amplifies the detected signal and drives the off-chip measurement instrumentation through the output buffer.

![Figure 1. Receiver architecture.](image-url)

The proposed OOK system is based on energy detection, which makes the front-end non-linear. As a
consequence, Friis formula does not apply and the computation of the link budget is not straightforward [9]. The equivalent model of the receiver in Fig. 2, consisting of the cascade of LNA and energy detector, is used to calculate the overall receiver equivalent noise figure \( F_{\text{RX}} \).

\[
\text{SNR}_{\text{in}} = \frac{E\left[ s_{\text{in}}^2 \right]}{E\left[ n_{\text{in}}^2 \right]} = \frac{E_a B_0}{N_0 B} \frac{P_{\text{in}}}{P_{\text{RX}}} \tag{1}
\]

where \( E\left[ \cdot \right] \) denotes the expected value, \( E_a \) the energy of the bit, \( B_0 \) the bit rate, \( N_0 \) the power spectral density of the channel noise and \( B \) the signal bandwidth. Accordingly, the output SNR can be calculated as:

\[
\text{SNR}_{\text{out}} = \frac{E\left[ s_{\text{out}}^2 \right]}{E\left[ n_{\text{out}}^2 \right]} = \frac{E\left[ G_{\text{LNA}} G_{\text{RX}} a_2^2 (2 n_0 + n_{\text{amp}}) + (n_0 + n_{\text{amp}}) + n_{\text{int}} \right]}{E\left[ (a_2 G_{\text{LNA}} a_2) \right]} \tag{2}
\]

Expanding (2) and solving for \( \text{SNR}_{\text{out}} \) at the output, the equivalent receiver noise figure \( F_{\text{RX}} \) is:

\[
F_{\text{RX}} = 4F_{\text{LNA}} \left( 1 + \frac{3F_{\text{LNA}}}{4\text{SNR}_{\text{in}}} + \frac{\sigma_{\text{int}}^2}{4P_{\text{RX}}G_{\text{LNA}}^2 P_{\text{LNA}}} \right) \tag{3}
\]

where \( F_{\text{LNA}} \) is the noise figure of the LNA. Two important insights can be pointed out. First, even if the receiver is completely noisless, the SNR degrades by 6dB. Second, unlike the common linear case, the equivalent receiver noise figure \( F_{\text{RX}} \) depends not only on the gain and noise figure of its blocks, but also on the input SNR. This is due to the squaring action of the energy detector that translates to the output an amount of noise proportional to the power of the input signal (see Eq. 3).

In short-range chip-to-chip communications, the typical distance to be covered is 10cm. Assuming a transmitter output power of 10dBm, reasonable at 50GHz, the signal power at the input of the receiver is -34dBm. Taking into account 4dB link margin, this translates to a minimum SNR of 33dB at the input of the receiver. Since at least 17dB of SNR is required to demodulate an OOK signal with BER<10\(^{-12}\), the overall receiver noise figure cannot exceed 16dB. The requirement further tightens to 10dB after taking into account the squaring action of the energy detector. Assuming a maximum LNA noise figure of 10dB, the LNA gain needs to be at least 25dB over the receiver bandwidth to properly suppress the aggregated noise of the squarer and following stages, estimated to be \( \sigma_{\text{int}}^2=500\text{nV}^2 \) by simulation.

![Communication distance at 10Gbps as a function of LNA gain assuming 10dBm transmitted power, 10dB LNA noise figure, \( \sigma_{\text{int}}=500\text{nV}^2 \), a-1 and 4dB link margin.](image)

Fig. 3 shows the communication distance against the LNA gain. As it can be seen, due to the energy detector action, the LNA is required to realize a gain greater than 25dB, while keeping a noise figure around 10dB. Targeting these specs over a 20GHz bandwidth around 50GHz is challenging. At higher LNA gain, only the LNA noise figure and energy detector SNR degradation limit the link performance. In this context, recognizing the detrimental effect of the energy detector on the degradation of the receiver SNR is paramount for a correct link budget and transceiver operation.

### III. BUILDING BLOCKS

#### A. LNA

Six common source stages two by two stacked in a current re-used architecture construct the LNA core. Cascaded stages result in large gain while the current re-use leads to low power consumption. To enable 10Gbps communication, in addition to the large gain, a wide operating bandwidth of 20GHz is also required. Third order inter-stage networks are employed between the amplifying stages to achieve a larger bandwidth. The frequency responses of the inter-stage matching networks are stagger tuned to further extend the overall LNA bandwidth.

To convert the signal from the S. E. output of the LNA to the differential input of the ED, a balun is required. To correctly operate, the impedance of the two coils should be much greater than the load impedance (i.e. the one of the gates of the ED in this case), and the coupling factor \( k \) should be as close as possible to 1. However, the electrical characteristics of the two topmost thick-copper layers available in the back-end of the employed CMOS 28nm technology allow a \( k \) within 0.8-0.9, while the maximum value achievable for the inductances to keep their self-resonance frequency well above the 50GHz of the carrier, is lower than 200\( \mu \)H. Based on these stringent design constraints, the two octagonal single-turn 150\( \mu \)H coils...
where designed to show a k of 0.82 and a self-resonance frequency of 85GHz. The resulting 6dB loss of the balun needs to be taken into account by the minimum gain requirement of the LNA. The balun is very compact, occupying 95x95μm² only.

B. Envelope Detector

Envelope detector circuits are mainly based on exploiting the 2nd order non-linearity of the MOSFET operating in saturation to produce an output signal proportional to the square of the input. Due to the stringent receiver noise requirements, ED gain is a critical parameter to maintain high SNR signal and relax the gain of the LA, drastically reducing the overall power consumption [10].

Fig. 4 (a) shows the source-follower based ED, where the push-push connection of the pair also nulls the 1st order component of the output signal. The main drawback of this circuit is the limited gain [11]. To increase the gain, an improved version of the one proposed in [12] is presented in Fig. 4 (b). The proposed ED combines rectification with amplification by means of a class-AB biasing of the NMOS input pair. A tunable PMOS in triode is employed as a load to accommodate different input amplitudes. A cascode transistor has been inserted between the push-push pair and the load in order to improve the output resistance and thus maximize the achievable gain. The output amplitude of the source-follower based ED $A_{out,sf}$ and the proposed one $A_{out,AB}$ are:

$$A_{out,sf} \approx \frac{1}{16} \frac{1}{V_{ov}} A^2_m$$  \hspace{1cm} (4)

$$A_{out,AB} \approx \frac{1}{8} \frac{g_m R_L}{V_{ov}} A^2_m$$  \hspace{1cm} (5)

where $g_m$ is the MOS transconductance, $R_L$ the load resistor, $V_{ov}$ the overdrive voltage and $A_m$ the input amplitude. More than 2x improvement in the gain can be achieved, strongly preventing the reduction of the SNR due to the nonlinear energy detection of the ED.

C. Limiting Amplifier

The LA core consists of the cascade of five differential stages closed in a DC offset cancelation loop. The output buffer drives the measurement setup. The LA core stages are realized with differential pairs with cross-coupled capacitances for bandwidth extension. No inductive peaking has been employed to minimize the area occupancy.

The cascade of $n$ identical gain cells, each one having a bandwidth $BW_c$, exhibits an overall bandwidth of

$$BW_{tot} = BW_c \sqrt{2^{1/n} - 1}$$  \hspace{1cm} (6)

where $m$ is equal to 2 for first-order stages and 4 for second order stages [13]. In our case, the network is first order and thus $m$ is 2. For a certain gain $A_{tot}$ required for the multistage amplifier over the bandwidth $BW_{tot}$, the minimum gain-bandwidth product $GBW_c$ of the single stage is required to be [14]:

$$GBW_c = \frac{BW_{tot}}{A^{1/m}_{tot} \sqrt{2^{1/n} - 1}}$$  \hspace{1cm} (7)

The main lobe of the baseband 10Gbps OOK spectrum occupies a bandwidth of 10GHz. Since the best compromise between SNR and Inter-Symbol Interference (ISI) contribution is achieved for a receiver bandwidth around 0.7 times the one of the signal, the targeted $BW_{tot}$ is 7GHz. Given the required SNR at the output and the expected integrated noise, a minimum amplitude of 400mV is needed, requiring a minimum gain $A_{tot}$ of 36dB for the LA. From (7), the best design compromise is achieved with 5 stages each one delivering 7.2dB gain and 18.2GHz bandwidth, still challenging to achieve in the 28nm technology node, especially at large signal. Note that in this calculation, the buffer has been neglected since the 60fF parasitic capacitance of the output pad together with the 50Ω resistance of the BERT leads to a bandwidth of more than 50GHz for the last stage itself. Since the fourth stage is already working in large signal regime even under the minimum input signal expected, the fifth core stage has then been changed into a f<sub>T</sub>-doubler architecture to taper through the buffer avoiding losses in bandwidth [14]. The schematics of a single LA stage and buffer are shown in Fig. 5.

![Figure 4](image1)

Figure 4. Source follower based envelope detector (a) proposed envelope detector (b).

![Figure 5](image2)

Figure 5. Schematic of the LA stage (a) and the output buffer (b).

The targeted signal amplitude of 400mV S.E. requires 8mA to be delivered by the last stage into the 50Ω
impedance of the Bit Error-Rate Tester (BERT). To minimize the input capacitance required to drive such current, a f4-doubler stage has been employed. An open drain configuration has been selected to avoid current partition with the load resistances of the stage, thus minimizing the size of the buffer for the given output swing. Two off-chip bias tees bias the stage.

The offset cancelation loop employs a similar differential pair as the core stages. The offset is sensed at the input of the buffer rather than the output, since this one is open drain and thus its DC gain is equal to zero. The feedback is closed at the output of the first LA stage in order not to place the 350Ω load resistance of the pair directly in parallel with the load of the ED, which would seriously degrade its gain. The pole of the loop-filter has been set to 450kHz, low enough to avoid significant eye closure due to the drop of longest expected run.

IV. SIMULATION RESULTS

To verify the performances of the proposed architecture, post-layout simulations were performed using Cadence SpectreRF. The overall receiver power consumption is 70mW from 1V Vdd: 30mW for the LNA and 40mW for the envelope detector and limiting amplifier. The chip area is 1450x800μm² including pads.

The simulated conversion gain (S21), input reflection coefficient (S11), and noise figure (NF) of the LNA are shown in Fig. 6. The LNA achieves a gain of 26dB over a bandwidth of more than 28GHz. The S11 is better than -10dB across the 45-65GHz bandwidth. The NF is less than 6.8dB across the whole operating band.

![LNA simulated conversion gain (S21), input reflection coefficient (S11) and noise figure (NF).](image)

To assess the link performance, a 10Gbps PRBS32 bitstream modulated by a 50GHz carrier was fed into the balun with a transient noise simulation. The amplitude of the input signal was set to -38dBm, i.e. the expected value at the input of the LNA when the receiver is placed at a distance of ~10cm from the transmitter with 4dB link margin. The single-ended eye diagram at the output of the LA is depicted in Fig. 7. An SNR better than 17dB was simulated, consistent with a simulated BER<10⁻¹².

In Table I, the performance of the receiver is compared to the state of the art, assuming 100mW Pdiss of the TX. The proposed work shows the highest combination of datarate and communication distance employing non-directive antenna while still keeping low power consumption.

### V. CONCLUSION

A short-range mm-wave 50GHz wireless OOK receiver for 10Gbps communication has been presented. The receiver was realized in 28nm CMOS technology and it consumes 70mW from 1V power supply when effectively demodulating a 10Gbps signal at 10cm distance with a BER of 10⁻¹².

![Simulated single-ended eye diagram with noise, corresponding to a communication distance of 10cm.](image)

<table>
<thead>
<tr>
<th>Datarate (Gbps)</th>
<th>Distance (mm)</th>
<th>Gain (dB)</th>
<th>f_carrier (GHz)</th>
<th>Pdiss (mW)</th>
<th>Tech</th>
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<td>60</td>
<td>308</td>
</tr>
<tr>
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<td>1000</td>
<td>6.5</td>
<td>60</td>
<td>1772</td>
</tr>
<tr>
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<td>60</td>
<td>286</td>
</tr>
<tr>
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<td>327</td>
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<td>25</td>
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<td>4.0</td>
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</tr>
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</table>

This Work     | 10           | 100      | 3.0             | 50        | 170  |
|               |              |          |                 | 28n       |      |

### REFERENCES

Junlei Zhao was born in Yichang, China, in 1986. He received the B.S. and M.S. degrees in Electronics Engineering in 2008 and 2011, respectively, both from Peking University, Beijing, China. During his Master degree thesis, he studied high-speed digital to Analog Converter. Since 2011, he works toward the Ph.D. degree in Microelectronics. His research interests include RF and mm-wave IC design, with particular focus on local power transceiver for high-speed short-range wireless communication.

Kambiz Hadipour was born in Tehran, Iran, in 1984. He received the bachelor degree in Electrical Engineering from Zanjan University, Zanjan, Iran in 2006. In 2010, he received the master degree with honor from Tarbiat Modares University, Tehran, Iran. He is currently working towards the Ph.D degree in Microelectronics at University of Pavia. His major research interests include RF and mm-wave IC design, with advanced CMOS technologies. From 2007, he has been a member of IEEE and IEEE Solid State Circuits Society. From 2011 he has become a member of IEEE Communication Society.

Andrea Ghilioni was born in Pavia, Italy, in 1984. He received from the University of Pavia, Italy, the B.S. and M.S. degrees with honors in Electronics Engineering in 2006 and 2008 respectively and the Ph.D. degree in Microelectronics in January 2012, with Professor Francesco Svelto as Advisor. His current research interests cover RF/microwave and mm-wave IC design in scaled CMOS technologies, focused on low-power transceivers for multi-Gbps wireless communications. From 2010 he has been a member of IEEE and IEEE Solid State Circuits Society.

Matteo Bassi was born in Padova, Italy, in 1985. He received the B.S., M.S. (Summa cum Laude) and Ph.D. degrees in Electronics Engineering from the University of Padova, Italy, in 2007, 2009 and 2013, respectively. In 2008 and 2009 he was an EAP student at the University of California, San Diego. In 2012 he was a visiting Ph.D. student at the Analog Integrated Circuits Laboratory, University of Pavia, Italy. Since 2013 he is Assistant Professor at the University of Pavia, Italy. His main research interests are in the field of RF integrated circuits. He co-developed and realized the first CMOS integrated high-resolution radar transceiver front-end for breast cancer detection. Presently, he is working on mm-wave systems and high-speed serial interfaces. He is recipient of the IEEE Microwave Theory and Techniques Society Graduate Fellowship for Medical Applications 2012.

Andrea Mazzanti was born in Modena (ITALY) in 1976. He received the Laurea and Ph.D. degrees in Electrical Engineering from the Università di Modena, ITALY in 2001 and 2005 respectively. During the summer of 2003, he was with Agere Systems, Allentown, PA as an Intern. In 2005, he obtained a Post-Doctoral position with the Università di Pavia, Pavia, Italy, during which time he was involved with CMOS RFICs for cell-phone applications. From 2006 to 2009, he was an Assistant Professor with the Università di Modena and Reggio Emilia, where he taught a course on advanced analog IC design. In January 2010, he joined the Università di Pavia. He has authored over 50 technical papers. His main research interests cover device modeling and IC design for high-speed communications and millimeter-wave systems. Dr. Mazzanti has been a member of the Technical Program Committee of the IEEE Custom Integrated Circuit Conference (CICC) and the IEEE International Conference on IC Design and Technology (ICICDT) since 2008.

Francesco Svelto received the Laurea and Ph.D. degrees in electrical engineering from Università di Pavia, Italy, in 1991 and 1995, respectively. In 1997, he became an Assistant Professor with the Università di Bergamo, Italy. Since 2006, he has been the Director of a joint scientific laboratory (between the Università di Pavia and STMicroelectronics), dedicated to research in microelectronics with an emphasis on millimeter-wave systems for wireless communications, high-speed serial links, and read-write channels for hard disk drives. The laboratory hosts roughly 40 engineers equally divided between ST employees, Ph.D. students, and professors. Dr. Svelto is member of the technical program committee of the International Solid State Circuits Conference and has been a member of Custom Integrated Circuits Conference, Bipolar/ BiCMOS Circuits Technology Meeting and European Solid State Circuits Conference. He served as Associate Editor of IEEE Journal of Solid State Circuits (2003-2007), and as Guest Editor for a special issue on the same journal in March 2003. He is co-recipient of the IEEE Journal of Solid State Circuits 2003 Best Paper Award, and he has been elevated IEEE Fellow in 2013.