A Highly-Integrated Low-Power 10Gbps OOK Receiver for mm-Wave Short-Haul Wireless Link in CMOS 28nm

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Abstract—This paper presents a 50GHz wireless receiver for 10Gbps on-off keying (OOK) modulated signals designed in 28nm CMOS. An in-depth analysis indicates that the energy detector has a substantial impact on the receiver performance and should be properly taken into account in the link budget. The work covers the design of a novel 50GHz broadband low noise amplifier and its co-design with envelope detector and limiting amplifier. The extracted simulation results show that the receiver is able to detect a 10Gbps signal at 10cm distance with a BER of 10^{-12} while consuming only 70mW from 1V power supply.

Index Terms—receiver, OOK, mm-wave, envelope detector, Limiting amplifier, CMOS

I. INTRODUCTION

The complexity of electronic systems is increasing continuously. The amount of data elaborated grows on daily basis, while the trend of distributed and high-performance computing is leading to the development of new systems with demanding requirements. Multi-core/multi-node computers necessitate a huge number of short-range I/O interfaces with tens of Gbps bandwidth capability. However, wired connections such as backplanes have limited bandwidth, heavily limiting the mechanical design flexibility and raising the costs of materials and assembly. In this context, the concept of a wireless chip-to-chip connection becomes very attractive, promising high flexibility and versatility [1].

The mm-wave frequency range, nominally located between 30GHz and 300GHz is of great interest in this framework [2]-[3]. The spectrum is very broad and still unpopulated, allowing allocating bandwidths several GHz wide, leading to multi-Gbps communication speed even with very simple modulation techniques [4]-[6]. Moreover, with a wavelength of less than 10mm, the size of the antenna turns out to be very compact, fitting into the IC package or the chassis of small devices, allowing miniaturization with respect to current wired solutions [7].

Though mostly oriented to digital applications, deep sub-micron silicon CMOS technology lends itself to implementing analog functions at high frequencies: for

each step of minimum gate length reduction, a corresponding increase in f_T is achieved, being in excess of 450GHz for 28nm [8]. The System on Chip (SoC) approach for an entire analog transceiver in the mm-wave range becomes thus very attractive.

In this paper we address the realization of the signal detection into a wireless On-Off Keying (OOK) receiver for 10Gbps communications with 50GHz carrier frequency. Section II describes the architecture of the receiver and the link budget analysis, while section III details the main building blocks. Section IV describes simulation results, and conclusions follow.

II. ARCHITECTURE AND LINK BUDGET

The complete architecture of the receiver is shown in Fig. 1. The 50GHz OOK-modulated signal is collected by the off-chip patch antenna and delivered to the single-ended Low-Noise Amplifier (LNA). Bondwires in a ground-signal-ground (GSG) configuration are employed to connect the antenna to the LNA input, allowing covering distances of several mm with negligible signal loss. The output of the LNA is fed to the Envelope Detector (ED), which performs power detection. Since the structure of the ED requires a differential input, an on-chip balun has been interposed to properly convert the single-ended output signal of the LNA. A dummy ED is connected to the second input of the Limiting Amplifier (LA) to improve the power-supply rejection ratio (PSRR). The LA amplifies the detected signal and drives the off-chip measurement instrumentation through the output buffer.
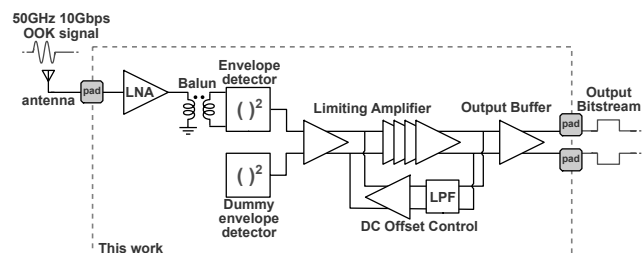

Figure 1. Receiver architecture.

The proposed OOK system is based on energy detection, which makes the front-end non-linear. As a

consequence, Friis formula does not apply and the computation of the link budget is not straightforward [9]. The equivalent model of the receiver in Fig. 2, consisting of the cascade of LNA and energy detector, is used to calculate the overall receiver equivalent noise figure F_{RX}.
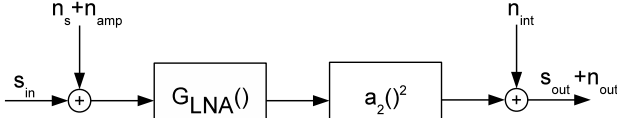

Figure 2.   Equivalent model of the receiver with noise sources.

In this model, s_{in} is the desired input signal, n_s the channel noise, n_{amp} the input-referred LNA noise and n_{int} the aggregated noise of the envelope detector and following stages, while G_{LNA} and a_2 are the LNA gain and squarer gain, respectively.

The input signal-to-noise ratio (SNR) is given by:

$$SNR_{in} = \frac{E[s_{in}^2]}{E[n_s^2]} = \frac{E_b B_r}{N_0 B} = \frac{P_b}{P_{N0}} \quad (1)$$

where $E[\bullet]$ denotes the expected value, E_b the energy of the bit, B_r the bit rate, N_0 the power spectral density of the channel noise and B the signal bandwidth. Accordingly, the output SNR can be calculated as:

$$
\begin{aligned}
SNR_{out} &= \frac{E[s_{out}^2]}{E[n_{out}^2]} \\
&= \frac{E[(a_2(G_{LNA}s_{in})^2)^2]}{E[(a_2 G_{LNA}^2(2s_{in}(n_s + n_{amp}) + (n_s + n_{amp})^2) + n_{int})^2]}
\end{aligned} \quad (2)
$$

Expanding (2) and solving for SNR at the output, the equivalent receiver noise figure F_{RX} is:

$$F_{RX} = 4F_{LNA}\left(1 + \frac{3F_{LNA}}{4SNR_{in}} + \frac{\sigma_{n_{int}}^2}{4P_{N0}a_2^2 G_{LNA}^4 P_b F_{LNA}}\right) \quad (3)$$

where F_{LNA} is the noise figure of the LNA. Two important insights can be pointed out. First, even if the receiver is completely noiseless, the SNR degrades by 6dB. Second, unlike the common linear case, the equivalent receiver noise figure F_{RX} depends not only on the gain and noise figure of its blocks, but also on the input SNR. This is due to the squaring action of the energy detector that translates to the output an amount of noise proportional to the power of the input signal (see Eq. 3).

In short-range chip-to-chip communications, the typical distance to be covered is 10cm. Assuming a transmitter output power of 10dBm, reasonable at 50GHz, the signal power at the input of the receiver is -34dBm. Taking into account 4dB link margin, this translates to a minimum SNR of 33dB at the input of the receiver. Since at least 17dB of SNR is required to demodulate an OOK signal with BER<10^{-12}, the overall receiver noise figure cannot exceed 16dB. The requirement further tightens to 10dB after taking into account the squaring action of the energy detector. Assuming a maximum LNA noise figure

of 10dB, the LNA gain needs to be at least 25dB over the receiver bandwidth to properly suppress the aggregated noise of the squarer and following stages, estimated to be σ_{nint}^2=500nV^2 by simulation.
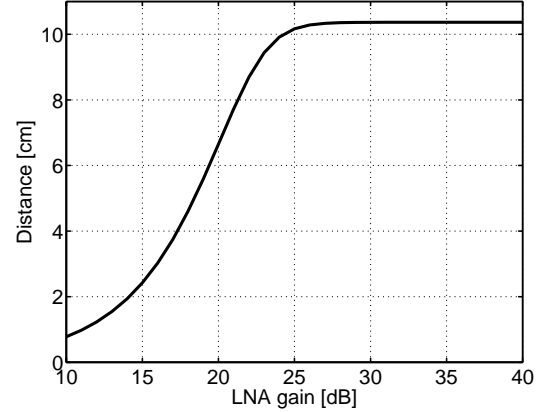

Figure 3.   Communication distance at 10Gbps as a function of LNA gain assuming 10dBm transmitted power, 10dB LNA noise figure, σ_{nint}^2=500nV^2, a_2=1 and 4dB link margin.

Fig. 3 shows the communication distance against the LNA gain. As it can be seen, due to the energy detector action, the LNA is required to realize a gain greater than 25dB, while keeping a noise figure around 10dB. Targeting these specs over a 20GHz bandwidth around 50GHz is challenging. At higher LNA gain, only the LNA noise figure and energy detector SNR degradation limit the link performance. In this context, recognizing the detrimental effect of the energy detector on the degradation of the receiver SNR is paramount for a correct link budget and transceiver operation.

III.   BUILDING BLOCKS

A.   LNA

Six common source stages two by two stacked in a current re-used architecture construct the LNA core. Cascaded stages result in large gain while the current re-use leads to low power consumption. To enable 10Gbps communication, in addition to the large gain, a wide operating bandwidth of 20GHz is also required. Third order inter-stage networks are employed between the amplifying stages to achieve a larger bandwidth. The frequency responses of the inter-stage matching networks are stagger tuned to further extend the overall LNA bandwidth.

To convert the signal from the S. E. output of the LNA to the differential input of the ED, a balun is required. To correctly operate, the impedance of the two coils should be much greater than the load impedance (i.e. the one of the gates of the ED in this case), and the coupling factor k should as close as possible to 1. However, the electrical characteristics of the two topmost thick-copper layers available in the back-end of the employed CMOS 28nm technology allow a k within 0.8-0.9, while the maximum value achievable for the inductances to keep their self-resonance frequency well above the 50GHz of the carrier, is lower than 200pH. Based on these stringent design constraints, the two octagonal single-turn 150pH coils

where designed to show a k of 0.82 and a self-resonance frequency of 85GHz. The resulting 6dB loss of the balun needs to be taken into account by the minimum gain requirement of the LNA. The balun is very compact, occupying 95x95μm^2 only.

B. Envelope Detector

Envelope detector circuits are mainly based on exploiting the 2nd order non-linearity of the MOSFET operating in saturation to produce an output signal proportional to the square of the input. Due to the stringent receiver noise requirements, ED gain is a critical parameter to maintain high SNR signal and relax the gain of the LA, drastically reducing the overall power consumption [10].

Fig. 4 (a) shows the source-follower based ED, where the push-push connection of the pair also nulls the 1st order component of the output signal. The main drawback of this circuit is the limited gain [11]. To increase the gain, an improved version of the one proposed in [12] is presented in Fig. 4 (b). The proposed ED combines rectification with amplification by means of a class-AB biasing of the NMOS input pair. A tunable PMOS in triode is employed as a load to accommodate different input amplitudes. A cascode transistor has been inserted between the push-push pair and the load in order to improve the output resistance and thus maximize the achievable gain. The output amplitude of the source-follower based ED $A_{out,sf}$ and the proposed one $A_{out,AB}$ are:

$$A_{out,sf} \cong \frac{1}{16}\frac{1}{V_{ov}}A_{in}^2 \qquad (4)$$

$$A_{out,AB} \cong \frac{1}{8}\frac{g_m R_L}{V_{ov}}A_{in}^2 \qquad (5)$$

where g_m is the MOS transconductance, R_L the load resistor, V_{ov} the overdrive voltage and A_{in} the input amplitude. More than 2x improvement in the gain can be achieved, strongly preventing the reduction of the SNR due to the nonlinear energy detection of the ED.
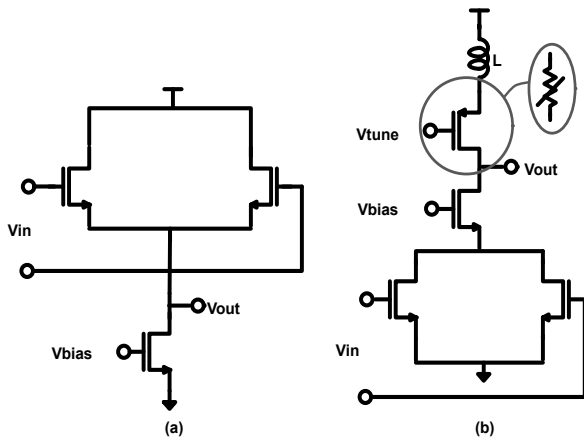
C. Limiting Amplifier

The LA core consists of the cascade of five differential stages closed in a DC offset cancelation loop. The output buffer drives the measurement setup. The LA core stages are realized with differential pairs with cross-coupled capacitances for bandwidth extension. No inductive peaking has been employed to minimize the area occupancy.

The cascade of n identical gain cells, each one having a bandwidth BW_c, exhibits an overall bandwidth of

$$BW_{tot} = BW_c \sqrt[m]{2^{1/n}-1} \qquad (6)$$

where m is equal to 2 for first-order stages and 4 for second order stages [13]. In our case, the network is first order and thus m is 2. For a certain gain A_{tot} required for the multistage amplifier over the bandwidth BW_{tot}, the minimum gain-bandwidth product GBW_c of the single stage is required to be [14]:

$$GBW_c = \frac{GBW_{tot}}{A_{tot}^{1-1/n}\sqrt{2^{1/n}-1}} \qquad (7)$$

The main lobe of the baseband 10Gbps OOK spectrum occupies a bandwidth of 10GHz. Since the best compromise between SNR and Inter-Symbol Interference (ISI) contribution is achieved for a receiver bandwidth around 0.7 times the one of the signal, the targeted BW_{tot} is 7GHz. Given the required SNR at the output and the expected integrated noise, a minimum amplitude of 400mV is needed, requiring a minimum gain A_{tot} of 36dB for the LA. From (7), the best design compromise is achieved with 5 stages each one delivering 7.2dB gain and 18.2GHz bandwidth, still challenging to achieve in the 28nm technology node, especially at large signal. Note that in this calculation, the buffer has been neglected since the 60fF parasitic capacitance of the output pad together with the 50Ω resistance of the BERT leads to a bandwidth of more than 50GHz for the last stage itself. Since the fourth stage is already working in large signal regime even under the minimum input signal expected, the fifth core stage has then been changed into a f_T-doubler architecture to taper through the buffer avoiding losses in bandwidth [14]. The schematics of a single LA stage and buffer are shown in Fig. 5.

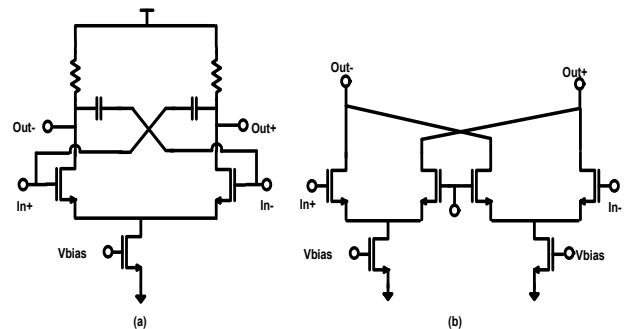Figure 4. Source follower based envelope detector (a) proposed envelope detector (b).

Figure 5. Schematic of the LA stage (a) and the output buffer (b).

The targeted signal amplitude of 400mV S.E. requires 8mA to be delivered by the last stage into the 50Ω

impedance of the Bit Error-Rate Tester (BERT). To minimize the input capacitance required to drive such current, a f_T-doubler stage has been employed. An open drain configuration has been selected to avoid current partition with the load resistances of the stage, thus minimizing the size of the buffer for the given output swing. Two off-chip bias tees bias the stage.

The offset cancelation loop employs a similar differential pair as the core stages. The offset is sensed at the input of the buffer rather than the output, since this one is open drain and thus its DC gain is equal to zero. The feedback is closed at the output of the first LA stage in order not to place the 350Ω load resistance of the pair directly in parallel with the load of the ED, which would seriously degrade its gain. The pole of the loop-filter has been set to 450kHz, low enough to avoid significant eye closure due to the drop of longest expected run.

IV. SIMULATION RESULTS

To verify the performances of the proposed architecture, post-layout simulations were performed using Cadence SpectreRF. The overall receiver power consumption is 70mW from 1V Vdd: 30mW for the LNA and 40mW for the envelope detector and limiting amplifier. The chip area is 1450x800μm^2 including pads.

The simulated conversion gain (S_{21}), input reflection coefficient (S_{11}) and noise figure (NF) of the LNA are shown in Fig. 6. The LNA achieves a gain of 26dB over a bandwidth of more than 28GHz. The S11 is better than -10dB over the 45-65GHz bandwidth. The NF is less than 6.8dB across the whole operating band.
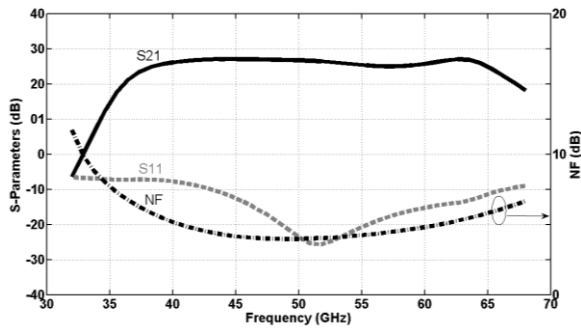

Figure 6.   LNA simulated conversion gain (S21), input reflection coefficient (S11) and noise figure (NF).

To assess the link performance, a 10Gbps PRBS32 bitstream modulated by a 50GHz carrier was fed into the balun with a transient noise simulation. The amplitude of the input signal was set to -38dBm, i.e. the expected value at the input of the LNA when the receiver is placed at a distance of ~10cm from the transmitter with 4dB link margin. The single-ended eye diagram at the output of the LA is depicted in Fig. 7. An SNR better than 17dB was simulated, consistent with a simulated BER<10^{-12}.

In Table I, the performance of the receiver is compared to the state of the art, assuming 100mW Pdiss of the TX. The proposed work shows the highest combination of datarate and communication distance employing non-directive antenna while still keeping low power consumption.

V. CONCLUSION

A short-range mm-wave 50GHz wireless OOK receiver for 10Gbps communication has been presented. The receiver was realized in 28nm CMOS technology and it consumes 70mW from 1V power supply when effectively demodulating a 10Gbps signal at 10cm distance with a BER of 10^{-12}.
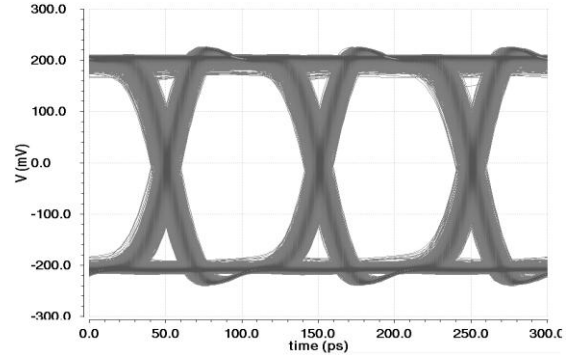

Figure 7.   Simulated single-ended eye diagram with noise, corresponding to a communication distance of 10cm.

TABLE I.   TYPE COMPARISON OF THE PROPOSED SOLUTION WITH THE STATE OF THE ART.

	Datarate (Gb/s)	Distance (mm)	$G_{Antenna}$ (dBi)	$f_{carrier}$ (GHz)	Pdiss (mW)	Tech CMOS
[15]	4	1000	25	60	308	90n
[19]	1.5	1000	6.5	60	1772	90n
[12]	1.5	60	5.0	60	286	90n
[16]	2.5	1000	24	84	327	65n
[17]	6.0	2000	25	60	230	65n
[18]	11	50	2.0	60	358	65n
[20]	2.62	40	0.0	60	1348	65n
[1]	11	14	4.0	56	70	40n
This Work	**10**	**100**	**3.0**	**50**	**170**	**28n**

REFERENCES

[1] K. Kawasaki *et al.*, "A Millimeter-wave intra-connect solution," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2655-2666, Dec. 2010.

[2] M. Bassi, M. Caruso, A. Bevilacqua, and A. Neviani, "A 1.75–15 GHz stepped frequency receiver for breast cancer imaging in 65 nm CMOS," in *Proc. ESSCIRC 2012*, Sept. 2012, pp. 353-356.

[3] M. Bassi *et al.*, "An integrated microwave imaging radar with planar antennas for breast cancer detection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 2108-2118, May 2013.

[4] E. Mammei, E. Monaco, A. Mazzanti, and F. Svelto, "A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension," in *Proc. IEEE Solid State Circuits Conf.*, Sanfransisco, USA, Feb. 2013, pp. 350-351.

[5] A. Ghilioni, A. Mazzanti, and F. Svelto, "Analysis and design of mm-wave frequency dividers based on dynamic latches with load modulation," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1842-1850, Aug. 2013.

[6] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2943-2955, Dec. 2011.

[7] B. Razavi, "Gadgets gab at 60 GHz," *IEEE Spectrum*, vol. 45, no.

2, pp. 46-58, Feb. 2008.

[8] C. H. Jan *et al.*, "RF CMOS technology scaling in high-k/metal gate era for RF SoC (system-on-chip) applications," in *Proc. 2010 IEEE International Electron Devices Meeting*, San Francisco, USA, Dec. 2010, pp. 27.2.1 - 27.2.4.

[9] S. Soldà *et al.*, "A 5 Mb/s UWB-IR transceiver front-end for wireless sensor networks in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1636-1647, July 2011.

[10] A. Gerosa, S. Soldà, A. Bevilacqua, D. Vogrig, and A. Neviani, "An energy-detector for noncoherent impulse-radio UWB receivers," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 5, pp. 1030-1040, May 2009.

[11] Z. Wang, "Full-wave precision rectification that is performed in current domain and very suitable for CMOS implementation," *IEEE Transactions on Circuits and Systems I*, vol. 39, no. 6, pp. 456-462, June 1992.

[12] L. Jri, Y. Chen, and H. Yenlin, "A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 264-275, Feb. 2010.

[13] R. P. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 512-521, Aug 1987.

[14] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2138-2146, Dec. 2003.

[15] C. Marcu *et al.*, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3434-3447, Dec. 2009.

[16] S.-J. Huang, Y. C. Yeh, W. Huaide, P. N. Chen, and J. Lee, "W-band BPSK and QPSK transceivers with costas-loop carrier recovery in 65-nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 3033-3046, Dec. 2011.

[17] A. Tomkins, *et al.*, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2085-2099, Aug. 2009.

[18] K. Okada *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2988-3004, Dec. 2011.

[19] T. Tsukizawa *et al.*, "A fully integrated 60GHz CMOS transceiver chipset based on WiGig/IEEE802.11ad with built-in self calibration for mobile applications," in *Proc. IEEE International Solid-State Circuits Conference*, Sanfransisco, USA, Feb. 2013, pp. 230-231.

[20] T. Mitomo *et al.*, "A 2-Gb/s throughput CMOS transceiver chipset with in-package antenna for 60-GHz short-range wireless communication," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3160-3171, Dec. 2012.

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