A Wide Tuning Range mm-Wave LC VCO

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***Abstract*—A 50 GHz cross-coupled complimentary differential LC VCO is presented in this paper. The VCO is implemented in 28nm bulk CMOS technology node and occupies an area of 0.007mm^2 excluding the pads. The circuit draws 5.2mA of current from a 1.0V supply and delivers a zero to peak output swing of 310mV to 360mV to the output buffer. It achieves a worst case phase noise of -113.2dBc/Hz at 10MHz offset leading to a figure of merit (FOM) higher than 182.3dBc/Hz at 50GHz. By employing a differential tuning mechanism based on a varactor and switched capacitors the VCO can be tuned from 47.4GHz to 52.7GHz corresponding to a tuning range of 10.5%. Furthermore, through a tunable gate bias for the NMOS core transistors, the power consumption of the VCO can be adjusted depending on the load of the tank. This way a power efficient design is obtained.**

***Index Terms*—voltage-controlled oscillators (VCO), mm-wave, cross-coupled pair, A-MOS varactor, CMOS**

I. Introduction

Millimeter-wave (mm-wave) wireless communication systems are attracting growing interests. With the continuous scaling of CMOS processes, it is now possible to design circuits operating in millimeter-wave frequency range using silicon technology. Several applications either exist or are envisioned for mm-wave frequencies among which, are broadband multi-Gbps data communication, automotive radar, medical & security imagining and chip-to-chip communication [1]-[3].

A mm-wave voltage-controlled oscillators is a key component in any radar or communication system. Ultra low power and low phase noise VCOs have been reported previously [4] but at the expense of reduced frequency tuning range. A frequency tuning range of more 20% is obtained in [5], [6] at the cost of large die area and power consumption.

LC VCOs can set a good compromise between frequency tuning range, phase noise, and power consumption by optimally sizing the VCO core transistors and maximizing the varactor capacitance range.

As any other mm-wave CMOS circuits, both lumped-element and distributed structures can be employed for mm-wave VCOs. Generally speaking, a purely lumped-element implementation results in a more compact design, whereas a distributed approach leads to better matching between simulation and measurement results [6].

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An essential component for any lumped LC VCO is the spiral on-chip inductor. However, it comes with the drawback of consuming large die area which translates to higher cost for the circuit. This trend is more pronounced in deeply scaled technologies because in contrast to their active counterparts, passive devices do not significantly reduce in size with process scaling.

Consequently, with the aim of reducing the die area, part of active and passive devices can be placed underneath the on-chip inductor to utilize the third dimension of an integrated circuit. Nonetheless, the size of the devices placed underneath the inductor should be kept small, so that the induced eddy current loops are localized in small regions and the losses are kept to a minimum.

Since the quality factor of varactor is inversely proportional to frequency and becomes dominantly low at mm-wave frequencies it is an extremely challenging task to design a high Q and wide tuning range VCO at mm-wave. Benefits from technology scaling cannot be expected. In particular, the higher quality factor of varactors at nodes with a smaller minimum feature size is at the cost of lower tuning range. Furthermore, due to the reduced supply, the range of variations of C_{max}/C_{min} and accordingly the tuning range of the VCO reduces. Furthermore, the limited supply voltage for the deeply scaled technology nodes reduces the output swing (hence increasing the phase noise), presenting another bottleneck for mm-wave VCO design.

The stringent trade-off between quality factor and tuning range of mm-wave oscillators dictates a low tuning range for a high FOM VCO. Various techniques exploiting alternative tuning approaches have been proposed to set a compromise between tuning range and FOM [7], [8].

This paper presents a low power wide tuning range 50GHz VCO, to address the aforementioned design constraints. The paper is organized as follows: The detailed structure and design of the VCO is presented in Section II. Layout of the VCO is described in Section III. Section IV provides the simulation result of the presented VCO and compares the result with some of state of the art. Finally, section V concludes the paper.

II. Design of the 50 GHz VCO

Different approaches can be used to implement the VCO. One possible architecture, shown in Fig. 1.(a), is employing the NMOS only tail biased topology. In this

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topology the common mode voltage at the tank is equal to V_{DD}. Consequently, it has a limited tuning range for the varactor. This is because the capacitance range corresponding to negative V_{GS} (for $V_{cont} > V_{DD}$) remains unused. Employing dc decoupling between the varactor and the output node and defining the dc voltages at the gates of the varactors equal to $V_{DD}/2$ solves this issue but poses its own challenges. The main drawback stems from the parasitics of the decoupling capacitors which load the tank and lower the operation frequency or force smaller inductance value to keep the same operating frequency. Furthermore, since the resistors used for biasing the varactors appear approximately in parallel with the tank, their value must be chosen much greater than the tank parallel resistance R_p. Even a tenfold ratio is not adequate as it lowers the Q approximately by 10%. The noise of these resistors modulates the varactor and produces substantial phase noise. Moreover, the noise on the mid supply bias and the biasing resistors directly modulate the varactors, resulting in substantial phase noise.

Another possibility to implement the VCO is the NMOS only top biased topology (Fig. 1.(b)). It can be used to utilize the whole tuning range of the varactor by biasing the output node at $V_{DD}/2$. However, when entering triode region each transistor in top biased architecture provides a direct resistive path to ground. Since the center tap of the tank inductor is also at ac ground, the tank Q heavily deteriorates. Thus, the top biased topology suffers severely when the cross coupled transistors enter deep triode region. Furthermore, due to the modulation of the output common mode level (and hence the varactors) by the noise current of I_{bias} this topology suffers from a high phase noise.

To address some of these drawbacks, in this design an NMOS-PMOS cross coupled pair is employed to construct the VCO. In this architecture the bias current is re-used by the PMOS devices, providing a higher transconductance for the same bias current and leading to faster switching of the cross coupled differential pair. But a greater benefit of this topology is the doubled voltage swing that it provides for a given bias current and inductor design. This is because in this architecture the current in each branch swings between $+I_{ss}$ and $-I_{ss}$ while in the NMOS/PMOS only topologies it swings between I_{ss} and zero.

A traditional NMOS-PMOS cross coupled VCO is illustrated in Fig. 1.(c). Due to the small available headroom for the bias current (I_{ss}), its noise current given by $4KT\gamma g_m$ tends to be large. This noise current modulates the output common mode level and accordingly the capacitance of the varactors, generating phase noise.

Furthermore, taking into account the available 1V supply and the threshold voltages of transistors, it is impossible to stack three transistors on top of each other and keep them in saturation in the employed 28nm technology node.

To solve these issues, according to Fig. 2, the bias current source is removed and the DC voltages at the gate of the NMOS core transistors are separated from the voltages at their drains through decoupling capacitors. A voltage source provides the bias for the NMOS pair.

Although removing the bias current source increases the supply sensitivity of the oscillator it leads to higher output swing because of the omission of the voltage headroom required to bias this current source. Furthermore, since it is one of the basic contributor of flicker noise ($1/f^3$), additional circuitries are commonly used to suppress its effect [9]. Removal of the current source leads to further simplification of the designed VCO.

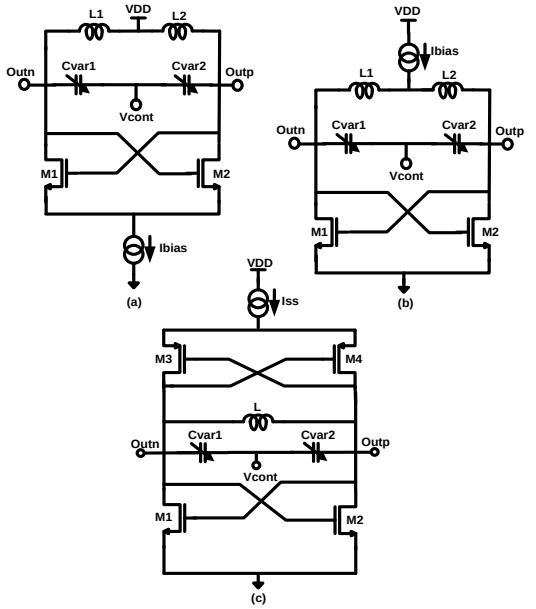

Figure 1. Different architectures for the VCO: Tail biased topology (a), top biased topology (b) and complimentary cross coupled pair (c)

To adjust the direct current in each oscillation band for the start-up of the oscillation, the VCO incorporates a digitally controlled biasing strategy. Utilizing a tunable control voltage helps to partially compensate the effect of Process, Voltage, Temperature (PVT) variations by regulating the bias current of the VCO through the gate voltage of NMOS core transistors.

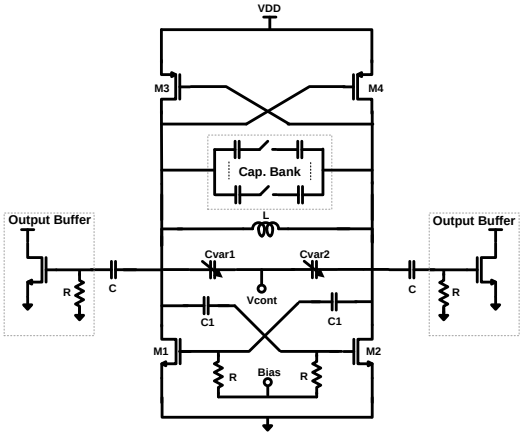

Figure 2. Schematic of the proposed VCO.

An Accumulation MOS (AMOS) varactor is used for frequency tuning. Due to its superior performance in terms of quality factor and tuning range, thin oxide

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varactor is selected over the thick oxide to realize the tank tunable capacitance. To achieve maximum quality factor, minimum allowed length -which is 50nm (60% larger than the minimum feature size)- has been chosen for the varactor while a 1μm width compromises tuning range and quality factor. Such varactor dimensioning results in a nominal variable capacitance of 22fF.

In order to symmetrically cover the positive and negative ranges of the varactor, the core transistors are sized and biased such that the common mode voltage at the tank equals $V_{DD}/2$.

A capacitive bank, switches fixed MOM capacitors in and out of the tank to extend the tuning range of the VCO.

The "on" resistance of the switches degrades the quality factor of the tank in discrete tuning. To lower the effect of this issue, according to Fig. 3.(a) switch (S_1) is put between the two MOM capacitors such that with differential switching at these nodes only half of R_{on} appears in series with each unit capacitor. This allows a twofold reduction in switch width for a given resistance [10].

Unfortunately the biasing switches S_2 & S_3 contribute a large phase noise. To avoid this issue, according to Fig. 3.(b), in this design the bias to drain and source's of S_1 is provided through two large resistors. The resistor biased version exhibits an enhanced Q; thus shows a better trade-off between tuning range and phase noise.

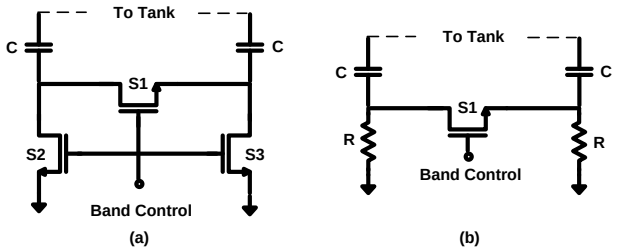

Figure 3. Capacitive bank unit cell (a) Modified capacitive bank unit cell (b).

Design parameters of the 50 GHz VCO are summarized in Table I.

TABLE I. PARAMETER VALUES OF THE DESIGNED VCO

Parameter	Value
Tank Inductor	60pH
Varactor	22fF
Core Transistors	25um
Switched Capacitor	4*x13fF
Decoupling Capacitor	100fF

* Number of rows in the capacitive bank

III. LAYOUT OF THE PROPOSED VCO

The VCO is realized in bulk CMOS 28nm technology node. In realizing the core transistors, gate pitches of 252nm has been selected for both NFET and PFET transistors as optimum compromise between parasitic resistances and capacitances of layout routing. A symmetric differential inductor is used to realize the tank inductance. Symmetric spiral inductors excited by differential waveforms exhibit a higher quality factor than their single-ended counterparts.

The two top most metal layers placed in parallel are employed to lower the series resistance of the single turn 60pH spiral. The outer diameter of the tank inductor is 50μm.

Modern fabrication processes require the most possible uniform metal density. However, on-chip inductors are often made of only few metal layers, resulting in low metal density in a large area. Consequently, dummy metal grids need to be placed under the inductor to maintain metal density uniformity and to meet the minimum density rules. One potential possibility to avoid this is to utilize the area underneath the inductor to put part of the circuitries, hence increasing metal density. Conventionally, due to the concern that components under the inductor would degrade its quality factor through eddy current loss, the real estate underneath the inductor was not utilized. However, if the size of the devices placed inside and/or around the inductor is small, the induced eddy current loops are localized in small regions which keeps the losses to a minimum [11].

Accordingly, as illustrated in Fig. 4, part of the area underneath the spiral is used to put the core circuit and to realize the digital bias control circuitry, reducing the circuit area to just 120x60μm.

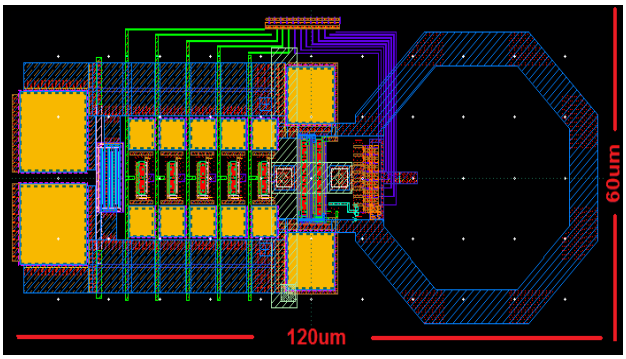

Figure 4. Layout of the proposed VCO. The tank inductor is enclosed by the dashed green line.

An important practical concern at mm-wave frequencies is the routing parasitics, which can result in large discrepancies between simulation and measurement [6]. To obtain a good agreement between simulated and measured results, parasitics of interconnects were carefully modeled through EM simulations and the extracted model illustrated in Fig. 5 was employed for circuit simulations of the tank. L_{par} and R_{par} in this figure show the parasitic inductance and resistance of the connection path, respectively.

The somehow distributed structure of the tank helps to split the tank capacitance from parasitic capacitances of the MOS devices, making possible a wider tuning range for the VCO.

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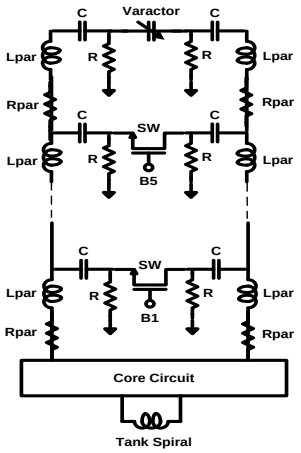

Figure 5. Model used for simulating the VCO's tank.

IV. Simulation Results

To alleviate the loading presented by the subsequent circuitries and further amplify the output swing of the VCO, the LO is connected to a common source buffer stage, which serves to drive the output pads and the 50Ω of the measurement set-up.

The VCO is simulated using Cadence Spectre with a 1.0V supply voltage. The two outputs of the VCO are connected to the buffer stage through two decoupling capacitors. The total current flowing through the VCO is less than 5.2mA.

As the switches in the capacitive bank turn on, the loss of the parallel branches degrades the quality factor of the tank. Consequently, larger g_m is required to start and maintain the oscillation. The required larger g_m is provided by increasing the bias voltage of the NMOS core transistors. This results in power saving because while a higher current is used at lower oscillating frequencies -where it is needed due to the larger tank losses- a smaller current can be used at higher frequencies. This way, the power consumption of the circuit is managed without degrading the phase noise performance.

Simulation results of the tuning range of the VCO versus the bias voltage variations are shown in Fig. 6. The VCO can be tuned from 47.4GHz to 52.7GHz. As expected, a conventional switched capacitor bank would result in non-uniform frequency steps that tighten at lower frequencies. To avoid blind zones in discrete tuning, each two consecutive tuning characteristic are devised to have some overlap.

Aggressively scaled technologies suffer from high process tolerances. A wide tuning range for the VCO guarantees compensation of frequency variation in these technology nodes.

As shown in Fig. 7 the phase noise at 10MHz offset is less than -115dBc/Hz at the center of the band and is below -113dBc/Hz across the whole tuning range of the VCO.

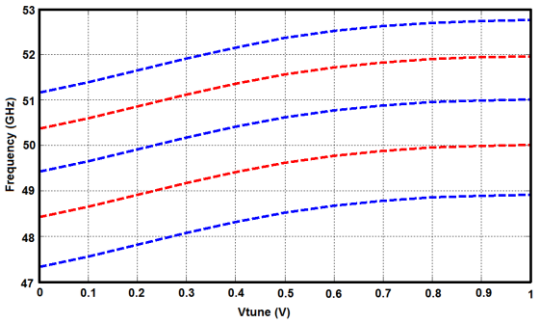

Figure 6. Tuning characteristic of the VCO versus the control voltage.

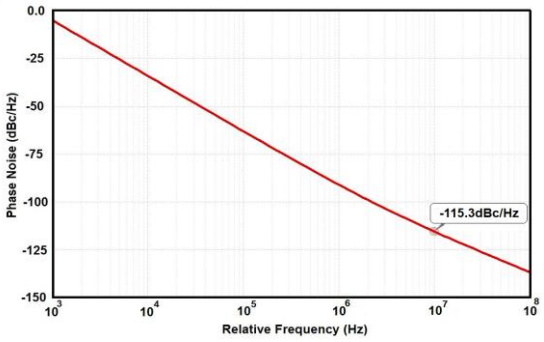

Figure 7. Phase noise vs. frequency offset from carrier at 50 GHz

Table II. compares the performance of the VCO with some of state of the art.

V. Conclusion

A mm-wave LC voltage controlled oscillator is presented in this paper. The VCO employs an NMOS-PMOS cross coupled pair to realize a low power high swing design.

A bank of switched capacitors extends the tuning range of the VCO to more than 10.5% around the center frequency of 50GHz. The VCO draws a maximum current of 5.2mA from a 1V supply.

By employing a variable digital biasing strategy for the gate of the NMOS core transistors, the power consumption of the VCO can be reduced to 2.7mW for the maximum oscillation frequency at which the losses of the tank are at their minimum.

The core area of the VCO is limited to 120µm x 60µm.

TABLE II. Performance of the VCO vs. State of the Art.

Ref.	Tech. (CMOS)	Freq. (GHz)	PN@10M (dBc/Hz)	Power (mW)	TR (%)	FOM (dBc/Hz)	Core (μm^2)
[12]	90nm	52	-117.0	20	11.5	-178.3	-
[6]	65nm	47.5	-118.5	16	22.9	-180.0	220x125
[13]	SiGe HBT	58.4	-115.0	28	14.7	-175.9	-
[5]	SiGe BiCMOS	52.5	-129.0	132	26.5	-182.2	420x400
This work	**28nm**	**50**	**-115.0**	**3.4**	**10.5**	**-183.7**	**120x60**

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It is implemented in 28nm bulk CMOS technology node and achieves a FOM greater than 182.3dBc/Hz across its whole tuning range.

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