Ultra-Low Voltage Low Power Bulk Driven Z Copy-Current Controlled-Current Differencing Buffered Amplifier

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***Abstract*—This paper presents Ultra Low Voltage (ULV) Low Power (LP) Z Copy-Current Controlled-Current Differencing Buffered Amplifier (ZC-CC-CDBA) with single voltage supply. The circuit is performed using bulk driven (BD) technique and it is capable to operate at ULV of 0.65V and consumes low power in the micro range. In addition to the topology simplicity, the proposed circuit offers high linearity and extended output voltage range. Eventually, to verify the functionality of the proposed circuit, current mode multi-function biquad filter using three ZC-CC-CDBAs with two grounded capacitors is included as an example of application. The simulations are performed in PSPICE environment using the 0.18µm CMOS technology from TSMC.**

***Index Terms*—bulk driven, current differencing buffered amplifier, filter, low power circuit**

I. Introduction

Minimizing the power consumption and reducing the supply voltage become essential demands in modern portable electronic devices and battery-powered implantable and wearable biomedical devices. Since low voltage (LV) LP operation either prolongs the battery life time or/and decreases device's size using a smaller battery [1]. These requirements boost the efforts of designers to propose circuits capable to operate under LV LP conditions.

The main barrier in LV LP analog circuit design is the rather high threshold voltage of the MOST. Hence various techniques have been invented to reduce or even remove the threshold voltage from the signal path. Among the most interesting techniques are the non-conventional ones: Bulk Driven (BD), Floating Gate (FG) and Quasi-Floating Gate (QFG) MOST [2]-[4].

The aforementioned non-conventional techniques were successfully utilized to build numerous of modern LV LP active electronic elements [4]-[24]. Since these techniques enjoy the following design advantages: ULV LP operation capability, simple circuitry, and extended input voltage range. Moreover, their relatively lower transconductance value and narrower bandwidth in comparison to conventional gate driven MOST (GD) are attractive features in some applications, such as biomedical ones, since the amplitude and the frequency of the biological signals are extremely low.

The bulk driven (BD) principle was introduced for the first time in 1987 [5]. Although the transconductance of the BD MOST is the smallest among the non-conventional techniques, it is capable to process AC and DC signals, while the capacitively coupled gates of FG and QFG MOSTs prevent processing DC signals. Furthermore The BD MOST occupies smaller area on chip than FG and QFG MOSTs due to their input capacitors [4][17]. During the last decade various interesting and effective active elements were designed utilizing the BD technique, such as operational transconductance amplifiers (OTAs) [4], [6], and [7], operational amplifiers [8], and [9], voltage followers [10], and [11], second generation current conveyors (CCIIs) [12], and [13], current differencing external transconductance amplifiers (CDeTAs) [14], winner take all circuit [15], differential-input buffered and external transconductance amplifiers (DBeTAs) [16] and Differential difference current conveyor (DDCC) [17].

The current differencing buffered amplifier (CDBA) principle was first published in 1999 [25]. Owing to its simplicity and capability to operate in current and voltage modes, it is considered as universal building block for analog signal processing with interesting application potentials. The capability of controlling the transfer parameters of the CDBA extends its applicability. Thus two controlling methods have been proposed: current controlled CDBA (CC-CDBA) [26]-[32], and digitally controlled CDBA (DC-CDBA) [33]. In several applications of the CDBA, There is a need for utilization of the output current signal flowing out of the output terminal to the working impedance [34]. However, this procedure is not easy to be achieved, since any attempt to use the output current affects the entire circuit performance. Therefore, providing copy of the output current is very useful in many applications. This copy can be performed by additional high impedance output terminal of the CDBA, thus this element can be named Z copy CDBA (ZC-CDBA) [35]. The CDBA building block has been widely used to design voltage mode or current mode filters [36]-[44]. Furthermore, various oscillators based on the CDBA were introduced in literature [26]-[28] [45] [46].

Manuscript received November 2, 2013; revised February 27 2014.

doi: 10.12720/ijeee.2.3.229-234

The purpose of this work is to introduce a new simple CMOS structure based on BD technique of the ZC-CC-CDBA capable to operate with ULV LP conditions. Thus the attractive features of this building block can be widely employed in LV LP applications.

This paper is organized as follows. Sect. II presents the principle and the internal structure of the novel ULV LP ZC-CC-CDBA based on the BD technique. In Sect. III, biquad multi-function current mode filter is introduced as an example of application. Sect. IV shows the simulation results, and Sect. V is the conclusion.

II. ULV LP ZC-CC-CDBA

The ZC-CC-CDBA is a five terminal active element; two low impedance input terminals (p, n), two high impedance output terminals (z, zc), and one low impedance output terminal (w). The schematic symbol of the ZC-CC-CDBA and its equivalent circuit are depicted in Fig .1(a) and (b), respectively.

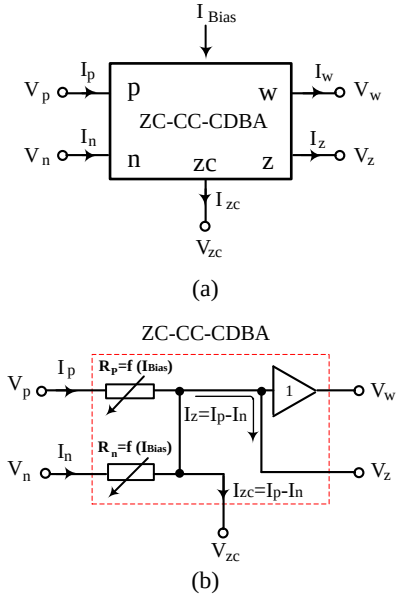

Figure 1. ZC-CC-CDBA: (a) schematic symbol, (b) equivalent circuit.

Unlike the well-known conventional CDBA, the input voltages V_p and V_n are not equal to zero. Instead they have finite parasitic input resistances R_p and R_n, respectively. The input/ output behavior of the ZC-CC-CDBA circuit can be described by the following matrix:

$$\begin{pmatrix} V_p \\ V_n \\ I_z, I_{zc} \\ V_w \end{pmatrix} = \begin{pmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_p \\ I_n \\ V_z \\ I_w \end{pmatrix} \quad (1)$$

The MOS internal structure of the proposed ZC-CC-CDBA is depicted in Fig. 2. Transistors M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, and M_{b6} represent multiple output current mirror providing the constant bias current I_{Bias} to the circuit branches. The current differencing unit (CDU) is the cascade of two BD current followers M_1, M_2, M_3, M_4 and M_5, M_6, M_7, M_8. Each of them is constructed from the flipped voltage follower current sensor structure (BD-FVFCS) [47] with enhanced BD current mirror [18]. This combination provides extremely low voltage operation capability and better linearity. The transistors M_4 and M_8 represent simple voltage source. The current I_B through these transistors is extremely small in comparison with the bias current I_{Bias} to avoid extra undesired offset. The transistors M_9, M_{10} mirror the output current of the first current follower (I_n+I_{Bias}) to be subtracted from the output current of the second current follower (I_p+I_{Bias}). The resulting current (I_p-I_n) is lead away from z terminal. Transistors M_{11} and M_{12} provide a current copy of z terminal to zc terminal. The voltage follower (VF) consists of BD differential input stage M_{13}, M_{14}. Transistor M_{15} acts as a tail transistor of the differential input stage. Transistors M_{b6} and M_{16} represent the second stage of the VF. Transistors M_{b4} and M_{b5} act as an active load. Transistors M_{13}, M_{14}, M_{15} construct BD flipped voltage follower differential structure (BD-DFVF) [47].

Owing to use the BD flipped voltage follower structure in the proposed circuit, the minimum power supply voltage $V_{DD,min}$ can be given by:

$$V_{DD,\min} = V_{GS} + V_{DSsat} \quad (2)$$

whereas V_{GS} and V_{DSsat} are the gate-source and the drain-source voltage of The MOST, respectively. It is obvious from (2) that the proposed circuit is capable to operate under ULV conditions.

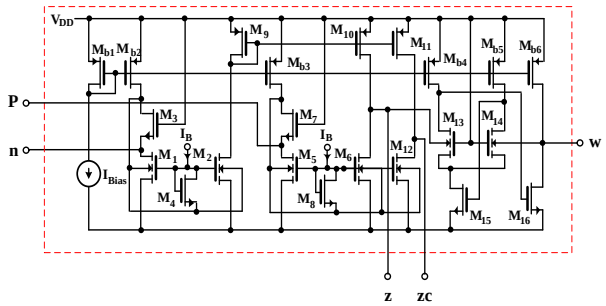

Figure 2. The proposed MOS structure of the ZC-CC-CDBA.

Moreover, the parasitic input resistances R_p, R_n can be described by:

$$R_{n,p} = \frac{1}{g_{m3,7} g_{mb1,5} r_{ds3,7}} \quad (3)$$

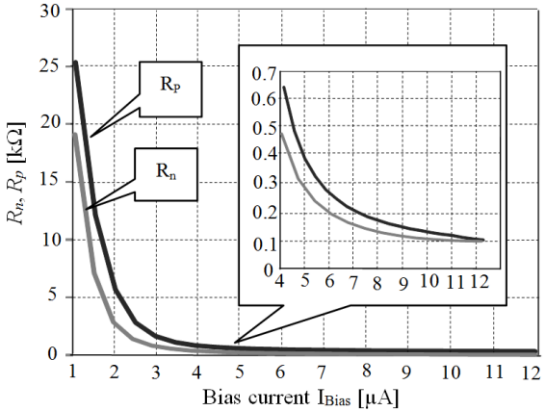

Figure 3. Parasitic resistances R_p and R_n versus the bias current I_{Bias}.

These resistances R_p and R_n can be adjusted via the bias current I_{Bias} as it is shown in Fig. 3. Hence designers started to utilize these resistances instead of the passive resistors in several applications.

III. Application Example

A current mode universal filter based on ZC-CC-CDBA is introduced in this section to confirm the functionality of the proposed circuit [32]. The multi-function current mode filter is depicted in Fig. 4. This filter performs three functions simultaneously: low pass, high pass, and band pass with high output impedance property. The parasitic resistances (R_{p1}, R_{n1}) of the ZC-CC-CDBA$_1$, (R_{p2}, R_{n2}) of the ZC-CC-CDBA$_2$, and (R_{p3}, R_{n3}) of the ZC-CC-CDBA$_3$ can be tuned via bias currents: I_{B1}, I_{B2}, and I_{B3}, respectively. The output currents I_{HP}, I_{BP} and I_{LP} of this filter are flowing out the zc_1, zc_2 and zc_3 terminals, respectively. These currents are flowing into the working impedances directly.

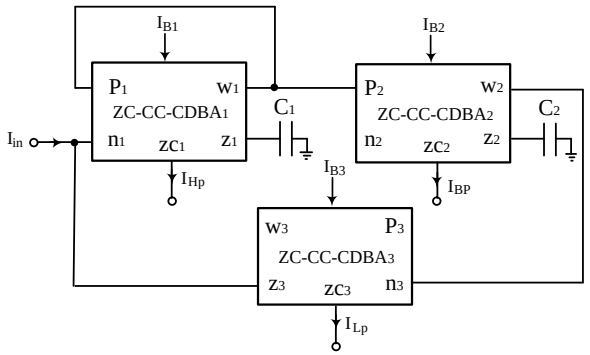

Figure 4. Current mode biquad filter based on ZC-CC-CDBA.

The transfer functions of the filter are given by:

$$\frac{I_{HP}}{I_{in}} = \frac{S^2}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad (4)$$

$$\frac{I_{BP}}{I_{in}} = \frac{-S/C_1 R_{P2}}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad (5)$$

$$\frac{I_{LP}}{I_{in}} = \frac{-1/C_1 C_2 R_{P2} R_{n3}}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad (6)$$

The pole frequency (ω_0) and the quality factor (Q) of the filter are described by:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad (7)$$

$$Q = R_{P1}\sqrt{\frac{C_1}{C_2 R_{p2} R_{n3}}} \quad (8)$$

It is obvious from (7) and (8), that the quality factor can be adjusted independently from the pole frequency by adjusting the value of R_{p1} via I_{B1}.

IV. Simulation Results

A. ULV LP ZC-CC-CDBA Simulation Results:

The performances of the proposed circuit are verified by PSPICE simulator using 0.18 µm CMOS technology from TSMC; its PSPICE model parameters can be found in [48]. The optimal transistors aspect ratios of the proposed circuit ZC-CC-CDBA shown in Fig. 2 are listed in Table. I.

TABLE I. The Transistors Aspect Ratios of The Circuit Shown in Fig. 2

Transistor	W/L [µm/µm]
M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, M_{b6}	15/1.5
M_9, M_{10}, M_{11}	80/3
M_3	3/0.3
M_7	8/0.3
M_1, M_2	40/2
M_5, M_6, M_{12}	40/3
M_4, M_8	80/1
M_{15}	20/3
M_{13}, M_{14}	30/3
M_{16}	15/3

All the simulations are performed for I_{Bias}=3 µA, I_B=4 nA with an extremely low voltage supply of 0.65 V. The DC curves $I_{z,zc}$ versus I_n and I_p are depicted in Fig. 5. Thanks to utilizing enhanced BD current mirror, the proposed circuit offers high linearity of I_z versus I_n and I_p with extremely low current offset whose value is less than 0.05 µA. The DC curves I_z versus I_p for various values of I_n are shown in Fig. 6, whereas the current I_n vary from -3 µA to 3 µA with a step of 1 µA.

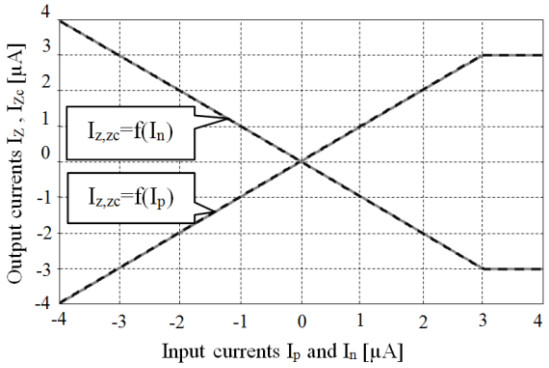

Figure 5. DC curves I_z, I_{zc} versus I_p and I_n.

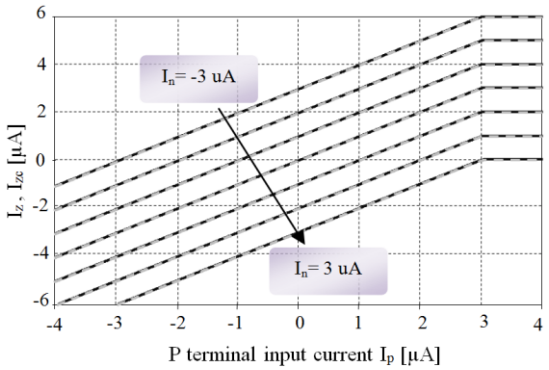

Figure 6. DC curves I_z, I_{zc} versus I_p for various values of I_n.

The frequency responses of the current gains $I_{z,zc}/I_n$ and $I_{z,zc}/I_p$ are shown in Fig. 7. The current gains are unity at low frequencies. The cutoff frequencies of these gains are 2.4 MHz and 5.15 MHz of $I_{z,zc}/I_n$ and $I_{z,zc}/I_p$, respectively. The frequency dependence of the parasitic impedance of the z terminal is shown in Fig. 8. The impedance of z terminal is very high about 2.67 MΩ at low frequencies.

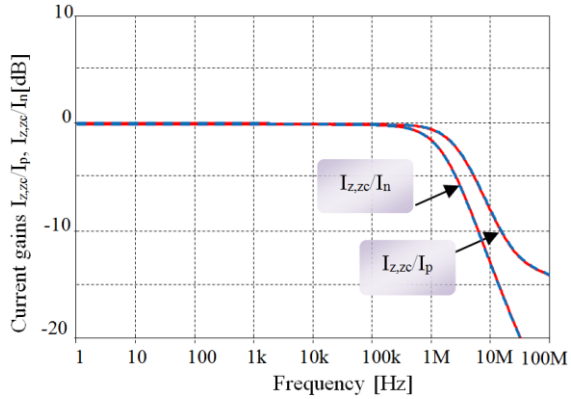

Figure 7. Frequency responses of the current gains $I_{z,zc}/I_p$, $I_{z,zc}/I_n$.

The DC curve V_z versus V_w is shown in Fig. 9. Besides, the voltage error (V_z-V_w) is depicted. The high linearity and the wide range operation can be observed. Furthermore, in the range from 0.04 V to 0.58 V, the voltage error is less than 1 mV.

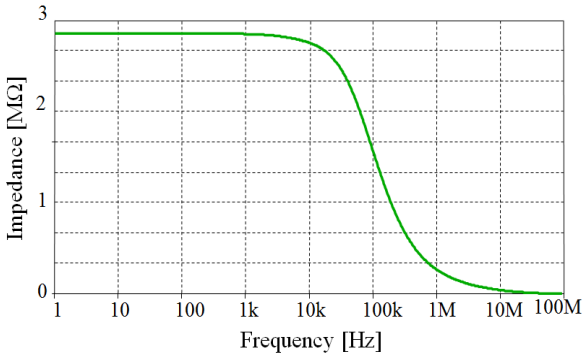

Figure 8. Frequency response of the parasitic impedances of z and zc terminals.

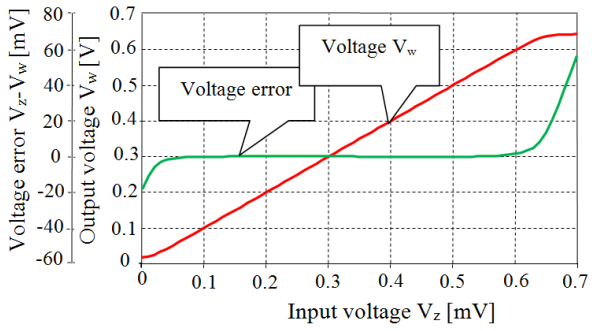

Figure 9. DC curves V_w versus V_z and the voltage error V_z-V_w.

The frequency response of the voltage gain V_w/V_z is clarified in Fig. 10. The AC simulation is performed using capacitive load of 1pF. The cutoff frequency is 11.18 MHz with unity gain at low frequencies.

The frequency response of the parasitic impedance of w terminal is depicted in Fig. 11. The value of this impedance at low frequencies is 1 kΩ. The most important features of the proposed ZC-CC-CDBA are listed in Table II.

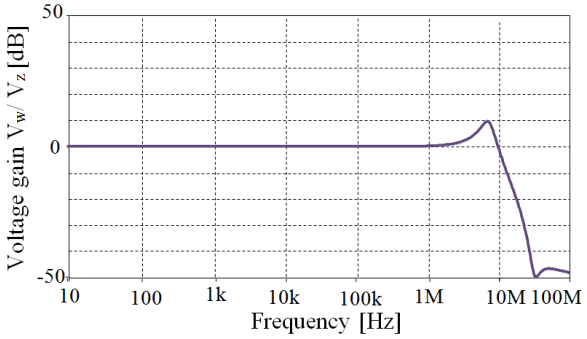

Figure 10. AC curve of the voltage gain V_W/V_Z.

The power consumption of the proposed circuit is extremely low (5.6 µW to 56 µW) for (I_{Bias}=1 µA to I_{Bias}=10 µA), respectively.

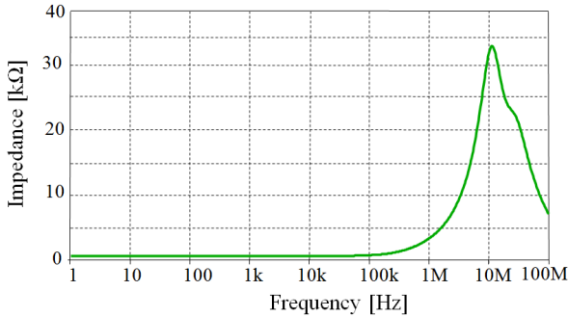

Figure 11. Frequency dependence of the parasitic impedance of w terminal.

TABLE II. THE MOST IMPORTANT CHARACTERISTICS OF THE CIRCUIT IN FIG. 2

Parameter	Value
Voltage supply, bias current	0.65 V, 3 µA
Power consumption for I_{Bias}=3 µA	17 µW
3 dB bandwidth of $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	5.15 MHz, 2.4 MHz
Current offset	<50 nA
Current gains $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	1, 1
3 dB bandwidth of V_w/V_z	11.18 MHz
voltage gain V_w/V_z	1
Voltage offset	<1 mV
Resistance of terminal Z	2.67 MΩ
Resistance of terminal w	1 kΩ

B. Simulation Results of the Current Mode Biquad Filter Based on ZC-CC-CDBA:

The simulation results of the multi-function current mode biquad filter shown in Fig. 4 are depicted in Fig. 12, 13 and 14. The three ZC-CC-CDBAs are biased by I_{B1}=I_{B2}=I_{B3}=1 µA. The components of the filter are C_1=5 nF and C_2=10 nF. That yields the pole frequency of 950 Hz, while the calculated pole frequency from (7) is 1 kHz. Thus the deviation is 5.2%. This error comes from the non-ideal parasitic properties of the ZC-CC-CDBA. The frequency responses of the current gains of the filter

shown in Fig. 4 are presented in Fig.12 for R_{load}=1 Ω. It is obvious that this filter can provide low pass, band pass and high pass functions simultaneously, without any change in the circuit topology. The band pass gain responses for various values of I_{B1} are depicted in Fig. 13. It can be observed that by adjusting the R_{p1} value via I_{B1}, the quality factor can be tuned independent from the pole frequency as it was clarified in (7) and (8). Moreover, Fig. 14 depicts the band pass filter gain responses for (I_{B1}=I_{B2}=I_{B3}=0.5 μA, 1 μA and 1.5 μA), it is noticeable that the pole frequency can be adjusted without affecting the quality factor as it was described in (7) and (8).

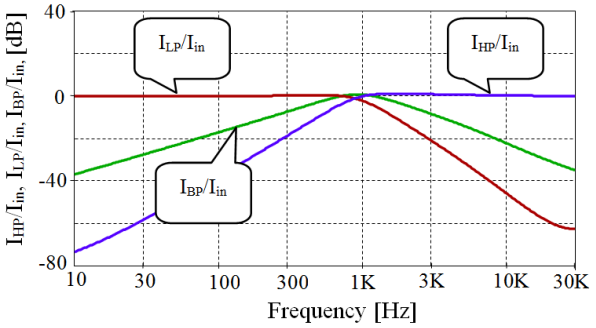

Figure 12. Frequency response of the proposed filter.

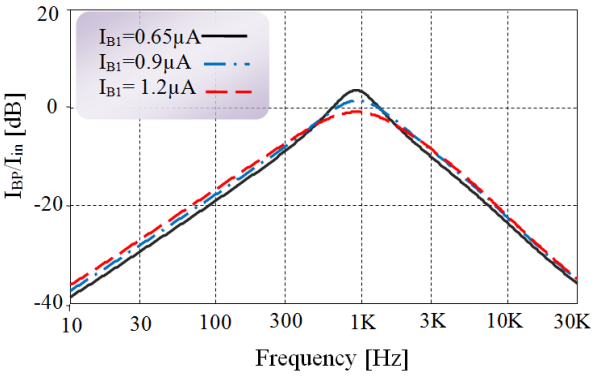

Figure 13. The response of the band pass filter for different I_{B1} values.

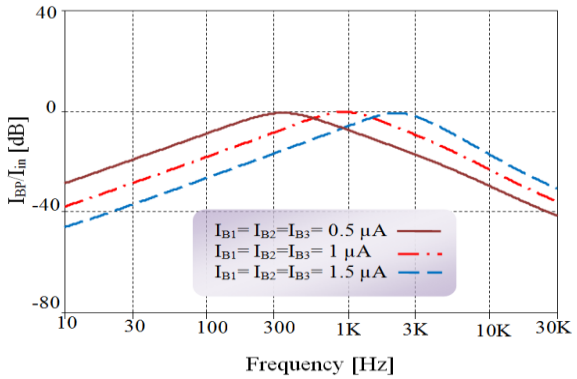

Figure 14. The response of the band pass filter for different values of I_{B1}, I_{B2} and I_{B3}.

V. Conclusions

This paper presents a new ULV LP bulk driven based ZC-CC-CDBA capable to operate under single supply voltage of only 0.65 V. Besides, the proposed circuit enjoys circuit simplicity, high linearity, extended output voltage range and tunable parameters. Furthermore, additional copy of the difference current (I_p-I_n) is available through zc terminal. This additional terminal solves the problem of utilizing output current to drive the working impedance directly. Eventually, as an example of application a multi-function current mode filter is presented to prove the functionality of the proposed circuit. Thanks to the tunable parameters of the circuit the quality factor and the pole frequency are adjustable independently.

Acknowledgment

The described research was performed in laboratories supported by the SIX project; the registration number CZ.1.05/2.1.00/03.0072, the operational program Research and Development for Innovation and has been supported by Czech Science Foundation project No.: P102-14-07724S.

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