

International Journal of Electronics and Electrical Engineering

CONTENTS

Volume 2, Number 4, December 2014

Multilevel Sequential Logic Circuit Design	254
<i>Avni Morgül and Fatma Sarıca</i>	
Fast Lock-in Time Phase Locked Loop Frequency Synthesizer for Continuous-Time Sigma-Delta ADC	259
<i>Jefferson A. Hora, Christina A. Garcia, Stella Sofia I. Sabate, and Meriam Gay Bautista</i>	
Verilog HDL Implementation of a Universal Synchronous Asynchronous Receiver Transmitter	264
<i>Jefferson Hora, Meriam Gay Bautista, Kramer C. Chua, and Demie Mae V. Dajao</i>	
Overstress-Free Charge Pump White LED Driver	270
<i>Allenn dela Cerna Lowaton and Hong-Yi Huang</i>	
3rd-Order Dual Truncation 18-Bit Audio MASH 2-1 Delta-Sigma Digital to Analog Converter in 90nm CMOS Technology Implementation	276
<i>Olga Joy Labajo-Gerasta, Mycel Capilayan, Mark Laurence Dandan, and Sittie Aleyah Magayo-ong</i>	
Gate Strength Aware DC Coverage Improvement	281
<i>Boon Chong Ang and Eng Lian Goh</i>	
3-D Solenoid Inductor Analysis in a 0.13 μm Digital CMOS Technology	286
<i>Chul Nam, Byeungleul Lee, Hyeon Cheol Kim, Jinseok Kim, Dong Wook Chang, and Bonghwan Kim</i>	
12-Bit Pipeline ADC Implemented in 0.09- μm Digital CMOS Technology for Powerline Alliance	291
<i>Olga Joy L. Gerasta, Lavern S. Bete, Jayson C. Loreto, Sheerah Dale M. Orlasan, and Honey Mae N. Tagalogon</i>	
Delay-Locked Loop Using 4 Cell Delay Line with Extended Inverters	298
<i>Jefferson A. Hora, Vincent Alan Heramiz, and Pleiades Faith Longakit</i>	
Full-Custom Design Fractional Step-Down Charge Pump DC-DC Converter with Digital Control Implemented in 90nm CMOS Technology	303
<i>Jhon Ray M. Esic, Van Louven A. Buot, and Jefferson A. Hora</i>	
Tuning and Control of Multi Variable Systems	309
<i>T. Chiranjeevi, I. V. V. Vijetha, B. N. CH. V. Chakravarthi, and M. Karthika</i>	
An Improved Great Deluge Algorithm (IGDA) for Solving Optimal Reactive Power Dispatch Problem	321
<i>K. Lenin, B. Ravindranath Reddy, and M. Surya Kalavathi</i>	
A Novel Encoding Scheme for Cross-Talk Effect Minimization Using Error Detecting and Correcting Codes	327
<i>Souvik Singha and G. K. Mahanti</i>	
Optimized Power Distribution Planning A Review	332

Navpreet Singh Tung and Sandeep Chakravorty

Finding Defective Elements in Antenna Array Using Fast Fourier Transform.....	336
<i>R Muralidharan, A Vallavaraj, G. K. Mahanti, and Ananya Mahanti</i>	