Multilevel Sequential Logic Circuit Design

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***Abstract*—Multilevel logic circuits has advantages of simpler circuit complexity, less interconnections and small chip area. However it has not found enough attention and applications because there is not sufficient hardware available. Reference [1] proposes a multilevel flip-flop circuit and its applications for building counter circuits. In this paper it is shown that it is possible to design any arbitrary sequential logic circuit by using this flip-flop. The multilevel circuit is simpler and uses fewer transistors compared to the binary equivalent circuit.**

***Index Terms*—multivalued logic, sequential logic, multivalued flip-flop, current mode CMOS logic**

I. Introduction

Multilevel or multivalued logic circuits (MVL) may implement the logic operations more efficiently and faster by increasing the radix of the system or the number of levels used, in the expense of reduced noise margin. These systems become equivalent to an analog system if the radix is very large. So, it suffers from the noise and parameter variations of the components used in the realization.

The current mode design can be successfully applied to higher-radix or multi-valued logic circuit design, abbreviated as CM-MVL. Current-mode MVL structures are presented in [11]**Hata! Başvuru kaynağı bulunamadı.**.

In current-mode design, the parameter variations of the components and the noise may result in incorrect logic levels may be obtained, if the number of cascaded stages exceeds a certain value. Therefore, it is unavoidable to restore the tabulated levels after a certain number of stages, unless the gates are self-restored type [12]. A new full-current mode CMOS-MVL restoration circuit is presented in [13].

II. Definitions

In a radix-*r* multilevel system, any *m*-variable logic function, $f(x_1, x_2,\ldots, x_m)$ may be represented in terms of basic operations, *MIN*, *MAX* and inverter. Here, each variable, x_i, takes a value from the set $R=\{0,1,\ldots, r\text{-}1\}$. The radix, *r*, corresponds to the number of possible signal levels. In current mode MVL logic, levels are represented by current levels in terms of a base current, I_b. Thus, a variable $x=0$ is associated with the current level value, $I_0=0$, $x=1$ is associated with $I_1=I_b$ and so on. However, in the circuits, a logic current level *l*, actually corresponds to an interval of the continuous quantity, *y*, such that

$$y \rightarrow l: \ \{y|\ (l-05)I_b \le y < (\ l+0.5)I_b\ \} \qquad (1)$$

This means that a total parameter variation plus noise of $\pm$ ½I_b may be tolerated.

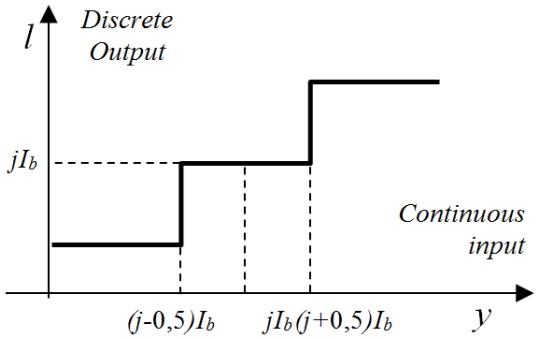

Figure 1. Conversion of continuous input signal to multilevel.

The definitions of basic MVL operations are given below [11].

$$MIN(x,y)=x\cap y=x\bullet y$$

$$MAX(x,y)=x\cup y=x+y$$

Complement of *x* :

$$\bar{x} = r-1-x$$

Truncated difference,

$$x \Xi y = \begin{cases} x-y & \text{if } x \ge y \\ 0 & \text{otherwise} \end{cases}$$

The literal, (L)

$$L(k,{}^a x^b) = \begin{cases} k & \text{if } a \le x \le b \\ 0 & \text{otherwise} \end{cases}$$

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$$k\text{-}CWC: \overset{k}{x^{\rightarrow}} \equiv (x+k) \mod r$$

The upper and lower threshold operations

$$upper-threshold,\ th_u:\ a|_b^c = \begin{cases} c & if\ a \geq b \\ 0 & otherwise \end{cases}$$

$$lower-threshold,\ th_l:\ {}_b^c|a = \begin{cases} c & if\ a \leq b \\ 0 & otherwise \end{cases}$$

III. Sequential Circuits

It is known that the basic building blocks of sequential logic circuits are the flip-flops. Characteristic equations and next-state tables for conventional flip-flops such as *SR*, *JK*, and *T* , for multilevel input signals are introduced in several studies [4]-[5].

Unfortunately, circuit level implementations of the equations are very complicated [6], [7] and they require the inversion of the current state output to calculate the next state. In current mode designs, inversion is performed by subtracting the current from the maximum allowable current [i.e. $(r - 1)I_0$]. This operation increases the power consumption considerably. So, the inverter must be avoided for a low power design.

Since all standard flip-flop equations require inversion, it is decided to define a new flip-flop, which does not use any inverter. This new flip-flop is called AB flip-flop because it has two inputs, A and B, and the transition equation which does not have inverted terms, is stated as follows [1]:

$$Q_{n+1}=A+B\bullet Q_n$$

The state transition table of the AB flip-flop is given in Table I. The flip-flop can successfully change its state for any input combination.

TABLE I. Transition table of the AB Flip-Flop

AB / Q_n	00	01	02	03	10	11	12	13	20	21	22	23	30	31	32	33
0	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
1	0	1	1	1	1	1	1	1	2	2	2	2	3	3	3	3
2	0	1	2	2	1	1	2	2	2	2	2	2	3	3	3	3
3	0	1	2	3	1	1	2	3	2	2	2	3	3	3	3	3

Block diagram of the AB flip flop is given in Fig. 2. It is composed of a *MIN* circuit to perform AND operation, a *MAX* circuit to perform OR operation and a *LATCH-RESTORER* circuit to HOLD and restore the current state.

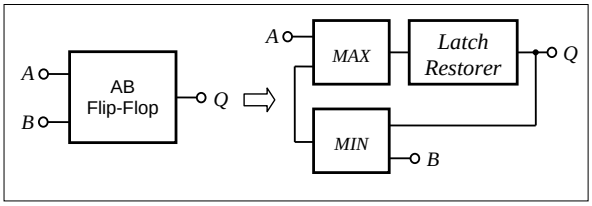

Figure 2. Block diagram of the AB flip-flop.

The *MIN* [14] and *MAX* [15] circuits are current-mode, multi-input circuits working based on winner/loser-takes-all principle as shown in Fig. 3. Although there are other simpler implementations of *MIN* and *MAX* circuits in the literature [4], this circuit is preferred because of its robustness. The *LATCH/ RESTORER* circuit is based on level restoration circuit design given in [13] and optimized for the new application to obtain smooth transitions. Since the current mode multilevel circuits are not self-restored the predefined current levels can be deviate from their original values due to some variations in active element dimensions, power supplies, technology parameters, etc. The signal must be restored to its original value before the variations exceeds $\pm I_b/2$ value. In addition, the flip-flop circuits have positive feedback in nature, which prohibits any variation from the predefined level. Otherwise, this variation forces the output to shift either to ground or power supply voltage. The restoration circuit is modified as LATCH/RESTORER circuit by adding a pass transistor properly. Both HOLD and restore operations performed at the same time by using the circuit given in Fig. 4.

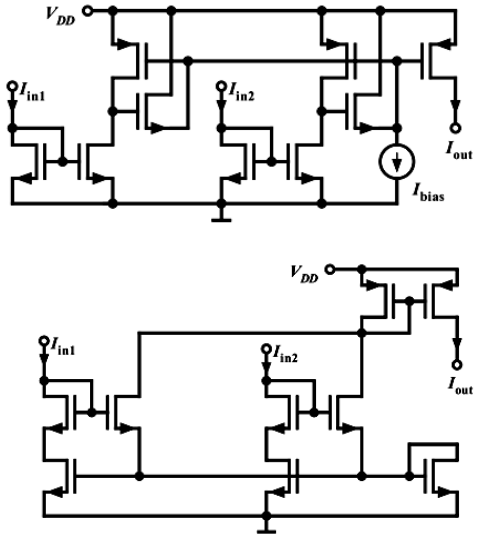

Figure 3. (a) *MIN* and (b) *MAX* circuits [14], [15].

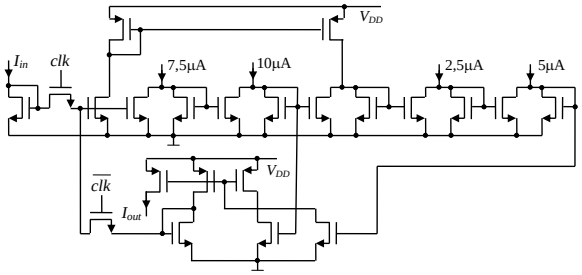

Figure 4. Modified latch and restoration circuit.

Timing of the flip flop circuit is performed by using two-phase clock signals (*clk*, $\overline{clk}$) which control the pass transistors of the latch circuit. The number of *Q* outputs (I_{out}) can be increased by adding more current mirrors to the final stage.

IV. Implementation of Sequential Circuits

Different type of sequential circuits, such as counters is designed by using the AB flip-flop, in order to show its usability.

A 1-digit modulo-4 counter is designed to test the new flip-flop. Then, the counter design work is extended to synchronous and asynchronous 2-digit modulo-16 counters. All these circuits are tested successfully [1]. A 4-level logic system is preferred (although most circuits are radix-free, minor modifications may needed to change/increase the logic levels for a 1-digit counter), in order to keep the noise margins in reasonable levels.

Using the counting diagram and state transition table of the flip-flop, we can obtain the next-state equation of the counter as follows, after necessary minimizations;

$$A_1 = Q_1^{\to 1},\ B_1 = 0$$
$$A_2 = {}^{3}Q_1^{\,3} \cdot Q_2^{\to 1},\ B_2 = {}^{0}Q_1^{\,2} Q_2$$

Here, $Q_1^{\to 1}$ and $Q_2^{\to 1}$ indicate 1-level clock-wise cyclic operation and ${}^{3}Q_1^{\,3}$ and ${}^{0}Q_1^{\,2}$ are literal operations. The ${}^{3}Q_1^{\,3}$ operation is logically equal to "detect if $Q_1 \geq 3$", and the ${}^{0}Q_1^{\,2}$ operation is logically equal to "detect if $Q_1 \leq 2$". So, we can replace the literal circuits with upper and lower threshold circuits, respectively. Threshold circuits are simpler and use fewer transistors than literal circuits. The complete block diagram of the synchronous 2-digit modulo-16 counter and simulation results are given in Fig. 5 and Fig. 6, respectively.

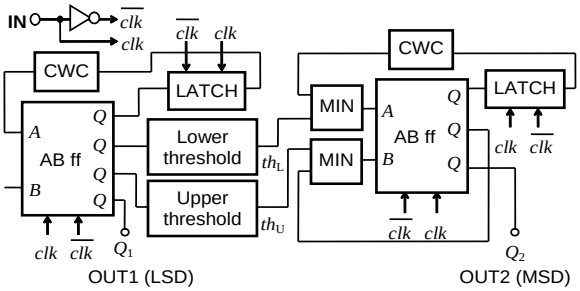

Figure 5. Synchronous 2-digit modulo-16 counter

In order to show the suitability of the proposed new flip-flop, for any sequential multi-valued logic application, we propose and presented in this paper, an arbitrary state diagram for 1-input, 2-output quaternary logic circuit. HSPICE simulations show that circuit is working correctly.

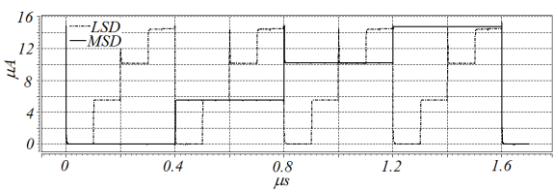

Figure 6. Simulation result of 2-digit modulo-16 counter.

The state diagram of the circuit is given in Fig. 7. Using this state diagram, truth table is formed and introduced in Table II. Here x is an input current, Q_2 and Q_1 are current state outputs and combined with x input to generate the excitation functions for A and B inputs of the flip-flops. Q_{2+} and Q_{1+} are the calculated next state output levels.

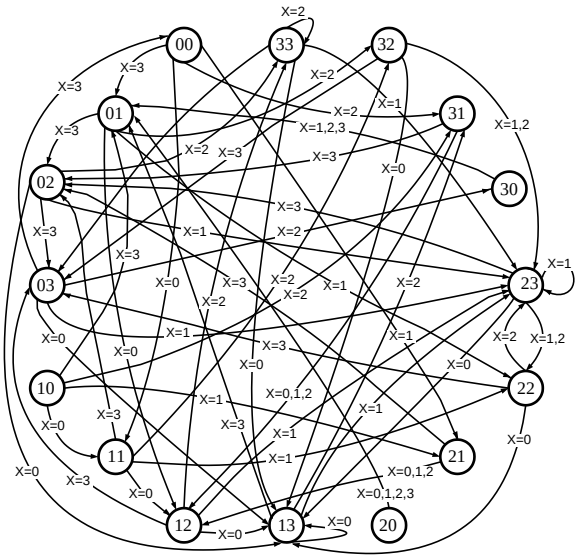

Figure 7. State diagram of the sequential circuit.

TABLE II. Truth Table of the Sequential Circuit

In	Present State		Next State		FF Inputs					In	Present State		Next State		FF Inputs			
x	Q_2	Q_1	Q_{2+}	Q_{1+}	A_1	B_1	A_2	B_2		x	Q_2	Q_1	Q_{2+}	Q_{1+}	A_1	B_1	A_2	B_2
0	0	0	1	1	1	0	1	0		2	0	0	3	1	1	0	3	0
0	0	1	1	2	2	1	1	0		2	0	1	3	2	2	0	3	0
0	0	2	1	3	3	2	1	0		2	0	2	3	3	3	0	3	0
0	0	3	1	3	0	3	1	0		2	0	3	3	0	0	0	3	0
0	1	0	1	1	1	0	1	0		2	1	0	3	1	1	1	3	0
0	1	1	1	2	2	1	1	1		2	1	1	3	2	2	1	3	1
0	1	2	1	3	3	2	1	1		2	1	2	3	3	3	1	3	1
0	1	3	1	3	0	3	1	1		2	1	3	3	1	0	1	3	1
0	2	0	0	1	1	0	0	0		2	2	0	0	1	1	2	0	0
0	2	1	1	2	2	1	0	1		2	2	1	1	2	2	2	0	1
0	2	2	1	3	3	2	0	1		2	2	2	2	3	3	2	0	2
0	2	3	1	3	0	3	0	1		2	2	3	2	2	0	2	0	2
0	3	0	0	1	1	0	0	0		2	3	0	0	1	1	3	0	0
0	3	1	1	2	2	1	0	1		2	3	1	1	2	2	3	0	1
0	3	2	1	3	3	2	0	1		2	3	2	2	3	3	3	0	2
0	3	3	1	3	0	3	0	1		2	3	3	3	3	0	3	0	3
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1	0	2	2	3	3	2	2	0		3	0	2	0	3	3	0	0	0
1	0	3	2	3	0	3	2	0		3	0	3	0	0	0	0	0	0
1	1	0	2	1	1	0	2	0		3	1	0	0	1	1	1	0	0
1	1	1	2	2	2	1	2	1		3	1	1	0	2	2	1	0	0
1	1	2	2	3	3	2	2	1		3	1	2	0	3	3	1	0	0
1	1	3	2	3	0	3	2	1		3	1	3	0	1	0	1	0	0
1	2	0	0	1	1	0	0	0		3	2	0	0	1	1	2	0	0
1	2	1	1	2	2	1	0	1		3	2	1	0	2	2	2	0	0
1	2	2	2	3	3	2	0	2		3	2	2	0	3	3	2	0	0
1	2	3	2	3	0	3	0	2		3	2	3	0	2	0	2	0	0
1	3	0	0	1	1	0	0	0		3	3	0	0	1	1	3	0	0
1	3	1	1	2	2	1	0	1		3	3	1	0	2	2	3	0	0
1	3	2	2	3	3	2	0	2		3	3	2	0	3	3	3	0	0
1	3	3	2	3	0	3	0	2		3	3	3	0	3	0	3	0	0

Using this truth table, we obtain the input functions, by inspection, as follows (unfortunately there is not a simple method to simplify the multilevel logic equations).

$$A_1 = Q_1^{\to 1}$$

$$B_1={}^0x^1 \cdot Q_1+{}^2x^3 \cdot Q_2$$

$$A_2={}^0Q_2^1 \cdot x^{\to 1}$$

$$B_2 = x^{\to 1} \cdot Q_1 \cdot Q_2$$

Here, $Q_1^{\to 1}$ Indicates 1-level clock-wise cyclic operation. ${}^0x^1$ and ${}^2x^3$ are literal operations [9]. They are logically equal to "detect if $x \le 1$" and "detect if $x \ge 2$", respectively. So, we can replace the literal circuits with upper and lower threshold circuits. Threshold circuits are simpler and use fewer transistors than literal circuits. The new sequential circuit can be designed as given in Fig. 8, by using these equations.

The circuit is tested for different input *x* currents, and the resulting output currents are shown in Figure 9. The results are totally compatible with the state diagram introduced in Fig. 7.

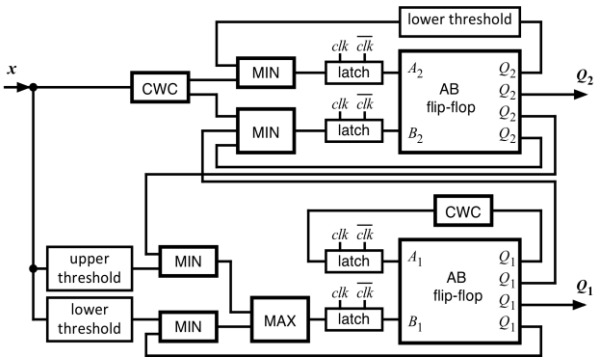

Figure 8. The sequential circuit

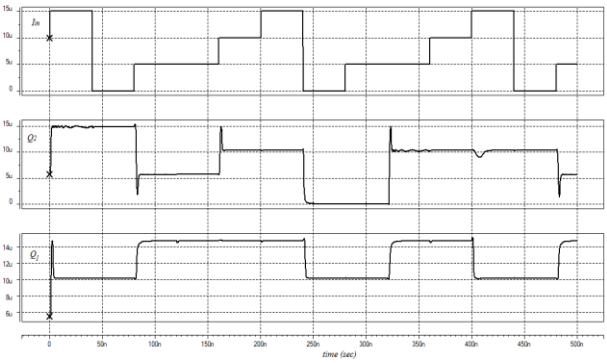

Figure 9. The input and output waveforms

V. Conclusion

In this study, we show that any sequential multi-valued logic circuit can be realized with the new multilevel AB flip-flop. An arbitrary state diagram for 4-level logic is drawn and it is realized by using the new flip-flop.

Future studies will be based on designing edge-triggered flip-flops rather than level triggered ones. This will hopefully reduce the number of transistor used and will improve the speed considerably.

Another issue about multi-valued circuits is the minimization issue. Unfortunately there is no known method, which may be implemented easily, to simplify the multilevel logic equations. The circuit designs will be less complicated with the effective minimization algorithms.

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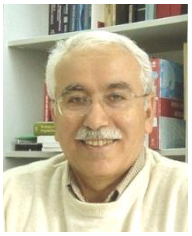

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