Fast Lock-in Time Phase Locked Loop Frequency Synthesizer for Continuous-Time Sigma-Delta ADC

Jefferson A. Hora, Christina A. Garcia, Stella Sofia I. Sabate and Meriam Gay Bautista
Microelectronics Lab, EECE Department, MSU-Iligan Institute of Technology, Iligan City, Philippines
Email: jefferson.hora@g.msuiit.edu.ph, meriamgay.bautista@g.msuiit.edu.ph

***Abstract*—A phase locked loop circuit that uses Phase Frequency Detector with NOR gates and divide-by-64 with pseudo-NMOS divide-by-2 frequency divider is proposed, designed and simulated in TSMC 0.18um 1P6M CMOS process technology to come up with minimum chip area and achieve fast lock-in time. This PLL design is specifically intended for Continuous-Time Sigma-Delta ADC operating at 640MHz frequency which is an important component of ICs used in electronics and communication devices whose clock rates and timing relationships are vital. This work has a lock-time of around 2.5us which is a fast lock-in value for the lock-in time of ADC clock generator. The desired output frequency which is 640 MHz is achieved on all corners ranging from 608 MHz to 672 MHz which is within 640MHz ±5% tolerance. In terms of the charge pump current, the proposed design used 77uA which is within the typical values of charge pump current ranging from 10uA to 100u. The PLL displays minimum total chip core area which is 8.3393 nm^2 and 0.2049 um^2 for off-chip and on-chip filter, respectively.**

***Index Terms*—phase locked loop, frequency synthesizer, sigma-delta ADC, phase detector, pseudo-NMOS dividers, charge pump**

I. Introduction

Digital systems make use of data in binary form that calls for the need of clocks to synchronize binary digits of 0s and 1s. As technology gets better with faster speed performance, engineers are challenged to sustain good clock synchronization. PLL is used in order to generate well-timed on chip clocks used in high performance digital systems [1][2].

Clock generation is an important component of any digital circuit. The most common clock references are typically based on quartz crystal oscillators. Crystal oscillators provide excellent stability with variations in supply voltage, temperature and process [3]. However, the typical frequencies covered by crystal oscillators range between few kilohertz up to several hundred megahertz only. Higher frequency clocks are difficult to find and cost much.

Manuscript received December 11, 2013; revised March 1, 2014.
This work is supported by DOST-ERDT funded research Eye-C Program.

Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. These calls for the need of frequency synthesizers that can provide such high frequencies that can't be catered by limited frequency crystal oscillators. As data rates increase to satisfy the increase in on-chip processing rate, the phase relationship between the input data and the on-chip clock is not fixed. To reliably receive the high-speed data, PLL provides a solution. PLL locks the clock phase that samples the data to the phase of the input data. Within the digital systems, well-timed clocks are generated with phase-locked loops (PLLs). The rapid increase of the system's clock frequency possesses challenges in generating and distributing the clock with low uncertainty [4].

In this paper, the crystal oscillator alone will not be able to provide the 640-MHz frequency needed for continuous-time sigma-delta ADC since this frequency is beyond the range of frequencies covered by crystal oscillator manufacturers. Considering the need for higher frequency range to sustain synchronous systems and realizing limited values of crystal oscillators, this study proposes the use of PLL to provide on-chip frequency synthesizers. This study proposes an innovative design of a minimum area phase locked loop in TSMC 0.18um CMOS Technology that can provide a 640 MHz output clock frequency for Continuous-Time Sigma-Delta ADC using a stable crystal reference frequency having a value of 10 MHz. To achieve minimum chip area and better fast lock-in time, different architectures were tested and the compared. The sub-circuits with best results were incorporated to the overall PLL design and implemented with proper floor plan to achieve minimum chip area.

II. System Architecture and Design

A. PLL Overall System

The overall system architecture of designed 640 MHz phase locked loop is composed of mainly of phase frequency detector (PFD), charge pump (CP), loop filter, voltage controlled oscillator (VCO), and divide-by-64 frequency divider as shown in Fig. 1.

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of

doi: 10.12720/ijeee.2.4.259-263

the reference clock. Over time, small frequency differences accumulate as an increasing phase error. If there is a phase difference between the two signals, it generates "up" or "down" synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an "up" signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage Vcontrol. On the contrary, if the error signal from the PFD is a "down" signal, the charge pump removes charge from the LPF capacitor, which decreases Vcontrol. Vcontrol is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP.

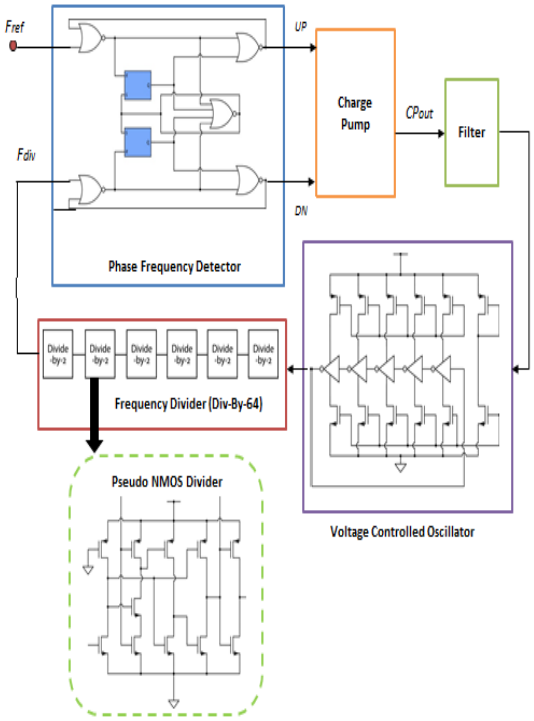

Figure 1. PLL overall system.

The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an "up" signal, the VCO speeds up. On the contrary, if a "down" signal is generated, the VCO slows down. The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock.

B. Phase Frequency Detector

The PFD is designed to generate symmetrical charge-up (up) and charge-down (dn) pulses [2]. The potential dead zone is eliminated by the four-input NOR gate, which acts as a reset to produce a minimum pulse width at the PFD output even when the phase error is zero [5].

The main cause of the dead zone is the relationship between the propagation delay of the internal gates for the reset of the PFD and the switching time of the charge-pump currents [6]. The phase frequency detector in this design used NOR gates to detect the phase difference between the two inputs from reference crystal oscillator and the feedback frequency from the divider. The NOR gates were designed so as to give a low phase error while maintaining low power design conditions. Fig. 2 shows the overall PFD with two-input NOR gate.

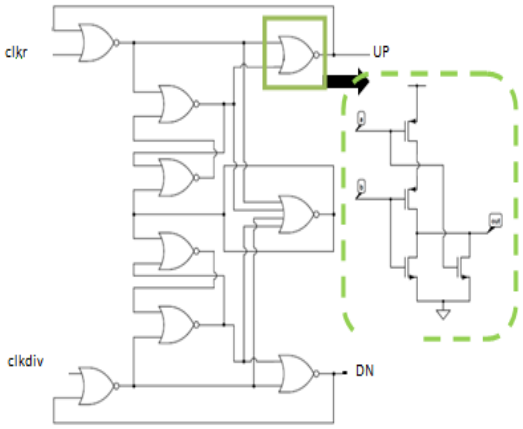

Figure 2. Phase frequency detector using NOR gates

C. Charge Pump

Charge pump is the second block of the PLL that responds according to the output error signal of the PFD. The charge pump (CP) is driven by the PFD to generate current pulses that add or remove charge from the loop filter capacitor [7]. Charge pump consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs. Fig. 3 shows that the circuit has three states. If QA=0, QB=0, then both switches are off and output voltage remains constant. If QA=1, QB=0, then current through the PMOS branch charges the capacitor. Conversely if QA=0, QB=1, then current through the PMOS branch discharges the capacitor. One of the requirements for an effective charge pump is equal charge/discharge current at any charge pump output voltage [1]. The currents through the PMOS branch and NMOS branch are made to be nominally equal.

The current equation shown in (1) is used to design the current source in the charge pump. Proper transistor sizing is carefully designed to avoid current mismatch.

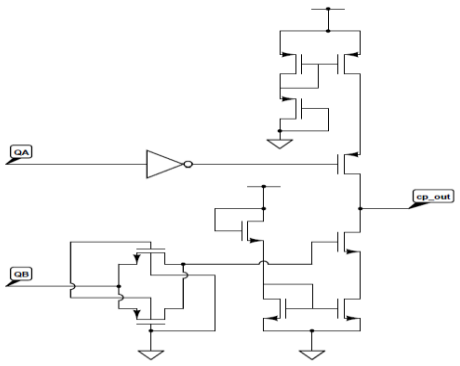

Figure 3. Charge pump schematic with pass gate

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{DSAT}^{\ 2} \quad (1)$$

D. Voltage Controlled Oscillator

A voltage-controlled oscillator is an electronic oscillator designed such that its oscillation frequency is controlled by a voltage input. For the PLL, the charge pump voltage controls the oscillation frequency of the VCO.The most popular type of the VCO circuit is the current starved voltage controlled oscillator. Unlike LC oscillators which contain inductors, the current starved VCO is relatively easy to implement in IC design.

Testing different VCO circuit, a ring VCO design was chosen for this PLL considering the above mentioned advantages fit for minimum chip area PLL. The circuit has 5 numbers of stages. It is important that the number of stages must be odd in order to oscillate. The schematic of the current starved VCO is shown in Fig. 4.

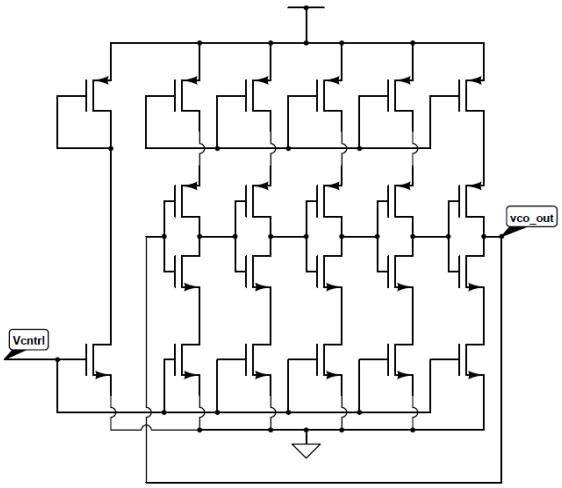

Figure 4. Current starved voltage controlled oscillator

E. Divide-by-64 Frequency Divider

The Frequency divider for this project is designed using the pseudo-NMOS logic instead of the TSPC divider. The TSPC divider and the conventional static logic cannot achieve frequency division since the input to the divider is a sinusoidal signal coming from the VCO. Fig. 5 shows the cascaded divide-by-2 frequency divider. Since the goal is to divide the VCO frequency to 64, the number of cascaded divide-by-2 frequency divider must be 6 (2n=64, where n=6).

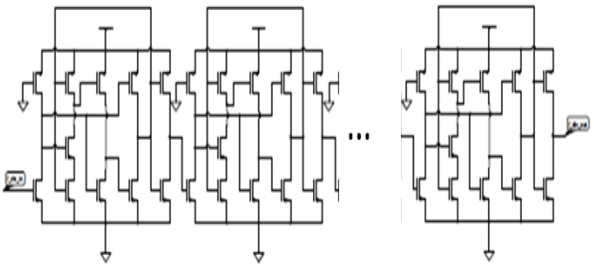

Figure 5. Divide-by-64 frequency divider

As the pseudo-NMOS logic is a rational logic, care must be taken on the aspect ratio between NMOS and PMOS transistors. By calculating NMOS and PMOS characteristics, the ratio of M_{n1} and M_{p1} can be expressed in (2) and (3).

$$\mu_n C_{OX}(\frac{W}{L})_n(V_{\max}-V_{tn}-\frac{V_{OL}}{2})V_{OL} \tag{2}$$

And which is also equal to,

$$=\frac{u_n C_{OX}}{2}(\frac{W}{L})_p(V_{dd}-V_{tp})^2 \tag{3}$$

For M_{n1} and M_{p1}, its ratio is designed so that the voltage of logic level "0" is smaller than the threshold voltage of NMOS transistors V_{tn} [8]. For the open loop voltage, the design was driven by (4).

$$V_{OL}=(V_{\max}-V_{tn})\left[1-\sqrt{1-\frac{u_p(W/L)_p(V_{dd}-V_{tp})^2}{u_n(W/L)_n(V_{\max}-V_{tn})^2}}\right]\le V_{tn} \tag{4}$$

The overall design of the VCO centered on the designing of the appropriate ratio between NMOS and PMOS transistors. For the general design, the sizing of the transistors was based on (5).

$$\frac{(W/L)_p}{(W/L)_n}\le\frac{u_p(V_{dd}-V_{tp})^2}{u_n(V_{\max}-V_{tn})^2}\left[1-\left(\frac{V_{\max}-2V_{tn}}{V_{\max}-V_{tn}}\right)^2\right] \tag{5}$$

III. Simulation Results

The proposed PLL design was simulated and implemented using TSMC 0.18um CMOS technology process with Synopsys Custom Designer tool. All blocks in the design was individually evaluated through series of testing and debugging until the design specifications were met.

A. System and Blocks Simulation

Fig. 6 shows the post-simulation of the charge pump responding when clkref leads clkdiv resulting to increasing voltage and responding when clkref lags clkdiv resulting to decreasing voltage inputted to the next block VCO. On the other hand, Fig. 7 shows the sub-circuit of pseudo-NMOS divide-by-2 frequency divider post-simulation result. It can be seen that for a 640 MHz frequency, the output of the divider is 640/2=320MHz.

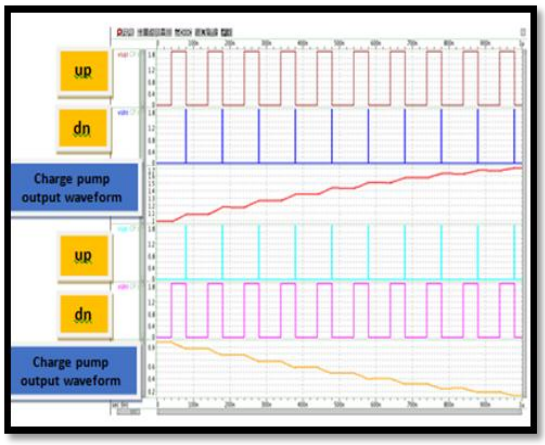

Figure 6. Charge pump post-simulation

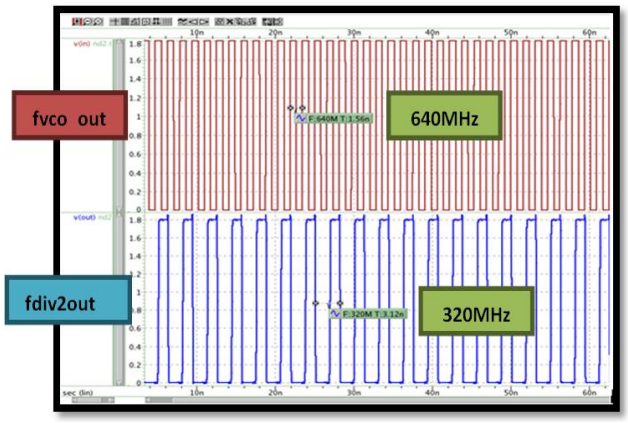

Figure 7. Frequency divider post simulation result

The implemented layout for the divide-by-64 divider is shown in Fig. 8. It can be seen that for a 640 MHz frequency, the output of the divider is 640/64=10MHz, where 10MHz is the reference frequency. Since the goal is to divide the VCO frequency to 64, the number of cascaded divide-by-2 frequency divider must be 6 (2^n=64, where n=6).

The overall PLL circuit is designed thoroughly using analog and digital techniques to achieve the desired specifications. The TT corner post-simulation waveform of the overall PLL is shown in Fig. 9.

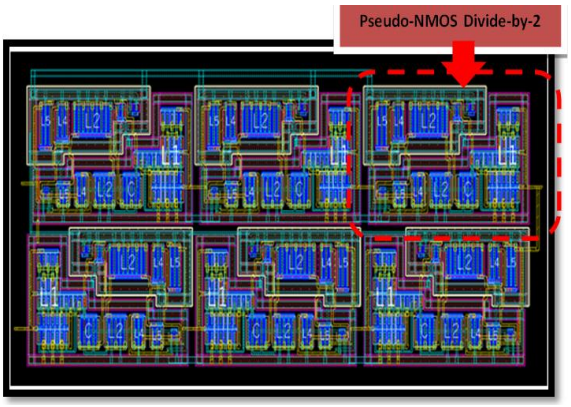

Figure 8. Divide-by-64 frequency divider overall layout

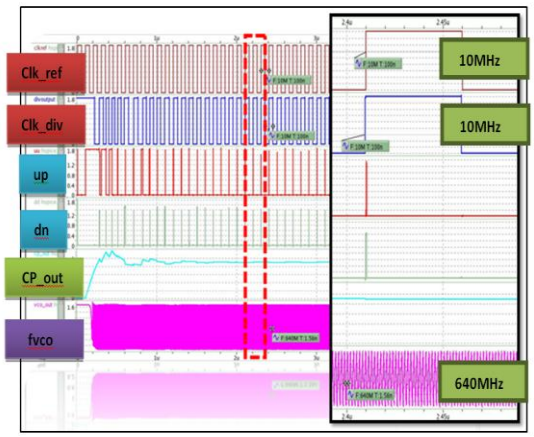

Figure 9. PLL post-simulation at TT corner

Also, in Fig. 9 shows that at TT corner, the settling time was around 2.25 µs which is faster than 3 µs based on the specifications. At approximately 2.25 µs to infinity, the PLL output frequency which is expected to be 640 MHz was constant. It can also be seen that at this time, the reference frequency labeled as clkref is in-phase with the divider frequency labeled as clkdiv. This means that the phase frequency detector will now detect no errors. The reset pulses present in "up" and down" waveforms have approximately equal values. Thus, when the loop was locked, makes the charge pump current relatively idle.

The Monte Carlo analysis for process variation test was also realized in this paper as shown in Fig 10. It was found out that for 30 iterations have a phase shift of 460p which is negligible. Also, the frequencies of the 30 iterations were still within the bandwidth of operation of Continuous-time Sigma –Delta ADCs.

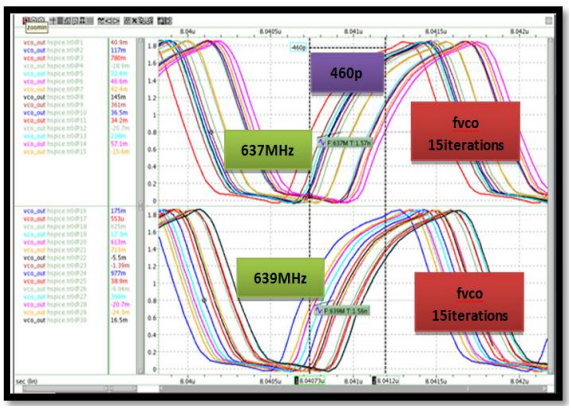

Figure 10. Iterations test result of Monte Carlo analysis

Shown in Fig. 11 is the overall layout of the proposed PLL design with on-chip filter with a total area of 0.2049 µm^2.

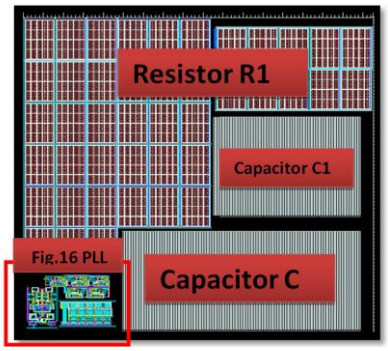

Figure 11. PLL layout with on-chip filter

B. Performance Comparison

The proposed research has an edge over two parameters namely lock-in time and chip area. The fast lock-in time of the proposed PLL has a significant importance since high speed ADCS today have clock rates of more than 10Msps. An acceptable lock-in time for fast-locking PLL is around 3.78us [15]. This work has a lock-time of around 2.5us which is an acceptable value for the lock-in time of ADC clock generator. However, a very fast clock of around nanoseconds settling time is not also desirable because it brings more spurs and noise into the PLL dynamics. In terms of chip area, minimum rule

was observed in the layout design to achieve minimum chip-area stated in the summary table above. A smaller chip area is desirable in any IC layout. It will not only require extremely small silicon die size but will also consume very little power with very little heat dissipation.

TABLE I. DESIGN SPECIFICATION SUMMARY AND COMPARISON

Parameter	[15]	[14]	Proposed Research
CMOS Process	0.18 um	0.18 um	0.18 um
Reference frequency	2 MHz	64 MHz	10 MHz – 11 MHz
Loop Bandwidth	-	0.4 MHz	1MHz
I_{CP} (Charge Pump Current)	20 uA	-	77 uA
Output Frequency Range	2.4 GHz	2.368 GHz -2.496 GHz	640 MHz – 704 MHz
Lock-in time	27 us	20 us	2.5 us
Division Ratio	15/16 dual modulus	64 integer-n	64 integer-n
Chip Area	1 x 2 mm^2	1.6 x 1.3 mm^2	0.2049 um^2 (On chip filter) 8.3393 nm^2 (Off- chip filter)

IV. CONCLUSION

This study completes the design of a 10-MHz reference input Phase Locked Loop suitable for Continuous-Time Sigma-Delta ADC that operates with 640 MHz clock frequency using TSMC 0.18um 1P6M CMOS technology process. The desired output frequency which is 640 MHz is achieved on all corners and is within 640 ± 5% with a lock-in time of 2.5 us. The design of phase frequency detector achieved a small dead zone which increased accuracy and solved the current mismatch problem in terms of phase error detection. The design of single-ended charge pump had a low current mismatch and lesser skew between the not-up (up') and down (dn) inputs using pass gate circuit. The design of divide-by-64 frequency divider avoided delays and loading effects carefully sizing the W/L of each MOS.

ACKNOWLEDGMENT

The authors wish to thank DOST-ERDT Eye-C Program for the research grant in providing the industry standard IC design tools. Special thanks to Synopsys engineers for the technical support.

REFERENCES

[1] Terlemez, "Oscillation control in CMOS phase-locked loops," Ph.D. dissertation, Georgia Institute of Technology, Georgia, USA., 2004.
[2] R. S. Yazdi, "Mixed signal design flow," M.S. thesis, University of Waterloo, Ontario, Canada, 2001.
[3] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," Institute of Electrical and Electronics Engineers (IEEE), *Journal of Solid-State Circuits*, vol. 41, no. 2, p. 433, February 2006.
[4] B. Razavi, *Design of Analog CMOS Integrated Circuits*, International, New York: McGraw-Hill, 2001, ch.15.
[5] H. Johansson, "A simple precharged CMOS phase frequency detector," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 295-299, Feb. 1998.
[6] H. Lee, T. W. Ahn, D. Y. Jung, and B. H. Park, "Scheme for no dead zone, fast PFD design," *Journal of the Korean Physical Society*, vol. 40, no. 4, pp. 543-545, April 2002.
[7] O. Kazanc, "High frequency low-jitter phase-locked loop design," *Engineering Project Report*, Yeditepe University, 2008.
[8] Y. S. Tak, "A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers," Master thesis, The Hong Kong University of Science and Technology, 1999.

Jefferson A. Hora received his bachelor degree in Electronics and Communications Engineering from the Mindanao State University-Iligan Institute of Technology (MSU-IIT), Philippines, in 2002 and his M.S. in Electrical Engineering major in IC Design from National Taipei University, Taiwan, in 2009. He has been an IC Design Engineer in Service & Quality Technology Co.,Ltd, Taipei, Taiwan from 2009-2010. Recently, a faculty member as Asst. Professor of MSU-IIT since 2010, and is a faculty affiliate and adviser of the Microelectronics Laboratory. His research interest focuses in power management IC, RF-DC converter, analog IC, FPGA design and prototype.

Meriam Gay Bautista received her bachelor degree in Electronics and Communications Engineering from the Mindanao State University-Iligan Institute of Technology (MSU-IIT), Philippines, in 2008 and her M.S. in Electrical Engineering major in IC Design from National Taipei University, Taiwan, in 2013. Recently, she is an Asst. Professor in the Department of Electrical, Electronics and Computer Engineering in MSU-IIT. Her research interest includes power electronics design, power management IC, DC-DC converter, analog IC, LED Driver and FPGA design and Implementation.

Christina A. Garcia received her bachelor degree in Electronics Engineering from thMindanao State University-Iligan Institute of Technology (MSU-IIT), Philippines in March 2013.

Stella Sofia Sabate received her bachelor degree in Electronics Engineering from the Mindanao State University-Iligan Institute of Technology (MSU-IIT), Philippines in March 2013.