Overstress-Free Charge Pump White LED Driver

Allenn dela Cerna Lowaton
MicroLab, EECE Dept., Mindanao State University–Iligan Institute of Technology, Iligan City, Philippines
Email: allenn.lowaton@g.msuiit.edu.ph

Hong-Yi Huang
NICS Lab, GIEE, National Taipei University (NTPU), New Taipei City, Taiwan
Email: hyhuang@mail.ntpu.edu.tw

***Abstract*—This paper presented a white light emitting diode (LED) driver that utilized charge pump in boosting the input voltage. The output voltage had been made sure that it was sufficient enough to overcome the forward voltage of the LED as well as provide voltage headroom for the transistors in every LED channel branch. The charge pump and its peripheral circuit, the clock booster circuit, do not suffer from gate-oxide overstress. Gate oxide overstress arose when the potential difference of a certain junction of a transistor exceeded the supply voltage. Moreover, this design can accommodate four (4) LEDs arranged in parallel. In comparison with the other DC-DC converters such as buck and/or boost, this work does not utilize an inductor. The non-utilization of inductor has offered an advantage in terms of lesser board area consumption and minimal height. The test chip was implemented using 0.35 µ m 5V 2P4M CMOS process. The chip area was measured to be 2350.05 µ m x 2496.70 µ m with an efficiency of 51%.**

***Index Terms*—overstress, non-overstress, charge pump, white LED driver**

I. Introduction

White light emitting diodes (LEDs) are being used nowadays in digital cameras, PDAs and LCDs among others. It is characterized by pollution-free, long life span (work time can be achieved 100,000 hours) and resistant to vibration and shock. It is a popular choice for background lighting and illuminations of consumer products. Compared with the commonly used CCFL (Cold Cathode Fluorescent Light), it requires less power and space [1]-[3]. However, its forward voltage drop is high. Typically, white LED has higher forward voltage at around 3.1 volts to 4.0volts as compared with other the LED colors. The intensity of illumination is determined by the average current through the white LED. Charge pump, a switched capacitor DC-DC converter will provide the needed current as well as the voltage for the white LEDs [4]. Shown in Fig. 1 is the schematic diagram of High Efficiency Current Regulated Charge Pump for a White LED Driver [5]. This system has one LED load. It has an output voltage produced by the pumping action of the flying capacitor and the charge transfer of the load capacitor. Unfortunately, this circuit suffers from gate-oxide overstress. When the flying capacitor is pumped higher than V_{DD}, the CK_2 will be at low level, thus, a junction potential higher than V_{DD} exists at gate to drain of M_{P2}.

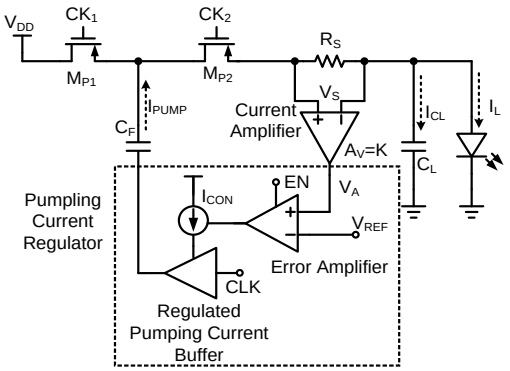


Figure 1. Schematic diagram of high efficiency current-regulated charge pump for a white LED driver

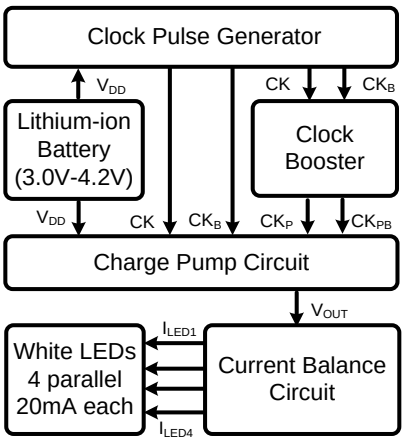


Figure 2. Functional block of the proposed charge pump white LED driver

Shown in Fig. 2 is the proposed overstress-free charge pump white LED driver. The motivation of this work is to provide a white light emitting diode (LED) driver that can accommodate 4 parallel LED outputs. Additionally, this work will utilize a charge pump that is free from the gate oxide overstress. Not a single power MOS switch in the charge pump circuit and its peripheral circuits will experience an overstress as well as latch-up.

Manuscript received December 5, 2013; accepted March 11, 2014.

doi: 10.12720/ijeee.2.4.270-275

White LED has a higher forward voltage as compared with other LED colors. Most supply batteries are sometimes too low for powering up white LEDs, a boost converter is usually needed. Inductors are employed in most DC-DC converters (i.e, buck, boost, etc.) in its operations. Unfortunately, not all applications can afford the presence of inductor in the design. Inductors consumed a considerable area which is a hindrance to product size minimization. Products are now getting thinner which is another reason to avoid inductor utilization in the design.

Charge pump, instead of having an inductor as a storage device, utilizes switches and capacitors in transferring charges from the input to be delivered at the output [6]-[11].

In this paper, Section II reviews the conventional design of the clock boost circuit as well as the charge pump. Section III presents the design including the operations and the schematics of the overstress-free charge pump white LED driver. Experimental results have been presented in Section IV. Lastly, Section V presents the conclusions.

II. Conventional Design of Clock Booster and Charge Pump

Fig. 3 shows the conventional clock booster design [12], [13]. The main purpose of this circuit is to produce clock signals, CK_P and CK_{PB} which will swings from 0 to $2V_{DD}$, alternately. Fig. 4 shows the conventional charge pump circuit. Fig. 5 shows the clock signals CK, CK_B, CK_P and CK_{PB}. CK and CK_B are clock signals produced from an internal clock generator circuit.

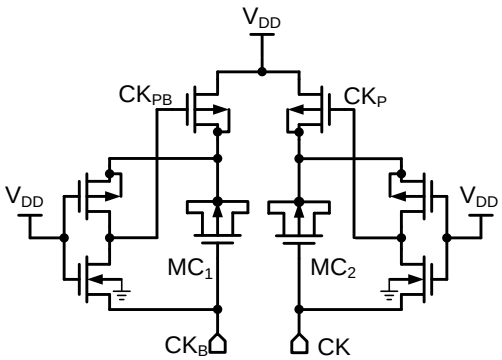


Figure 3. Conventional clock booster circuit

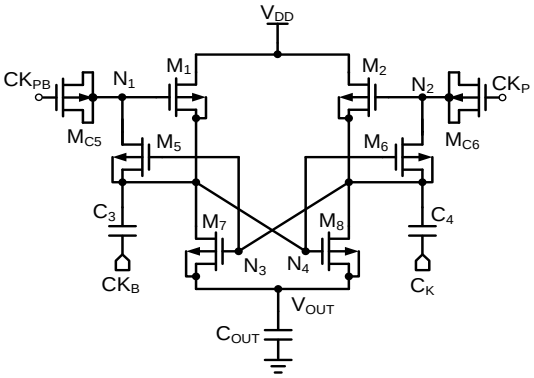


Figure 4. Conventional charge pump circuit

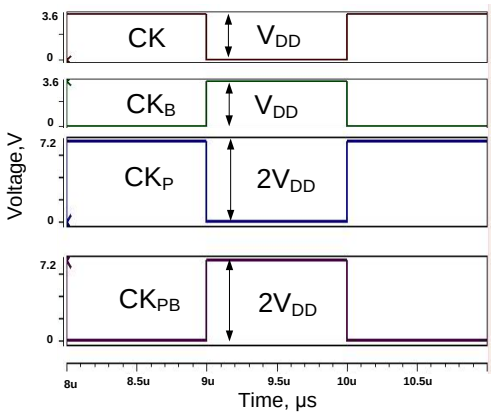


Figure 5. Clock signals: CK, CKB, CKP and CKPB

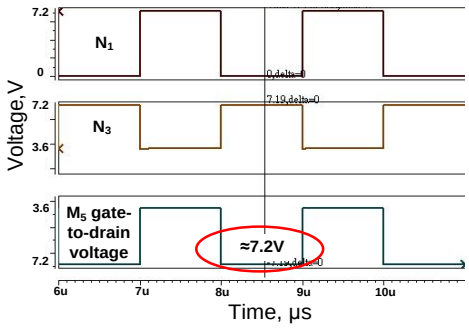
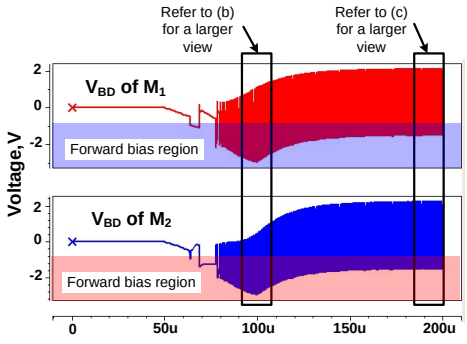


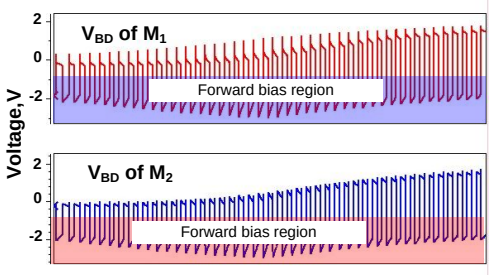
Figure 6. Gate overstress occurs in gate-to-drain junction of M5

At the same instant, N_3 will be at V_{DD} and N_2 will be at zero level which will turn ON M_2, M_6 and M_7 and will charge the capacitor C_4. Moreover, N_1 will approach $2V_{DD}$ which will cause the M_1 to be turned OFF

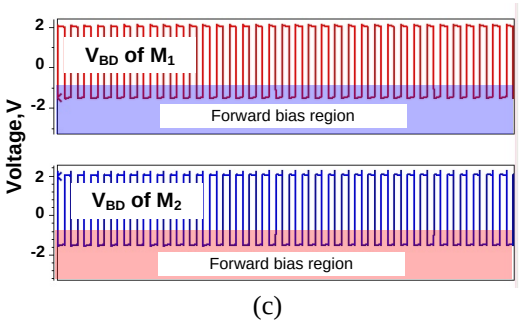
A problem arises when at a certain instant the CK_{PB} is at its low (0) level. At this instance, the node N_1 will be at zero level while the node N_3 is at its $2V_{DD}$. Clearly, a junction potential of $2V_{DD}$ can be seen in the gate to drain (V_{GD}) of M_5 as shown in Fig. 6.



(a)



(b)



(c)

Figure 7. Bulk to drain junction voltages (VBD) for M1 and M2 in conventional charge pump: (a) Transient and steady state, (b) Transient and (c) Steady state

Fig. 7 shows the bulk to drain voltages of the transistors M_1 and M_2 in the conventional charge pump shown in Fig. 4. The charge pump was connected to an output which consists of four (4) white LEDs that draws in a total of 80mA output current. An obvious concern regarding latch-up has been detected on this case. Transistors M_1 and M_2 are PMOS so it is expected that bulk to drain voltages must be positive, meaning, the bulk should always be higher than the drain. Apparently, from Fig. 8, it shows that there exists a problem on latch-up that needs to be addressed. It should be avoided that the bulk to drain junction of a PMOS be in a forward bias. In the event that it will become forward biased, a huge amount of leakage current will flow through it which is detrimental to the circuit operation and could cause damage. From Fig. 7(b), latch-up problem is at its peak and most severe during the transient period. Eventually during the steady state phase, latch-up still exists and it can be observed from Fig. 7(c).

III. Proposed Overstress-Free Charge Pump, Clock Booster and White LED Driver

Fig. 2 shows the functional block of the proposed overstress-free charge pump white LED driver. The major blocks that comprise the whole system are the following; clock generator, clock booster circuit, the charge pump or pump circuit and the current balance circuit. The Lithium-ion (Li-ion) battery [14] will provide the supply voltage for the whole system. It ranges from 3V to 4.2V. The clock pulse generator shown in Fig. 12 will provide the needed clock pulses for the charge pump circuit operations. Clock booster circuit also known as clock doubler provides a higher than V_{DD} ($2V_{DD}$ in fact) to the charge pump circuit to increase its pumping efficiency. The charge pump will basically increase the output voltage from the supply voltage. Ideally, output voltage will be twice the input voltage on no-load condition. Parasitic capacitances, power MOS "on" resistances, $R_{DS\ (ON)}$ will prevent the charge pump from achieving that ideal output voltage. The output voltage of the charge pump increases as the input voltage increases. The output voltage will provide the needed voltage headroom to overcome the forward voltage of the LED as well the needed drain to source voltage of the current mirrors. Current balance circuit, shown in Fig. 13, contains the voltage-to-current (V-I) converter, which will produce the reference current, I_{REF}, and the current mirrors that will multiply the current I_{REF} by two (2) and then by five (5) times. A high accuracy external resistor will provide the I_{REF}. The LED branches of the current balance circuit receive its supply from the output voltage of the charge pump.

Shown in Fig. 8 is the proposed clock booster circuit. To avoid the problem of overstress [15] being shown in Fig. 6 for the transistor M5 and transistor M6 (graph not shown), CK_{PB}, and CK_P now swings from V_{DD} to $2V_{DD}$ instead of from 0 to $2V_{DD}$ in the conventional design. Fig. 9 shows the pertinent signals from the proposed clock booster circuit.

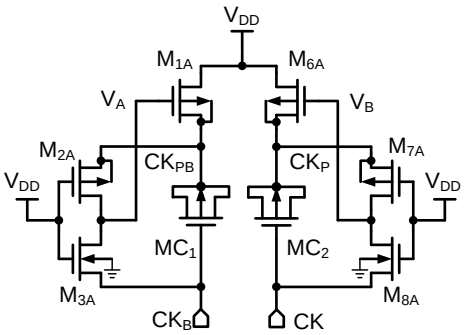


Figure 8. Proposed clock booster circuit

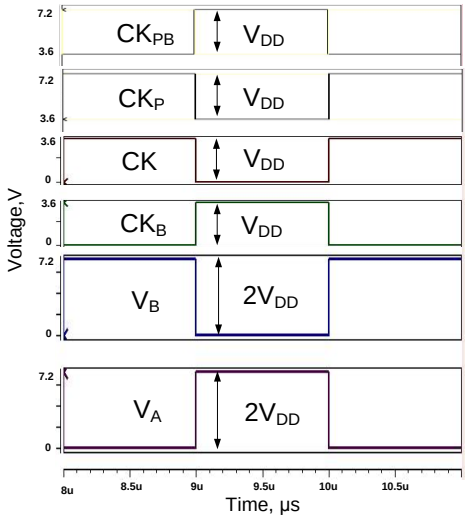


Figure 9. CK, CKB, CKPB,CKP, VA and VB signals

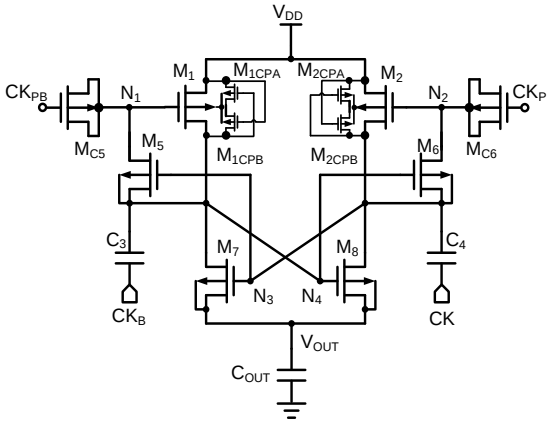


Figure 10. Proposed charge pump circuit

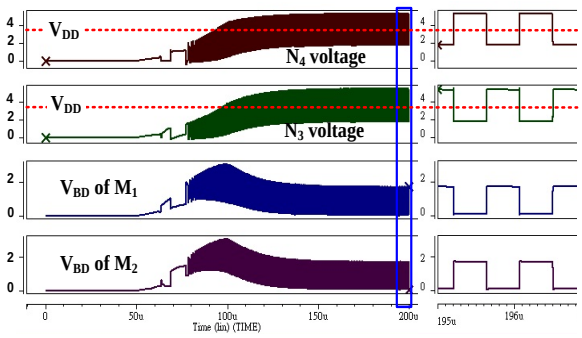


Figure 11. VBD of M1 and M2 and potentials of nodes N4 and N3

Fig. 10 shows the proposed charge pump circuit. The source nodes of power MOS switches M_1 and M_2 are connected to the V_{DD}. Moreover, MC5 and MC6 are MOS capacitors instead of PIP capacitors in order to save area during layout.

Fig. 11 shows those nodes N_4 and N_3 which happens to be the drain of power MOS switches M_1 and M_2, respectively swings lower than their sources which are connected at the V_{DD} . The nodes N_4 and N_3 are connected to the V_{OUT} via the transistors M_7 and M_8, respectively. Due to the combined effects of lower V_{GS} of switches M_1 and M_2 as well the higher output current demands at the output, the nodes N_4 and N_3 would be lowered down to as low as 1.8V. With that, there is a need to ensure that the bulks of M_1 and M_2 are always connected to the highest potential to avoid the problem of latch-up.

Two minimum sized transistors have been placed in transistors M_1 and M_2 to ensure that their respective bulks will be connected to the highest potential so as to avoid any latch-up problems. At this instant, the bulk of M_2 is connected to the V_{DD} rather than on node N_3. At the same instant, the bulk of M_1, although OFF at this point is connected at node N_4 rather than V_{DD}.

This LED driver circuit employed an on-chip clock generator. The clock generator (shown in Fig. 12) is expected to generate a 1MHz clock pulses with a 50% duty cycle. The clock pulse generator is composed of the following: current reference, the ramp generator, comparator, SR latch, static frequency divider and a taper buffer.

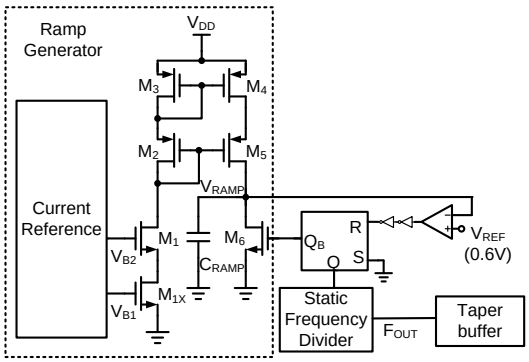


Figure 12. Clock pulse generator

Current balance circuit (see Fig. 13) will provide constant current to every LED connected to one of its four branches [16]. An I_{REF} of 2mA is expected to be produced from a voltage to current converter. An external resistor R will be utilized. Having an external resistor used for producing the I_{REF} will have the following advantages: (1) it won't suffer from unacceptable variation like the on-chip resistor did. Using a high accuracy external resistor will ensure that the produced I_{REF} will have a less variations. (2) It offers more flexibility as far as current that would flow per LED is concerned. Using a non-fixed resistor, one can modify or adjust a needed current per LED. The I_{REF} will then be copied through mirrors M_{P4} and M_{P5}. A high gain two stage op-amp is needed so that nodes N_1 and N_3 will be virtually shorted. Additional capacitor, C_C, for compensation is connected between nodes N_5 and N_3. A bias voltage from current reference is applied to the gate of M_{N2}. The potential at N_4 should be kept as low as possible; just enough for the M_{N3}, M_2, M_3, M_4 and M_5 to operate at saturation region. The mirror comprising M_{N3}, M_2~M_5 will copy the 4mA current and multiply it to 20mA to every LED branch. A high gain two stage op-amp is connected to every LED branch to force the drain voltages of M_2, M_3, M_4 and M_5 be the same with the potential at node N_4. Thus, ensuring that the copied current from the M_{N3} branch to the respective LED branches will be accurately five (5) times multiple of M_{N3} current. The anode terminals of the white light emitting diodes (white LEDs) are connected to the output node of the charge pump. The cathode terminals of LED_1~LED_4 will be connected to the drains of the M_{L1}~M_{L4} respectively.

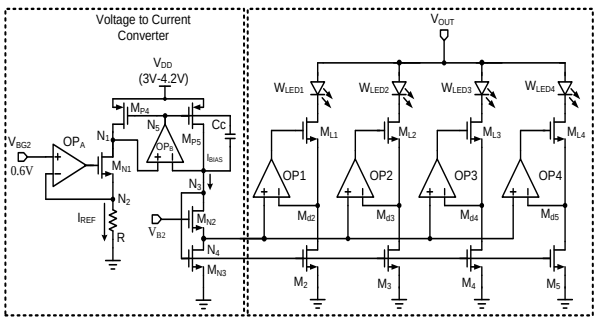


Figure 13. Current balance circuit

IV. Result and Discussion

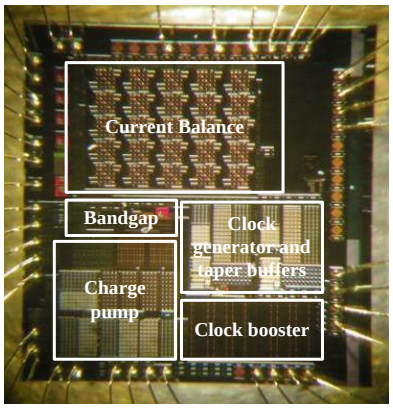


Figure 14. Die photo of the test chip

The proposed overstress-free charge pump white LED driver was fabricated using a 0.35um 5V 2P4M TSMC CMOS process and its photograph is shown in Fig. 14 which has a die size of 2.350mm × 2.497mm.

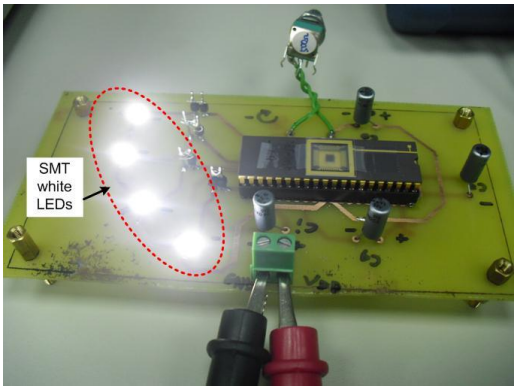


Figure 15. Chip measurement test set-up

Fig. 16 shows the plotted data of the measure current from the individual LED taken at the entire range of the input voltage. The measured results shows the LED currents from the input at 3V (the minimum supply), also when the input is at its nominal input which is 3.6V. Lastly, a measurement on currents when the supply is at its maximum has been provided also. Fig. 16 shows at the entire range of the supply; the chip has able to provide the needed current for all the LEDs. LED1 current is significantly higher than the other three LED currents.

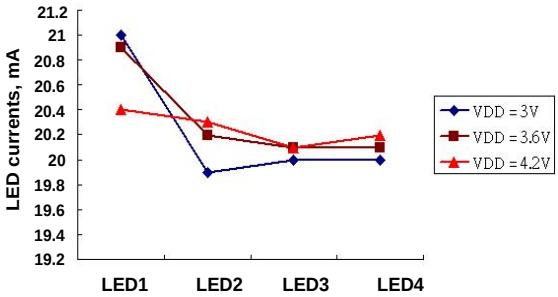


Figure 16. Measured LED currents

Table I shows the comparison table which contains the two previous works [5], [17] and this work. In comparison with [5], this work can accommodate four (4) LEDs arranged in parallel as compared with one LED from the previous work. In addition, this work does not suffer from gate oxide overstress as compared with [5]. Moreover, this work does not utilize an inductor as compared with [17]. The efficiency of the proposed circuit is lower as compared with the compared work. The following are the reasons this work has lower efficiency as compared with [5]. First, the previous work has only 1 LED while the proposed circuit has 4 LEDs in parallel. Second, the output current of the previous work is only 20mA while it's 80mA for the proposed one. Third, to produce the said output current, a huge size of the power MOS switches are needed for the charge pump of the proposed circuit as compared with the previous one. Fourth, the proposed circuit utilized a number of huge taper buffers as compared with the previous work. Lastly, this work has higher pumping frequency as compared with [5]. An optimal frequency of 1MHz is considered. Operating at lower frequency will requires bigger value of flying capacitor which in turns causes the buffer sizes to be increased. This work in comparison with [17] does not need any inductor in its operation. No inductor means less area consumption on the board and offers an advantage in terms of height. As compared with [17], this work offers flexibility and more control on every LED. For series connection, one non-performing LED will cause disruption on the system's operation.

TABLE I. COMPARISON TABLE WITH PREVIOUS WORKS

	T-CASII [5]	ISNE [17]	This work
Input Voltage	2.8V – 4.2V	3.7V - 4.3V	3V – 4.2V
Process	0.5µm CMOS	0.25µm 60V BCD	0.35µm 5V
Converter Type	Charge pump	Boost	Charge Pump
Inductor	No	Yes	No
Operating Frequency	200kHz	1.1MHz	1MHz
Load Current	20mA	60mA	80mA
Number of LEDs	1	12	4
LEDs arrangement	N/A	series	parallel
Gate-oxide overstress	Yes	No	No
Power Efficiency @4.2V	43%	87.7% @ V_{DD}= 4.3V	36%
@3.6V	54%	89.6% @ V_{DD}= 3.7V	41%
@3V	66%	N/A	51%
Chip Size	0.43mm^2	1.4 mm^2	5.867mm^2

V. CONCLUSION

In this paper, an overstress-free charge pump white LED driver has been presented. It can accommodate four (4) white light emitting diodes (LEDs) arranged in a parallel manner. Parallel arrangement allows a multiple of LEDs requiring only an output voltage enough to overcome the LED's distinct forward voltage. Moreover, having LEDs in parallel allows a control over the individual LED currents. This work presented a charge pump together with its clock doubler, the clock booster circuit, free from any gate oxide overstress. Gate oxide overstress is a time dependent concern when it comes to reliability. Circuits and chips with gate oxide overstress in the long run will suffer from operation disruption which will eventually leads to damage. In comparison with the other DC-DC converters such as buck, boost and buck-boost, this work does not utilize any inductor in boosting the input voltage in order to attain a higher output voltage. With this, there is an expected advantage in terms of lesser area in the board implementation. Moreover, this inductor-free white LED driver provides a height advantage. Products nowadays are becoming thinner which means that an LED driver with a minimal height will obviously have an edge.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC), Taiwan for the fabrication of the test chip.

REFERENCES

[1] Reach Technology. (June 2012). CCFL Versus LED Backlighting. [Online]. Available: http://www.reachtech.com/products/backlight/
[2] N. Giamello. (May 2012). LED Backlighting for LCDs: Options, Design Considerations, and Benefits. [Online]. Available: http://www.sharpledlcd.com/resources/LED%20Backlight%20Whitepaper.pdf
[3] Maxim. (June 2012). Why Drive White LEDs with Constant Current. [Online]. Available: http://www.maxim-ic.com/app-notes/index.mvp/id/3256
[4] Maxim. (June 2012). White LED boost converter versus charge pump. [Online]. Available: http://www.maxim-ic.com/app-notes/index.mvp/id/3243
[5] C. H. Wu and C. L. Chen, "High efficiency current regulated charge pump for a white LED driver," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 10, pp. 763-767, Oct. 2009.
[6] F. Pan and T. Samaddar, *Charge Pump Circuit Design*, New York: McGraw-Hill, 2006, pp. 41-120.
[7] V. Vitchev. (June 2012). Calculating Essential Charge Pump Parameter [Online]. Available: http://powerelectronics.com/passive_components_packaging_interconnects/capacitors/power_calculating_chargepump_circuits/index3.html
[8] J. F. Dickson, "On-chip high voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid State Circuits*, vol. sc-11, no. 3, pp. 374-378, June 1976.
[9] T. Tanzawa and T. Tanaka, "A dynamic analysis of Dickson charge pump circuit," *IEEE J. of Solid State Circuits*, vol. 32, no. 8, pp. 1231-1240, Aug. 1997
[10] M. D. Ker, S. L. Chen, and C. S. Tsai, "A new charge pump circuit dealing with gate-oxide reliability issue in low-voltage processes," in *Proc. Int. Symp.Circuits and Syst.*, 2004, pp. I 321 – I324.
[11] J. T. Wu and K. L. Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid State Circuits*, vol. 33, no. 4, pp. 592-597, Apr. 1998.
[12] C. Cruz, C. Filho, and V. Mognon, "A charge pump circuit without gate-oxide overstress for standard CMOS technology and suitable for low power applications," in *Int. Conv. Elect. Electron. Engineers Israel*, 2008, pp. 046-050.
[13] C. Cruz, C. Filho, and J. Lima, " A charge pump without overstress for standard CMOS process with improved current driver capability," in *Int. Conv. Elect. Electron. Engineers Israel*, Dec. 2008, pp. 618-622.
[14] Powerstream. (June 2012). PowerStream Prismatic Li-ion Battery H083448 Data Sheet. [Online]. Available: www.powerstream.com/p/H083448.pdf
[15] M. D. Ker, S. L.Chen, and C. S. Tsai, "Design of charge pump circuit with consideration of gate oxide reliability in low-voltage CMOS processes," *IEEE J. of Solid-State Circuits*, vol. 41, no. 5, pp. 1100-1107, May 2006.
[16] C. L. Chiu and K. H. Chen, "A high accuracy current-balanced control technique for LED backlight," in *Proc. Conf. IEEE Power Electron. Specialists Conf.*, June 2008, pp. 4202-4206.
[17] Y. T. Hsieh, *et al.*, "A high efficiency boost white LED driver for portable electronics applications," in *Int. Symp. Next-Generation Electronics*, Nov. 2010, pp. 13-16.

Allenn dela Cerna Lowaton was born in Lala, Lanao del Norte, Philippines on August 5, 1982. He obtained his degree in Bachelor of Science in Electronics and Communications Engineering at the Mindanao State University – Iligan Institute of Technology (MSU-IIT), Iligan City, Philippines on April 2008 and graduated Cum Laude. He finished his Master of Science in Electrical Engineering major in Integrated Circuits Design at National Taipei University, New Taipei City, Taiwan ROC on July 2012 with a GPA of 4/4. He had worked as a product engineer in Taiyo Yuden Philippines, Mactan Eco-Processing Zone at Lapu-Lapu City, Cebu from December 2008 up to August 2009. Presently, he is a full-time assistant professor at the Electrical, Electronics and Computer Engineering (EECE) Department at MSU-IIT.

Hong-Yi Huang currently is an Associate Professor at the Graduate Institute of Electrical Engineering at National Taipei University, New Taipei City, Taiwan. He obtained his Ph.D. in Electronics Engineering at National Chiao Tung University (NCTU) in Hsinchu, Taiwan. His current research interests include communication circuits, IR readout, high-bandwidth wireless IR transceiver, CMOS RF, embedded memory, low-power/high-speed integrated circuits and systems, bio-circuits and systems.