3rd–Order Dual Truncation 18-Bit Audio MASH 2-1 Delta-Sigma Digital to Analog Converter in 90nm CMOS Technology Implementation

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***Abstract*—A sigma-delta third order dual truncation MASH 2-1 D/A converter with 18-bit input format is successfully implemented in 90nm CMOS technology. This design focuses on the digital implementation of 64x upsampling digital interpolator and third-order delta-sigma MASH architecture. The interpolator is digitally designed by two cascading halfband FIR lowpass filter and the final stage is designed using CIC (Cascaded Integrator-Comb) filter. The third-order delta-sigma MASH modulator is implemented into two parts; these are digital part and analog part. The digital part is successfully implemented using RTL code while the analog part is thru MATLAB for behavioral and Cdesigner for actual implementation. The total area for the digital block is 30339.259853 μm^2 while the total cell area is 25918.75 μm^2 using the TSMC 0.13μm Logic CMOS Technology. Furthermore, the total dynamic power of the circuit (modulator and interpolator) while in operation is 11.1799 μW. With the 3rd-order dual truncation multistage noise shaping technology, SFDR of 110dB and SNR of 115 dB is achieved and its measured harmonics are all below -100dB. The total harmonic distortion of the whole analog block which has a chip area of 681um by 365um is 173m% and with a total power dissipation of 688.279uW.**

***Index Terms*—digital-to-analog converter, 1-bit DAC, 8-bit DAC, dual-truncation, analog lowpass filter, butterworth lowpass filter**

I. Introduction

The world we know today is gradually evolving into a digital-giant; almost everything is desired to perform the required processing in digital domain despite the fact that the real world signals in electronics are analog in nature [1].

There are reasons why the shift from analog to digital processing is being encouraged and implemented today. One of the major reasons is the flexibility of the digital circuits. Signals are represented digitally and can be transmitted without degradation due to noise [1].

Furthermore, because of its improved accuracy, reliability as well as low-cost, high-speed and low-power production compared to analog circuits, digital processing is mostly recommended today. However, in order for the transmitted digital signal to be converted back to its analog nature, ADC or Analog-to-Digital Converter and DAC or Digital-to-Analog Converter is being used. Thus, for these very significant reasons, designing and developing high resolution digital-to-analog converter and analog-to digital converter are given the utmost importance for this digital world to comprehend for the rampaging development of digital evolution. Noise shaping conversion method has become the main technology for high resolution A/D or D/A conversion for use in audio and telecommunications. This method attains high linearity by oversampling and noise shaping, which decreases the quantization noise in the signal band by emphasizing the noise in the out signal band. MASH (Multistage noise shaping) is a technology where theoretically, does not have limit to noise shaping order, thus making it easier to design highly accurate converters [1] [2].

This research about developing a 3rd – order Dual Truncation 18-bit Audio MASH 2-1 Delta-Sigma DAC in 90nm CMOS Technology Implementation aims to serve as a new frontier for high-quality DAC- search for audio application.

II. Design Architecture

The typical Sigma – Delta DAC is comprised of the interpolator, sigma – delta modulator, DAC, and low pass filter, as shown in Fig. 1.

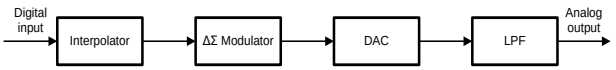

Figure 1. Digital to analog converter system

The general concept of a dual truncation delta-sigma noise-shaping loop structure is shown in Fig. 2[1] [2]. In this approach, the low order modulators, in this case, a second order and a first order modulator, is connected in cascade with its own quantizer. Since it makes use of two or more truncators or quantizers, it uses multiple truncations. The advantage of this method is that lower order modulator is unconditionally stable, thus the stability of the system is guaranteed. Also, the maximum input amplitude can be made almost equal to reference feedback. But this architecture also has disadvantages. It

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requires matching between analog and digital transfer functions and it has a multi-bit output. However, having a multi-bit output is disadvantageous because it needs to be accurately converted in a multi-bit, and hence complex, DAC. [2]

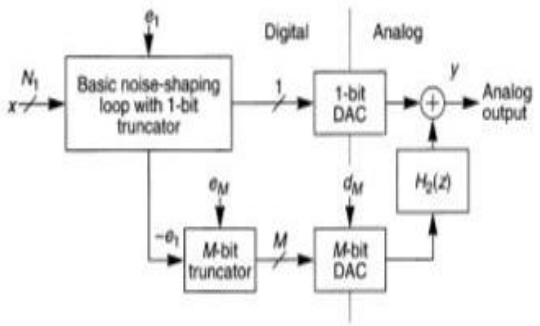

Figure 2. A dual truncation $\Delta\sum$ noise-shaping loop[1]

A. Digital Interpolator Block

Figure 3. Interpolating filter

As shown in Fig. 3, the first stage of the filter is operated at 2 f_S. This stage is used to suppress the odd-order images. The filter design also needs to have flat passband with extremely small gain variation in the 0 to f_B frequency range and a sharp cutoff. [1]

The second stage operates at 4 f_S. Its task is to remove the images between the 3 f_S, 5 f_S and so on. Its cutoff needs to be less abrupt compared to the first stage. After the FIR filters is the sinc filter, which repeats each output sample of the second IF stage 16 times. This results to an OSR of 64. [1]

B. Digital Modulator Block

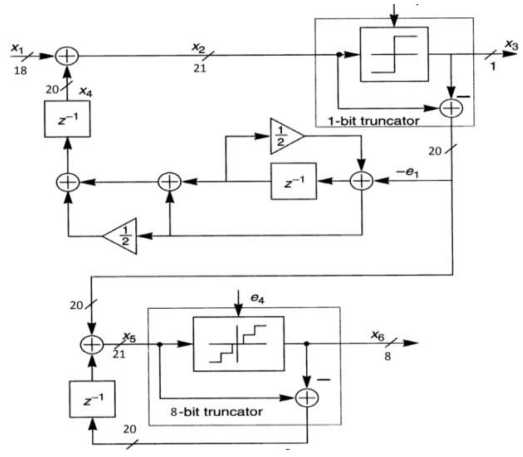

Figure 4. Digital implementation of 2-1 MASH modulator

The M-bit truncator is set to 8 bits to improve the overall output waveform, as well as to improve the signal-to-quantization-noise ratio. Signal-to-noise ratio of 120dB more is achieved when the input signal is 2^{17}. This is where the input signal amplitude is half of 1-bit quantizer output level.

Fig. 4 shows that there are five 18-bit adders in the basic noise-shaping loop and two adders in the correction path. The adder of each quantizer is considered to be a part of the quantizer thus each quantizer has two outputs. The output X_3 of the 1-bit quantizer is simply the MSB of the signal X_2; its integer value is 2^{20}or 2^{-20}. The other output $-e_1$ is the difference between signals X_2 and X_3 and is 20 bits wide. [1] [2]

C. Analog Block

The reconstruction of digital data is implemented using lowpass filter block and DAC that will be discuss further in the next section.

III. Analog Block Implementation

A. 1-BIT DAC

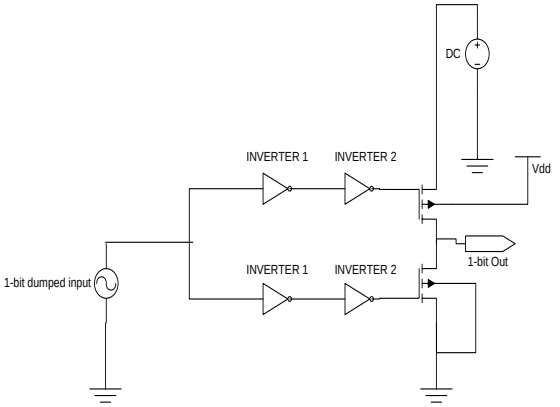

Figure 5. 1-bit digital to analog converter

The input of the 1-bit DAC in Fig. 5 will be dependent on the output of the 1-bit quantizer from the modulator.

B. 8-BIT DAC

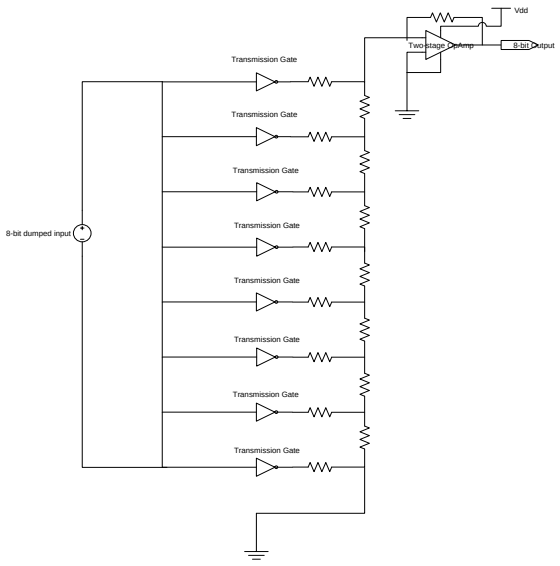

Figure 6. 8-bit R-2R digital to analog converter schematic

Fig. 6 shows the complete block of an 8-bit R-2R Ladder digital-to-analog converter which consist of resistor ladder network and feedback, transmission gate which acts as switch to digital input and operational amplifier which acts as filter and amplifier.

C. Analog Lowpass Filter

To reconstruct the original analog signal, an analog lowpass filter is need. The analog lowpass filter smoothens out the output of the MASH Digital to Analog Converter. The fact that practical DACs output a sequence of piecewise constant values or rectangular pulses would cause multiple harmonics above the nyquist frequency. These are typically removed with the analog low pass filter acting as a reconstruction filter.

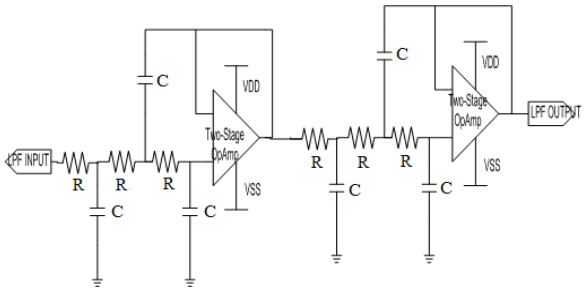

Figure 7. 5-th Order 20 kHz butterworth lowpass filter

Fig. 7 shows 5th Order 20 kHz Butterworth LPF. In this filter, a two-stage operational amplifier will be used. An operational amplifier can either be single-supplied or dual-supplied.

IV. Simulation Results

A. Digital Interpolator

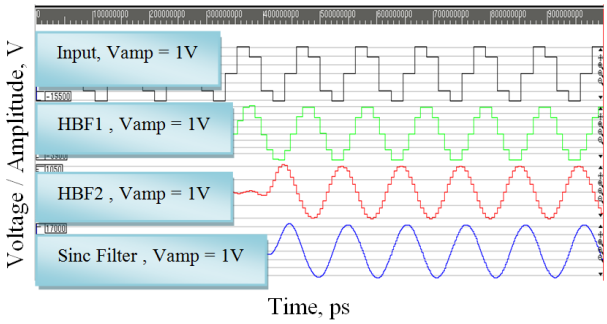

Figure 8. VERILOG compiler simulator result

In Fig. 8 the uppermost waveform is an input signal that is sampled at 48 kHz. Below it is the output of the first half band filter, then the output of the second, and lastly, the output of the sinc filter [3] [4]. The generated waveform from the VERILOG simulator is similar to the behavioral simulation of the interpolator.

B. Digital Modulator

The Fig. 9 shows the output of the interpolator, 1-bit quantizer output, then the 8-bit quantizer output, from top to bottom. In order to verify that the modulator works as expected, the data from the simulation is dumped to MATLABto see if the 1 – bit and 8 – bit quantizer outputs is able to reconstruct the original signal.

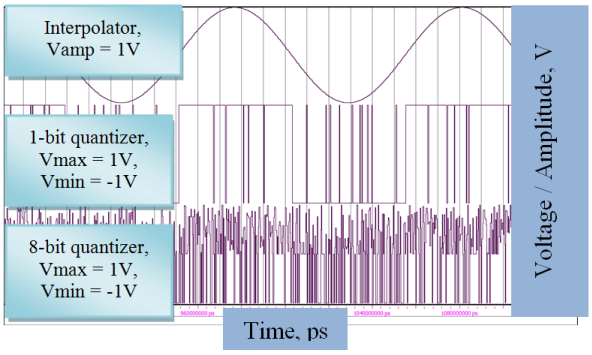

Figure 9. Actual modulator simulation in Xilinx ISE

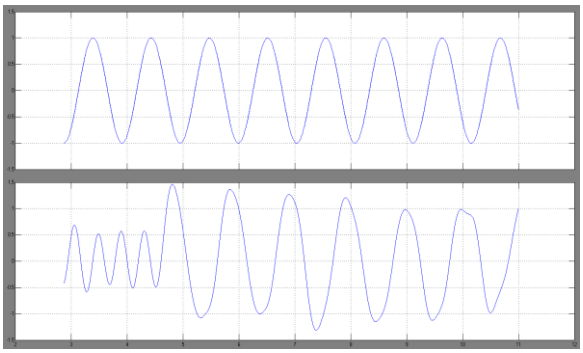

Figure 10. Modulator block Matlab simulation output

From this Fig. 10, a delay is seen. It takes about 0.45 ms for the system to stabilize. This is also due to the interpolator output which possesses a delay, as shown in Fig. 8.

C. 1-BIT DAC

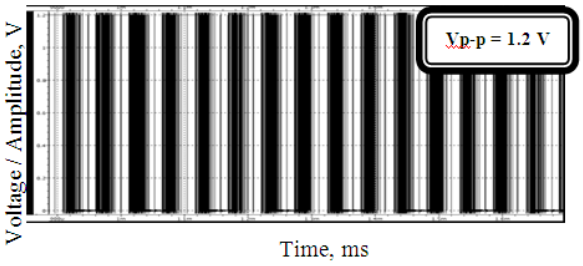

Figure 11. Actual 1-bit DAC output

D. 8-BIT DAC

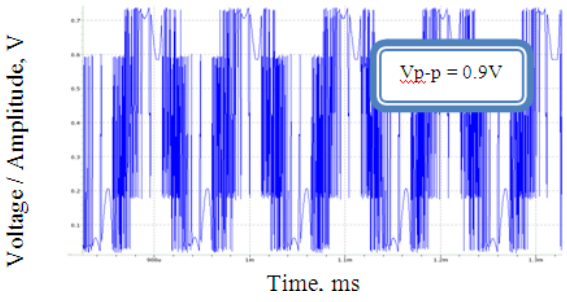

Figure 12. Actual 8-bit DAC output

Fig. 11 and Fig. 12 show an actual output of 1-bit DAC and 8-bit DAC respectively. The input is a piece wise linear function file from the dumped MATLAB output.

E. 1-BIT Plus 8-BIT DAC

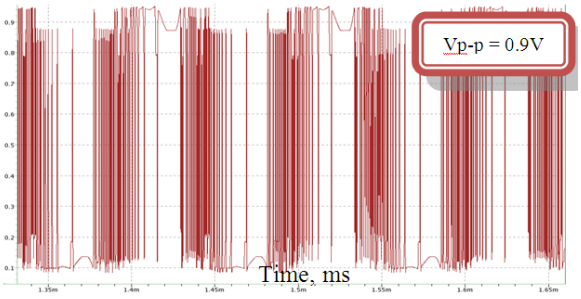

Figure 13. Simulation result of sum of 8-bit and 1-bit DAC

Fig. 13 shows the result of a multi-bit architecture and a multi-stage noise shaping DAC architecture.

F. Analog Lowpass Filter

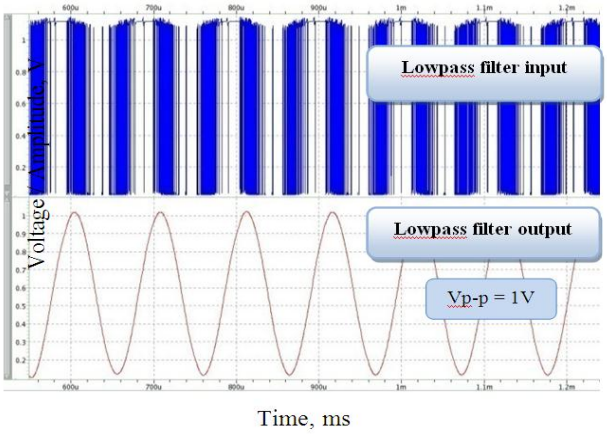

Figure 14. Lowpass filter output with actual (dumped) input

The output waveform of the whole system after the lowpass filter is shown above (Fig. 14). The bottom waveform is the output of the lowpass filter while the top waveform is the output of the sum of 8-bit and 1-bit DAC. The output of the lowpass filter is also the output of the overall integrated analog block; it has the peak-to-peak amplitude of 1V and a period of 104us which shows that the input of the integrated analog block has a frequency of 9.6 kHz.

G. Signal-to-Noise Ratio

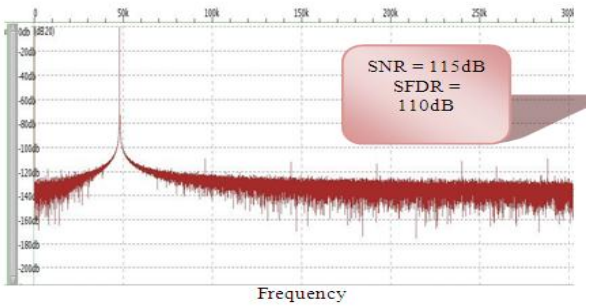

Figure 15. Signal-to-noise ratio of the whole system

The Fig. 15 shows the Signal-to-Noise ratio of the final output of the actual simulation (dumped input) of the whole block with sampling frequency of 48 kHz. The SNR is 115dB which meets the expected SNR which is greater than 100 dB and SFDR of 110dB.

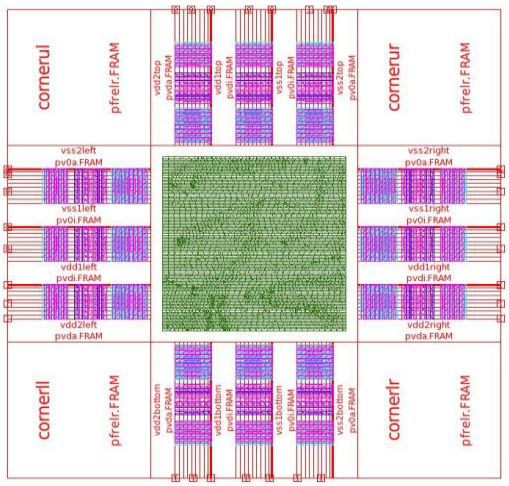

Figure 16. Layout of interpolator and modulator

Fig. 16 shows the layout of the combined interpolator and modulator. This is achieved by using the TSMC 0.13µm Logic CMOS Technology. The total area is 30339.259853 μm^2 while the total cell area is 25918.75 μm^2.

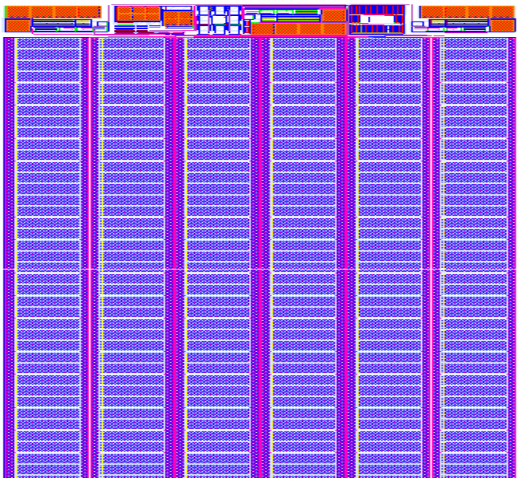

Figure 17. Whole analog block layout

Fig. 17 shows the complete layout for the whole analog block which consist of the layout of summation for 1-bit DAC and 8-bit DAC, layouts of eight transmission gates for the eight digital inputs and sixteen resistors for the R-2R ladder network, a resistor for the feedback, an operational amplifier, a summing amplifier and a reconstruction filter which is a 5^{th}-order Butterworth lowpass filter.

This design of 3^{rd}-order dual Truncation 18-bit Audio MASH 2-1 Delta-Sigma Digital to Analog Converter in 90nm CMOS Technology Implementation has the design specifications in Table I.

TABLE I. DESIGN SPECIFICATIONS

Analog Supply Voltage (AVdd) :	3-3.3V
Digital Supply Voltage (DVdd):	1.2V
Ambient Temperature:	25˚C
Input Sample Rate:	3.072 MHz (64xfs Mode)
Measurement Bandwidth:	48kHz
Word Width:	18 bits
Load Capacitance:	<50pF
Load Impedance:	<47kΩ
Input Voltage HI:	2- 2.8V
Input Voltage LO:	0.4-0.8V
SNR:	>100dB

V. CONCLUSION

An 18 bit audio MASH 2-1 oversampling delta-sigma D/A converter is analyzed and has been successfully implemented. The fundamentals of delta-sigma DACs and special aspects when they are used in audio applications are discussed in detail in different chapters of this paper. Thus, the conclusion and analysis of this research are formulated and summarized as follows:

- Digital interpolator and modulator structure is designed and developed in this research. Two cascading halfband filters and CIC.
- The total area for the digital block is 30339.259853 μm^2 while the total cell area is 25918.75 μm^2 using the TSMC 0.13µm Logic CMOS Technology.
- An efficient 8-bit R-2R ladder DAC and a 1-bit DAC has been designed which undergoes different stability tests.
- A 5^{th} -order 20kHz Butterworth Lowpass filter has been designed and has been put to several tests to measure the specifications and stability.
- A stability issues is guaranteed during implementation of MASH 2-1 architecture. The structure is successfully implemented by combining single stage delta-sigma loops and second-order delta-sigma loop.
- Simulated results are presented and all simulations are based on ideal and actual behaviors. Furthermore, the actual simulation shows that the digital part and analog part is working and is effective since the digital message which is the original code has been reconstructed after passing through the lowpass filter.
- Layout is implemented throughout the whole block and post simulations are conducted and are compared to the pre simulation of the schematic. The results show considerable differences between the pre and post simulations.
- The total power dissipation is 688.279uWatts which is efficient enough considering the technology file being used in the project and compared to commercialized DACs which dissipates greater power.
- The Signal-to-Noise Ratio is shown to be 120dB and the Spurious Free Dynamic Range or SFDR is 110dB which is acceptable for an 18-bit resolution D/A converter.

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