# 3-D Solenoid Inductor Analysis in a 0.13 μm Digital CMOS Technology

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***Abstract*—This paper presents the analysis of a small-area on-chip solenoid inductor using the 0.13μm digital CMOS process. The on-chip solenoid inductor is vertically constructed using metal and via layers with a horizontal scalability. This gives the advantage of occupying a small area due to its 3-D structure compared to a spiral inductor. The electrical characteristics of the solenoid inductor have been analyzed by employing 3-D EM simulation. The proposed equivalent model of the solenoid inductor is introduced to get the insight of the scalability so that the selection of the inductance is simply choosing the number of turns. This small area solenoid inductor can be good candidate for LC type VCO for GHz PLL in the standard CMOS process with saving die cost.**

***Index Terms*—solenoid inductor, Voltage Controlled Oscillator, EM simulation**

## I. Introduction

As the recent remarkable growth in the digital CMOS technology has reached several GHz in the $f_t$ frequency, many studies have been done regarding digitally controlled oscillator (DCO)s operating in the several gigahertz range [1]-[2]. However, the spiral type inductor in the DCOs is still the one traditionally used in RF process and so it suffers from a low quality factor and occupies a large area, impacting upon the low processing cost desired for the digital CMOS process. In addition, circuit designers have to face the challenges in designing the spiral inductor by oneself and take responsibility for its performance.

A solenoid inductor implementation has been studied in [3], which mainly uses micro electro mechanical systems (MEMS) technology. By virtue of the good conductivity of copper, the electroplated inductor has a high quality factor and an inductance of a tenth of nH. [4]. However, the post MEMS processing requires the additional mask steps and increases the processing cost. Prior to 0.13 μm CMOS process, the poor conductivity of Al CMOS process has adapted a thick metallization method of interconnection in order to reduce the series resistance of inductor. For example, in a LC type voltage controlled oscillator (VCO) in 0.18μm RF process, the spiral inductor uses top metal with thickness of 3 μm.

Since CMOS technology has started to adopt Cu metallization below 0.13 μm process, it opens the possibility of implementing a low series resistance inductor in LC type VCO. Unfortunately, the large area planar spiral inductor is still used in the digital CMOS process.

In this paper, a solenoid inductor using metal and via stacking is proposed and its electrical characteristics are evaluated in terms of inductance and quality factor using 3D-EM simulation. In the long run, the solenoid inductor could be used for LC-type VCO in the standard CMOS process. Two types of inductors according to the different dimension have been implemented and measured its characteristics using a HP E4440A. The measured S-parameters were used in analyzing the proposed equivalent lumped model and the parameter optimization.

## II. On-Chip Solenoid Inductor Design

### A. Solenoid Structure

Generally, a spiral inductor is fabricated using the planar CMOS process. Thus, the magnetic flux of the spiral inductor penetrates the substrate with its axis perpendicular to the wafer surface. As a result, the spiral inductor suffers from a low quality factor due to the substrate loss.

On the contrary, the solenoid inductor shown in Fig. 1 is built by metal and via interconnection and moreover, its axis is parallel to the substrate. This makes the solenoid inductor less susceptible to the substrate losses due to the eddy current. In Fig. 1, the bottom plate is represented by M1 and top plate by M6. The posts are

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connected between the top plate and the bottom plate by Vias (V1-V5).

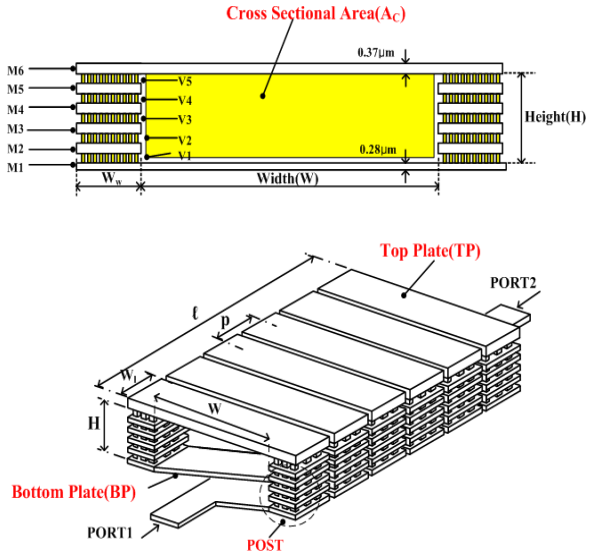



Figure 1. A structure of the solenoid inductor.

In general macro-scale, the solenoid inductance is expressed in terms of its dimension.

$$L_S = \frac{4\pi\times10^{-7}\times N^2\times A_c}{N\times p} \quad (1)$$

where $N$ is the number of turns, Ac is the cross-sectional area that the magnetic flux is crossing; $p$ is the pitch between each turn.

Since the cross area (Ac) is the width (W) and the height (H) and the maximum height is limited by the process technology, the inductance is proportional to the width and the number of turns as Eq. 2.

$$L_S \propto W \times N \quad (2)$$

The series resistance (Rs), which directly affects the quality factor by $Q = {\omega \cdot L_s}/{R_s}$, will be increased due to the skin effect [5] and the proximity effect with an increasing frequency. As the proximity effect from the conductor moves farther from the adjacent turns, it can be neglected and so the approximation of Rs is given by;

$$R_s = R_{dc}\frac{t}{\delta\cdot(1-e^{\frac{-t}{\delta}})} \quad (3)$$

$$R_{dc} = \rho_{\square}\cdot\frac{2N(W+2W_w)}{W_l} \quad (4)$$

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \quad (5)$$

where $t$, $W_W$ and $W_l$ represent the metal thickness, the post width and the post length, respectively; $\rho$, $\mu$ and $f$ are the resistivity of the copper, the permeability of the air and the operating frequency, respectively. Considering a greater than 5GHz operating frequency, the skin depth is about 0.94μm which is larger than the top metal thickness 0.9μm in 0.13μm digital CMOS process. Thus, ignoring the skep effect, the series resistance, $Rs$ becomes 1.2 $R_{dc}$. Then Rs can be rewritten as

$$Q = 0.833\frac{\omega\cdot L_S}{R_{dc}} \quad (6)$$

In addition, the width of the solenoid (W) is larger than the post width, ($W_W$) and length ($W_l$). Rdc is proportional to N • W. the quality factor is also only inversely proportional to N • W as;

$$Q \approx \frac{1}{W\cdot N} \quad (7)$$

From the Eq. (2) and Eq. (7), we can extract the design parameters of the solenoid inductor as W and N. These parameters give insights to the rule of thumb of design the solenoid inductor. However, it is not sufficiently explain the exact performance for circuit simulation when it comes to, for example, LC type VCO using the solenoid inductor so that the EM simulation is required.

### *B. EM Simulation*

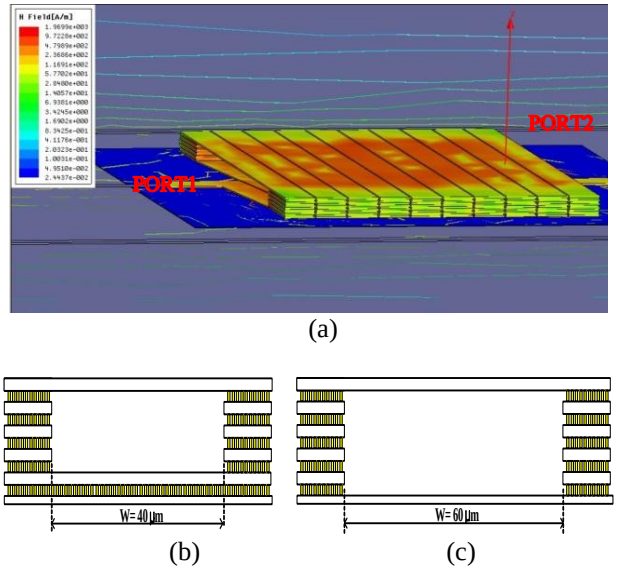



Figure 2. (a) HFSS simulation result of solenoid inductor (b) Design Type I: W=40μm, and (c) Type II: W=60μm.

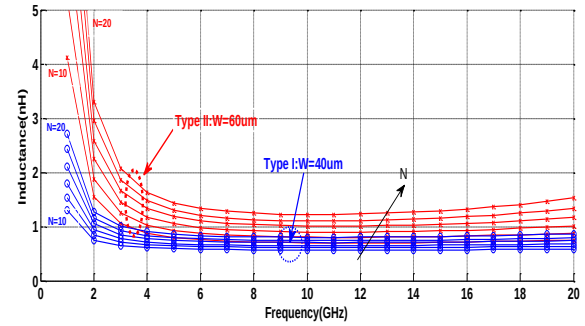
Fig. 2(a) shows the EM simulation result, H-field from HFSS [6] simulation. For EM simulation, the input excitation is applied to PORT 1 and PORT 2 terminals. The EM simulation gives also its result in S-parameters. Then, the inductance of quality factor of the inductor is determined uniquely from the Y-parameters converted from the S-parameters by;

$$L_{11} = \frac{-1}{2\pi\cdot f\cdot im(Y_{11})}, Q_{11} = \frac{im(Y_{11})}{Re(Y_{11})} \quad (8)$$

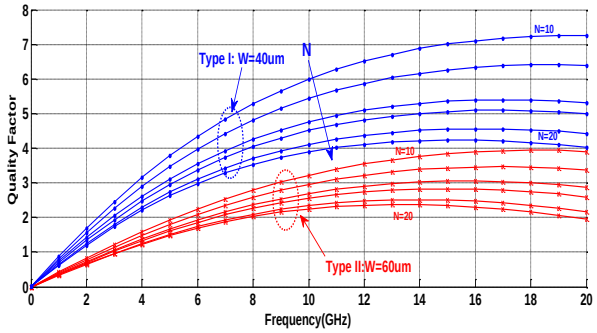
where $L_{11}$ and $Q_{11}$ are the inductance and quality factor looking at port1, im($Y_{11}$) and Re($Y_{11}$) are the imaginary part and real part of $Y_{11}$.

The proposed solenoid inductors have two types according to the width (W), type I: 40 μm (Fig. 2(b)) and type II: W=60μm (Fig. 2(c)). Notably, type I has bottom plates stacking metal1 (M1) and metal2 (M2) in order to reduce the series resistance. Each type has a varied number of turns (N) from 10 to 20 by even number increments. Fig. 3 shows the results of the inductance ($L_{11}$) and quality factor ($Q_{11}$) from the HFSS simulation.

From Fig. 3(a), the inductance is range from 0.6 to 0.9 nH for type I and from 0.8 to 1.5 nH for type II and the quality factor has 7 and 4 in maximum for type I and type II respectively. It is clear that the inductance increases according to Ws from 40 μm to 60 μm and Ns from 10 to 20 and the quality factor decreases according to W and N as Eq. (2) and Eq. (7). Since the quality factor is directly affected by the total length, that is Ls, the type I inductor with stacked bottom plate, has a higher quality factor than type II.



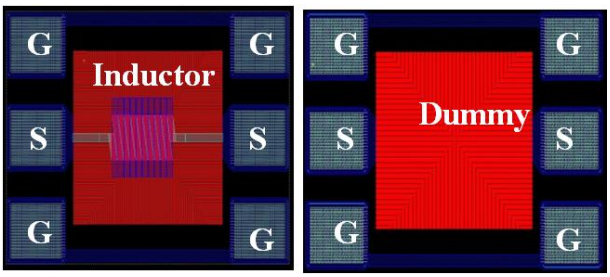

(a)




(b)

Figure 3. (a) Inductance and (b) Quality factor from the simulation of type I (W=40 μm) and type II (W=60 μm).

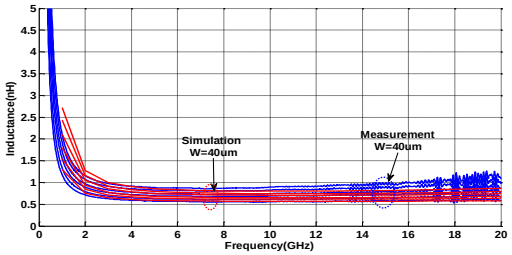
### C. Inductor Measurement



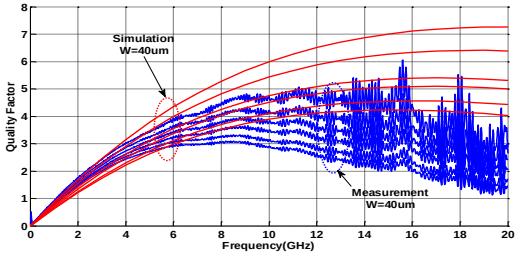

(a) ( b)

Figure 4. The layout of (a) solenoid inductor and (b) open pad for de-embedding.

Solenoid inductor was fabricated in 0.13 μm digital CMOS process and measured using on-chip probing. With a network analyzer (N5230A), a cascade microtech probe station and cascade microtech ground-signal (GSG) probes, the two port S-parameters of the solenoid inductor were measured range from 100 MHz to 20 GHz. The pad de-embedding was performed by subtracting out Y-parameters of open pad from Y-parameters of the solenoid inductor. Fig. 4 shows an inductor layout with probe pattern and open pad used for pad de-embedding. The measured inductance and quality factor after de-embedding are shown along with the simulation results in Fig. 5.




(a)

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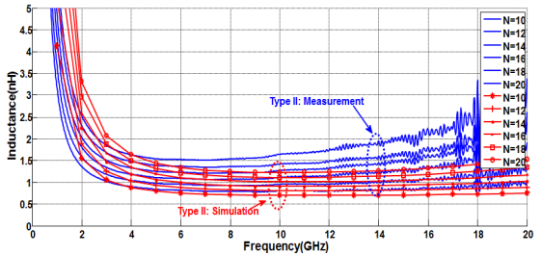


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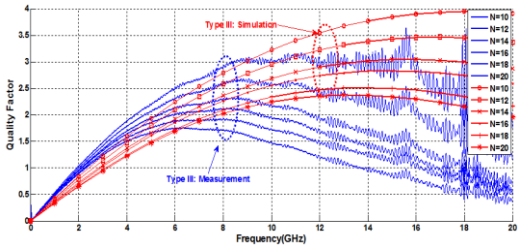



(d)

Figure 5. (a) and (c): Measured inductance (Blue) vs. the simulated inductance (Red) (b) and (d): the measured Q-factor (Blue) vs. the simulated Q-factor (Red) of type I and type II inductor respectively.

## III. Solenoid Inductor Modeling

In general, the spiral inductor has been characterized using "π" model [7]-[8]. The solenoid inductor can also use this "π" model ignoring some parameter. In this paper, a lumped-element circuit from the spiral model was established for the solenoid inductor model as shown in Fig. 6.

In this model, $R_S$ and $L_S$ are the series resistance and the inductance, respectively. The capacitance coupling, $C_f$ which is modeled as a feed forward fringing one between two terminals can be neglected since two terminals are surely separated by the inductor length. $C_P$ is denoted as the base plate coupling capacitance with the substrate. $C_{SI}$ and $R_{SI}$ are the substrate parasitic capacitance and

resistance, respectively. With this model, every inductor from type I and type II with number of turns has been optimized over 100 MHz and 20 GHz about the magnitude and phase with the measured de-embedded S-parameters using Agilent ADS [9]. The results are listed in Table I.

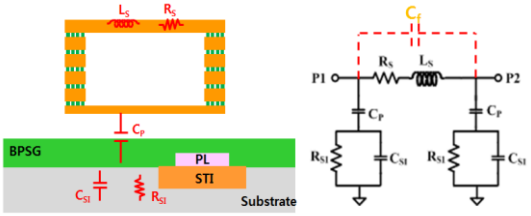



Figure 6. The lumped equivalent model for the solenoid inductor.

TABLE I. SUMMARY OF PARAMETERS FOR THE PROPOSED SOLENOID INDUCTOR MODEL

| Model | # of Turn | $L_S$(nH) | $R_S$(Ω) | $C_P$(fF) | $R_{SI}$(Ω) | $C_{SI}$(fF) |
|---|---|---|---|---|---|---|
| Type I (40W) | 10 | 0.50 | 3.52 | 82.5 | 182.4 | 9.95 |
| | 12 | 0.54 | 4.42 | 91.9 | 180.1. | 14.7 |
| | 14 | 0.59 | 4.95 | 101.0 | 181.9 | 14.4 |
| | 16 | 0.64 | 5.78 | 108.7 | 193.1 | 13.0 |
| | 18 | 0.70 | 5.85 | 114.0 | 169.4 | 10.6 |
| | 20 | 0.75 | 6.71 | 120.0 | 174.4 | 10.9 |
| Type II (60W) | 10 | 0.68 | 7.27 | 100.2 | 198.5 | 12.7 |
| | 12 | 0.78 | 9.25 | 112.6 | 189.3 | 15.8 |
| | 14 | 0.88 | 11.6 | 122.7 | 181.1 | 16.5 |
| | 16 | 0.99 | 13.4 | 133.0 | 184.9 | 14.5 |
| | 18 | 1.10 | 14.0 | 136.9 | 173.9 | 8.0 |
| | 20 | 1.20 | 16.7 | 142.9 | 167.7 | 7.6 |

Among these model parameters, $R_{SI}$ and $C_{SI}$ are almost constant over design parameters, W and N. $L_S$, $R_S$ and $C_P$, however, seems dependent on these design parameters, W and N. Fig. 7 shows each model parameters such as $L_S$, $R_S$ and $C_P$ for type I and type II have dependency against the number of turns (N). From a structure point of view, each design parameters have a relationship of the width and the height, which can be written as;

$$C_{P2} = C_{P1} * W_2/W_1 \quad (9)$$

$$L_{S2} = L_{S1}*(W_2+H_2)/ (W_1+H_1) \quad (10)$$

$$R_{S2}=R_{S1}*(W_2+H_2)/ (W_1+H_1) \quad (11)$$

where $W_1$ = 40μm for type I, $W_2$= 60μm for type II, $H_1$ and $H_2$ is the height of the post for type I and type II, respectively.

TABLE II. COMPARISON INDUCTOR DIE AREA

| Ref | [10] | [11] | [12] | [13] | This Work |
|---|---|---|---|---|---|
| Process (μm) | 0.24 | 0.18 | 0.09 | 0.13-SOI | 0.13 |
| Inductor Type | Spiral | Ring | Spiral | Spiral | Solenoid |
| Inductor Size($mm^2$) | 0.053 | - | 0.020 | 0.212 | 0.013 |

Since the width of the plate is larger than the height of the post, that is W >> H, $R_{S2}$, $L_{S2}$ and $C_{P2}$ are approximately 1.2~2.5 times $R_{S1}$ , $L_{S1}$ and $C_{P1}$.

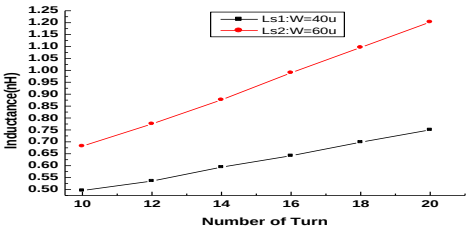
Furthermore, each turn of solenoid inductor is repeated in longitude and design parameters can be expressed in terms of N as shown in Fig. 8. Thus these equations are summarized as

$$L_S (N) =0.048*N + 0.20 \quad (12)$$

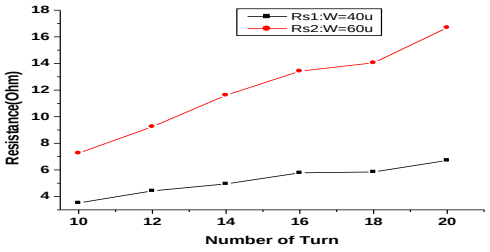
$$R_S (N) =0.765*N+0.78 \quad (13)$$

$$C_P (N) =4.132*N+62.17 \quad (14)$$

From these equations, the constants, $L_S$ (0), $R_S$ (0) and $C_P$ (0) come from the parasitic of input terminals.




(a)

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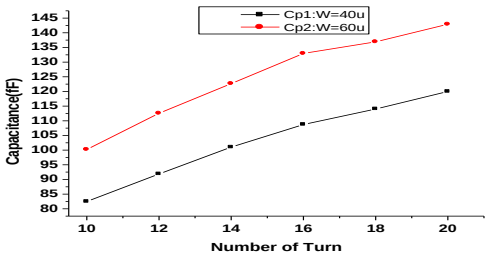


(c)

Figure 7. (a) $L_S$ .vs. N (b) $R_S$ .vs. N (c) $C_P$ .vs. N; subscript of each parameter denotes 1 for type I and 2 for type II.

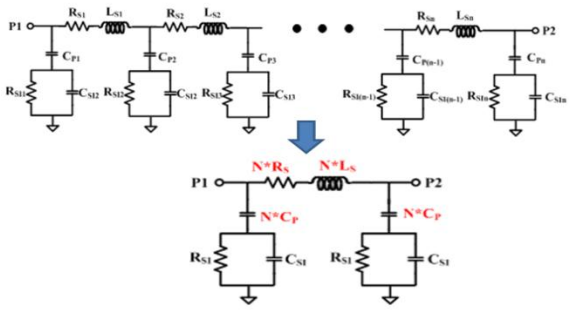


Figure 8. The proposed unified equivalent model of solenoid inductor.

## IV. CONCLUSIONS

A small area solenoid type inductor was proposed and its electrical characteristics were evaluated by EM simulation. The two types of solenoid inductors were

fabricated and compared to the simulation result. Using the proposed unified equivalent model, the design parameters based on the dimension were optimized over high frequency band and linearized by 1st order equation.

The solenoid inductor has small area compared to the prior art as shown table II. This solenoid inductor is expected to use the LC type VCO in gigahertz PLL in the standard CMOS process with saving die cost. Moreover, the scalability by number of turns gives the advantage of choosing the inductance and quality factor by engineer insight.

## ACKNOWLEDGMENT

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