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Full-Custom Design Fractional Step-Down Charge Pump DC-DC Converter with Digital Control Implemented in 90nm CMOS Technology

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***Abstract*—A full-custom design fractional step-down charge pump DC-DC converter with digital control is proposed, design and simulated in 90nm 1P9M CMOS process technology. This paper aimed to design a simple and small solution size implementation of DC-DC converter with fast settling time response and low ripple output voltage *implementation* while not compromising efficiency requirement. Moreover, this converter can operate at internally fixed 1 MHz with input voltage from 2.2V to 3.3V suitable for two batteries power applications. The converter is design to have an output voltage of 1.1V with load current requirement of greater than 10mA, a ripple voltage less than l0mV and a faster settling time of 82.9 µs. The peak efficiency is over 75%.**

***Index Terms*—charge-pump, DC-DC converter, fractional step- down, peak efficiency, output voltage**

I. Introduction

Many portable electronic devices are emerging in the market and are widely used by billions of people every day. To make these devices portable, one may consider the size and performance of the battery. Importantly, high conversion efficiency should be designed to contribute a wider time range for the battery in operation. In overall, the optimum size and weight of portable devices might be the primary choice of the consumer, thus, miniaturization and reduction of the external components of power converter should be integrated in a single chip if possible. This converter is a DC- DC which plays an important role in the Power Management Unit (PMU) on a System-On-a-Chip (SOC) design. Wherein, PMU system is composed of several DC-DC converters and voltage regulators. It is necessary to have a PMU in SOC's in order to regulate the voltage and convert this unregulated voltage to different regulated voltages for the different subsystem inside the SOC's.(1)

In designing the converter, efficiency requirement for a particular application should be will defined since the choice of DC-DC converter architecture defines it aside from addressing the physical issues.

Therefore, this study focuses in designing a simple DC-to-DC converter through switched capacitor or known as charge pump DC-DC converter topology. In particular, a Fractional Charge Pump Step-down DC-DC converter with digital control is presented in this paper. It uses three fractional conversion ratios which simulated and implemented in 90nm CMOS process technology.

Moreover, the proposed digital part of the system of the design will be done by customizing the implementation of the transistor level to have a better control and in fine tuning the overall system performance. This technique will try to improve the low efficiency performance of the traditional architecture.

II. Circuits Discription

A. System Description

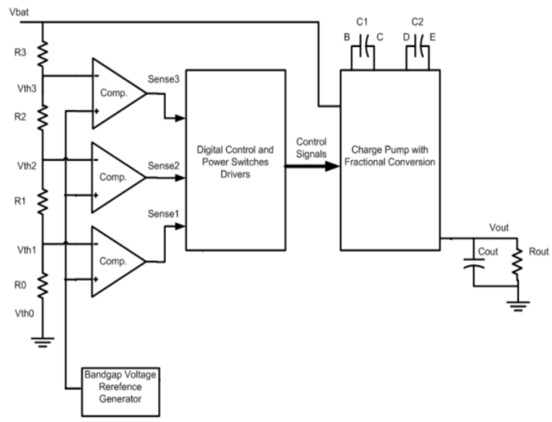

Figure 1. Overall block diagram of the charge pump DC-DC converter

Fig. 1 illustrates the structure of the fractional charge pump DC-DC converter with digital control. The converter is composes of power stage, digital control, power switches drivers and the battery sensing block consisting of resistors and three comparators.

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The power stage contains external capacitors and a power switches array, which consists of several power transistors. The operational mode of the system are based on the three comparator's digital outputs and the control selection will base on the input introduce in the system as describe from Table I.

TABLE I. COMPARATORS DIGITAL OUTPUT, SELECT MODE AND VIN TRANSITION MODE THRESHOLD

Sense 3	Sense 2	Sense 1	Modes	cm0	cm1
0	0	0	1/1	1	1
0	0	1	2/3	1	0
0	1	1	1/2	0	1
1	1	1	1/3	0	0

Furthermore, the input battery voltage is first detected by the series resistors formed as voltage divider to produce the reference voltages for the hysteresis comparators, which are used to select different charge pump structures.

Hysteresis comparators as shown in Fig. 2 and are adopted in the system to prevent the mode to oscillate that is cause by the sudden change of external situations. The digital control and power switches driver block used to generate the driving signals of the power transistors used as switches to control the charge pumps. It is implemented by a source-coupled differential pair with a positive feedback to provide a high gain wherein the gain result simulation is derived from (2).

$$A_v = \sqrt{\frac{\mu p(W/L)1}{\mu n(W/L)10}}\, x \frac{1}{1-\alpha} \qquad (1)$$

where α is positive feedback factor.

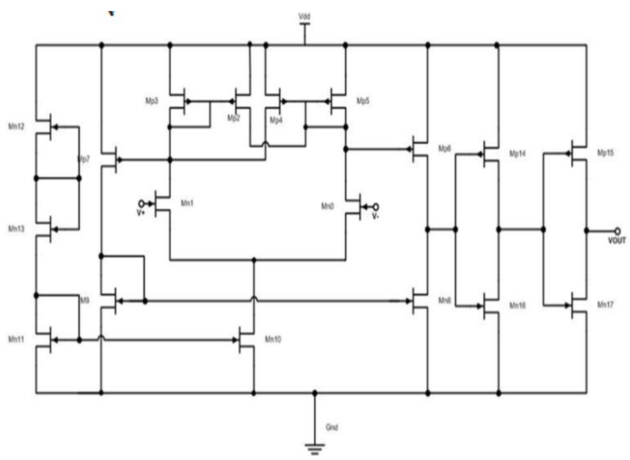

Figure 2. Schematic of hysteresis comparator

B. *Charge Pump Fractional Convertion Ratios*

Fractional conversion ratios can be realized by different charge pump structures, shown in Fig. 3. The charge pump can provide three different conversion ratios, that is, 1, 2/3, 1/2 and 1/3 constructed by the different predetermined switch sequences, shown in Table II.

TABLE II. POWER SWITCHES CONFIGURATION AND CLOCK PHASES

Ratio	*Phase 1*	*Phase 2*	*Off*
1/3	1, 4, 7	2, 6, 8, 9	3, 5
1/2	1, 5	2, 6	3, 4, 7, 8, 9
2/3	1, 3, 5, 7	2, 4, 8	6, 9
1/1	1, 2, 3, 9	1, 2, 3, 9	4, 5, 6, 7, 8

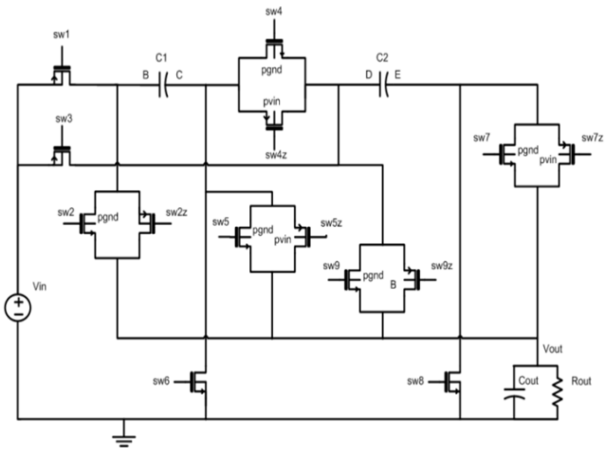

Figure 3. Schematic of the power switches used in the charge pump

For ratio equal to 1, it is like the conventional LDO (low dropout regulator) as it can produce very small ripple voltage. (3) Ratios equal to 1/3, 1/2 and 2/3 are realized in the two non- overlapping clocks with a frequency of 1MHz.

On the other hand, SW1 and SW3, connecting the flying capacitors to the input voltage were implemented with PMOS power transistors, in order to enable full range operation with VIN used to supply the charge pump drivers. The switches that connect the flying capacitors terminals to the ground voltage were implemented with NMOS transistors, allowing lower area implementation for equivalent RDS resistance. The remaining switches were implemented with NMOS and PMOS transistors in parallel, implementing a low equivalent resistance during start-up and normal operation in all modes.

The dimensions of the transistors where determined using the drain current equation. Considering the NMOS transistor, when small VDS voltage is considered, the drain- source resistance, RDS, in the linear region (switch operation) of a transistor is given by (4).

$$R_{ds} = \frac{1}{\frac{W}{L}\mu Cox(V_{gs-}V_{th})} \qquad (2)$$

Moreover, a precision voltage reference and a wide range of temperature range are essential in many applications such as data and power converters. In this design, bandgap circuit is used as a reference voltage in the hysteresis comparator of the voltage sensing circuit. Fig. 4 shows the schematic design of the used bandgap voltage reference architecture with a voltage output of 1.1V.

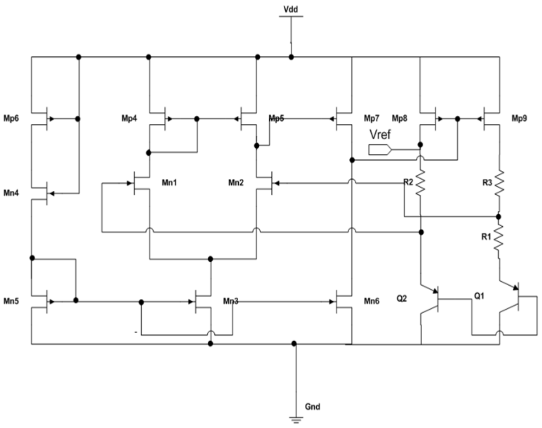

Figure 4. Bandgap voltage reference of 1.1V

III. Digital Control

A. Control Techniques

Constant frequency control is used as a control technique and two sequenced phases of operation are also employed to control the amount of charge injected in the flying capacitors. During the charge phase, the flying capacitors are charged to the proper voltage by connecting it with the battery. On the other hand, in the discharge phase, the flying capacitors are connected to the output terminals and consequently, discharged into the load through the output capacitor. Table III is a more detailed data as control logic table basing the logic operation of each switch for every mode and phase.

TABLE III. Switch Operation for Each Mode and Phase

Modes and Switch-On Phases (Phase 1 – X, Phase 2 – Y)									
CM CM0	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
0 0	X	Y	OFF	X	OFF	Y	X	Y	Y
0 1	X	Y	OFF	OFF	X	Y	OFF	OFF	OFF
1 0	X	Y	X	Y	X	OFF	X	Y	OFF
1 1	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON

Consequently, the said logic table can generate logic equations for the control of the power switches from bits mode (cm1, cm2) and phases (phase 1, phase 2) as shown in Table IV.

TABLE IV. Switch Logic Equation

Switch	Equation
Sw1 =	Phase1 + (cm1’ x cm0)
sw2 =	Phase2 + (cm1’ x cm0)
sw3 =	(Phase1’ x cm1) + (cm1’ x cm0)
sw4 =	(Phase1’ x cm1’ x cm0) + (Phase2’ x cm1’ x cm0)
sw5 =	Phase1’ x (cm1’ x cm0 + cm1’ x cm0)
sw6 =	Phase2’ x cm1
sw7 =	Phase1’ x cm0
sw8 =	Phase2’ x cm0
sw9 =	(Phase2’ x cm1’ x cm0) + (cm1’ x cm0)

B. Control Blocks and Circuits

The charge pump digital control block is compose of sawtooth wave, non-overlapping clock generator, pre-switch control, switch control, drivers and a comparator as shown in Fig. 5. The drivers circuit block is used to drive the power switches in the power module.

On the other hand, Fig. 6 shows the schematic of the pre–switch control that generates two driving signal Cm0 and Cm1 which are used to control the mode of operation of the charge pump. It is controlled according to the voltage sense output. The logic circuit was generated from Table I thru Karnaugh mapping. (5) Furthermore, Fig. 7 is the switch control logic circuit implemented in the system which was generated basing from the logic equation formulated in Table IV above.

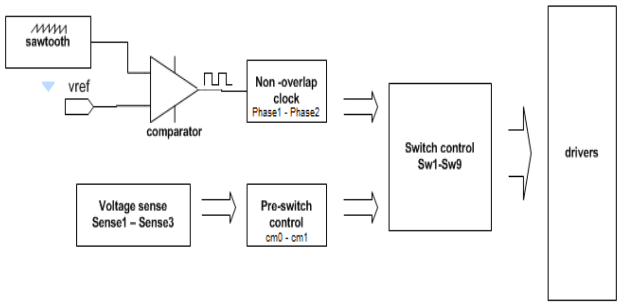

Figure 5. Block diagram of charge pump digital control

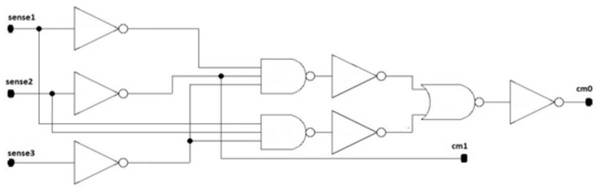

Figure 6. Pre–switch control

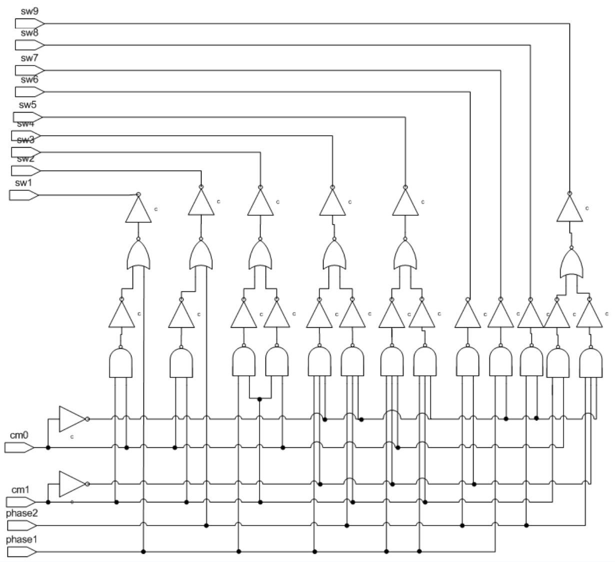

Figure 7. Switch control

IV. Simulation Results

The simulated result of bandgap output voltage reference was verified and tested thru its temperature and voltage supply independence and most importantly, the Monte Carlo simulation analysis for process variation test. Fig. 8 shows the temperature curvature waveform of the bandgap simulated at 3 different major corners with target output voltage of 1.1V.

Figure 8. Bandgap temperature variation test @ TT, FF and SS corner

On the other hand, the waveform shown in Fig. 9 is the switch control output waveform at different modes depending on the supply voltage value. Furthermore, mode 1/1 do not have phases because the flying capacitors are disconnected at this mode and the input is connected directly to the output via switches 1, 2, 3 and 9.

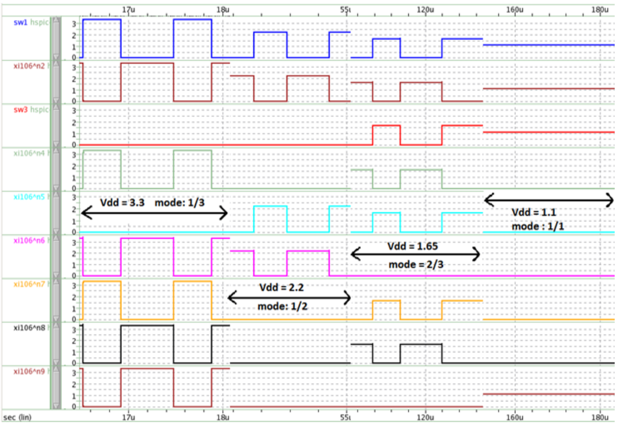

Figure 9. Switch control output waveform in different modes

Whereas, Fig. 10 shows the output voltage waveform of the fractional charge pump DC-DC converter wherein is steady at 1.1V with 1mA load current at supply voltage ranging from 3.3 to 2.2, justifying that the overall system works well. However, in 1.65V supply voltage, there is a significant voltage rise up to 1.15V with the reason that when changing from 2.2V to 1.65V, the excess of charge in the flying capacitors will be delivered progressively to the output capacitor as required by the load.

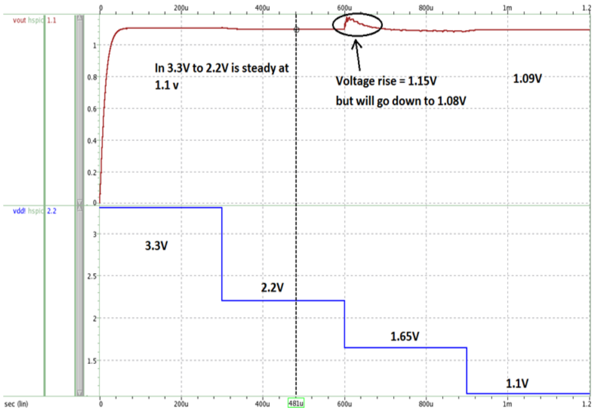

Figure 10. Output voltage at different supply level

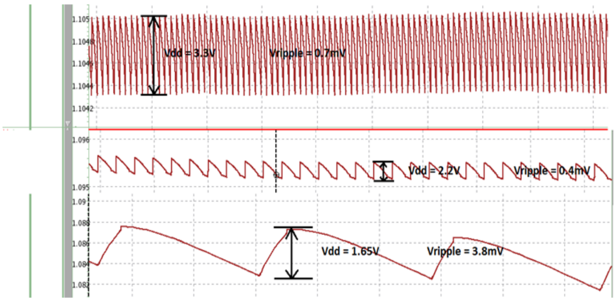

Figure 11. Ripple voltage at 3 different Vdd value (3.3V, 2.2V,1.65V)

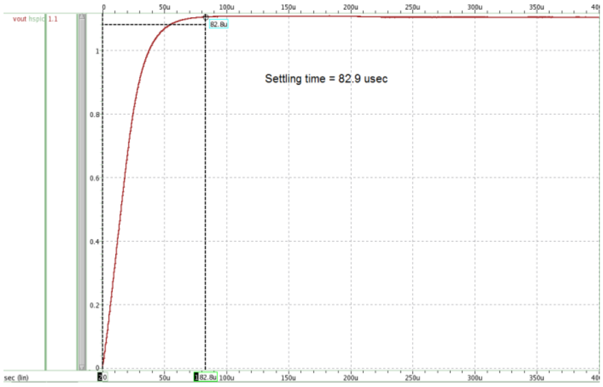

Figure 12. Charge pump DC-DC out voltage settling time

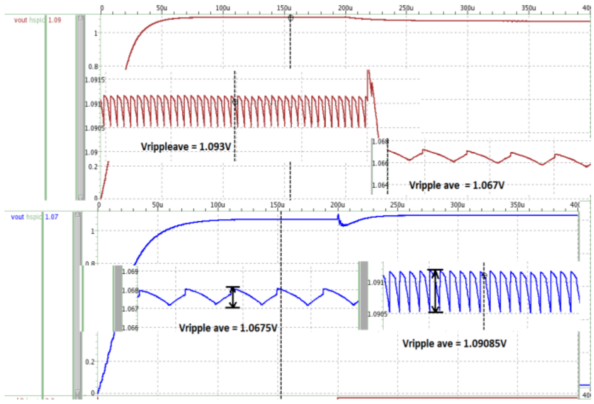

Figure 13. Line regulation @ 5mA load

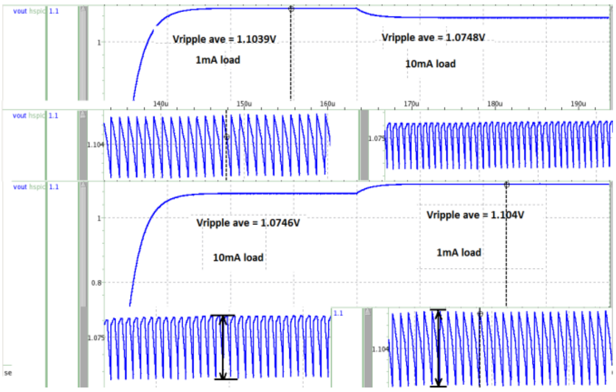

Figure 14. Load regulation waveform @ Vdd =3.3V

Fig. 11 shows the ripple voltages of 0.7 mV, 0.4 mV and 3.8mV simulated at 3 different supply voltages equal to 3.3V, 2.2V and 1.65V, respectively. Also, Fig. 12 shows a fast settling time of the system at 82.9 µs which is much better compared to other sources referred. Furthermore, line and load regulation was also measured with the simulated waveform shown in Fig. 13 and Fig. 14, respectively.

Fig. 15 shows the efficiency graph of the proposed design fractional charge pump DC-DC converter measured at input voltages of 3.3V and 2.2V with a pick efficiency of 76%. Also, Fig. 16 depicted the design layout of the overall fractional-charge pump DC-DC converter with occupies an are with a dimension of 753 µm by 406 µm. Moreover, Table V shows the overall simulation results summary of the system design.

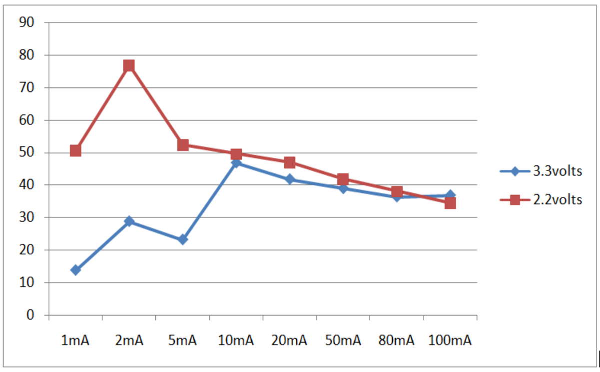

Figure 15. Efficiency plot for Vdd of 3.3V and 2.2V

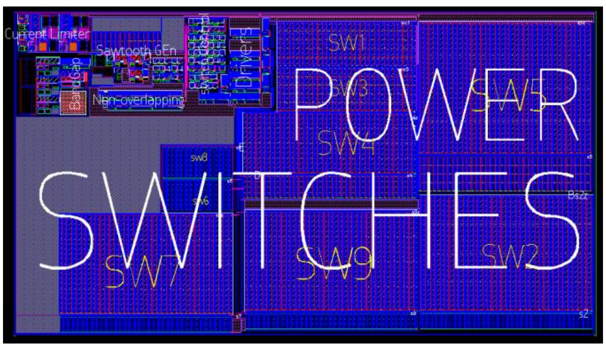

Figure 16. Design layout of the proposed fractional charge-pump DC-DC converter

TABLE V. FRACTIONAL CHARGE PUMP DC-DC CONVERTER SIMULATION RESULTS SUMMARY

Parameters	This Paper
Input voltage	2.2 – 3.3v
Output ripple	<10mv(.08/.04)mV
Output Voltage	1.1V
Switching Frequency	1Mhz
Output Current	0 – 10mA
Maximum Efficiency	Peak of 76%
Architecture	90nm
Load regulation -3.3V	2.915mV/mA
2.2V	2.94mV/mA
Line Regulation(5mA)	23.64mV/V
2.2-3.3V	21.23mV
Flying Capacitors	1uF
Load Capacitor	3uF

V. CONCLUSION

A full-custom design fractional charge pump was designed and evaluated in 90nm CMOS process technology. The proposed design achieved a digital controlled charge pump to select appropriated mode according to supply voltage and to have a regulated voltage output of 1.1V. A control method was designed in order to optimize the modes of operation and transitions between them, for different input voltages and output currents. Moreover, had achieved an output ripple less than 10mV, much faster settling time system at 82.9 µs and having a peak efficiency of 76% at low load condition.

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