Design, Fabrication and Analysis of a 1.1 ghz Phase-Locked Loop Frequency Synthesizer for Wireless Communication Systems

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***Abstract*—A 1.1GHz phase-locked loop frequency synthesizer has been developed, designed and fabricated to study phase noise (PN) of the system. The system has been implemented by using a frequency synthesizer (ADF4002, Analog Devices), having a low noise digital phase frequency detector, a precision charge pump, a programmable reference divider (R divider) and a programmable feedback frequency divider (N divider). The charge pump, reference divider and phase frequency divider are programmed externally through a serial peripheral interface by writing to CLOCK, DATA and LATCH ENABLE control of the device. The system is interfaced to a personnel computer through an 8085 microprocessor via RS232 serial bus. This paper will give a brief outline of the hardware design, testing and study the PN of the system.**

***Index Terms*—phase-locked loop, loop filter, phase noise, OshonSoft**

I. Introduction

A frequency synthesizer is an electronic system that generates one or more frequencies derived from a single reference frequency [1]. Such systems are used as accurate frequency sources in a wide variety of electronic apparatus and extensively in radio frequency (RF) wireless communication systems for clock extraction and generation of low PN local oscillator signal from an on-chip voltage controlled oscillator (VCO) [2], [3], [4], [5]. The Phase locked loop (PLL) is widely used in designing frequency synthesizers and is a key block in most of the frequency synthesizers. The PLL frequency synthesizer uses a feedback loop for synchronization of output phase and frequency with the phase and frequency of a reference signal. The major problems in designing such a system are frequency accuracy, frequency step, tuning range, amplitude, PN and sideband (spur) [6]. In the process of frequency synthesis, PN is generated in the system and hence predicting the PN in the system and accurate modeling of such system in component level is essential [7]. Prior to widespread use of synthesizers, radio and television receivers relied on manual tuning of a local oscillator. The variations in temperature and aging of components use to cause frequency drift. Automatic frequency control (AFC) solved some of the drift problem, but manual retuning is often necessary. The ultimate goal of PLL frequency synthesizers is to generate precise and stable output frequencies with fast switching and minimal spurious and PN [8], [9]**.** It can maintain good accuracy in frequency over time and changing temperatures. The fast switching and low spurious noise represent a tradeoff that depends upon the synthesizer's loop filter (LF). By properly designing the LF, a desired balance can be achieved between PLL spurious levels and lock time. In view of the above we propose to design, fabricate and analyze a 1.1GHz PLL frequency synthesizer suitable for wireless communication systems.

Manuscript received August 8, 2013; revised March 1, 2014.

II. The Proposed System

The block diagram of the proposed system is shown in Fig. 1. It consists of a frequency synthesizer (ADF4002), a passive LF, a VCO (MC100EL1648), a reference frequency generator, a buffer amplifier and an 8085 microprocessor (μP) unit. The synthesizer consists of a low noise phase frequency detector (PFD), a programmable R divider, a feedback frequency N divider, and a precision charge pump (CP). The R divider allows the input reference frequency to be divided down to produce the reference clock (CLK) for the PFD. It has a wide range of division ratio from 1 to 16383. The N divider is a 13-bit counter and has division ratios from 1 to 8191. The PFD compares the phase and frequency of the signal from R and N divider. It produces an output control signal proportional to the phase and frequency difference between them. The on-chip registers of the synthesizer can be programmed externally by using serial peripheral interface (SPI) through writing to CLK, DATA and latch enable (LE) control of the device. The

doi: 10.12720/ijeee.3.1.19-23

maximum allowable CLK rate of the device is 20MHz. The system is interfaced to personnel computer (PC) through 8085 µP via RS232 for writing data to the device. A buffer circuit is also interfaced in-between the synthesizer and the µP. The synthesizer includes a 24-bit shift register where the data is clocked down on each rising edge of the signal. Initially, the data is clocked with most significant bit (MSB) and transferred from the shift register to one of the four latches available in the device on the rising edge of LE. The destination latch is determined by the state of the two least significant bits (LSB) in the shift register. An external parallel tank circuit consisting of an inductor and a capacitor is used with the VCO to adjust the frequency. The varactor diode (MMBV609) with a parallel inductor is connected into the tank circuit to provide a voltage variable capacitance for the input of the VCO. These components have direct impact on the tuning sensitivity and PN. The quality factor (Q) of the tank circuit has direct impact on the resulting PN of the oscillator [10]. Therefore, the Q is kept high for lower PN in the oscillator. The typical operating frequency of the VCO is up to 1100MHz. The VCO output is fed to Spectrum Analyzer (Make: Agilent, Model: N9320B, 9KHz-3 GHz), Digital Storage Oscilloscope (DSO) (Make: Tektronix, Model: TDS2014C, 100MHz, 2GS/s, 4 channel) and Digital Phosphor Oscilloscope (DPO) (Make: Tektronix, Model: TDS3052, 500 MHz, 2.5 GS/s). The spectrum analyzer, DSO and DPO are interfaced to PC via universal serial bus (USB) for online monitoring and recording data.

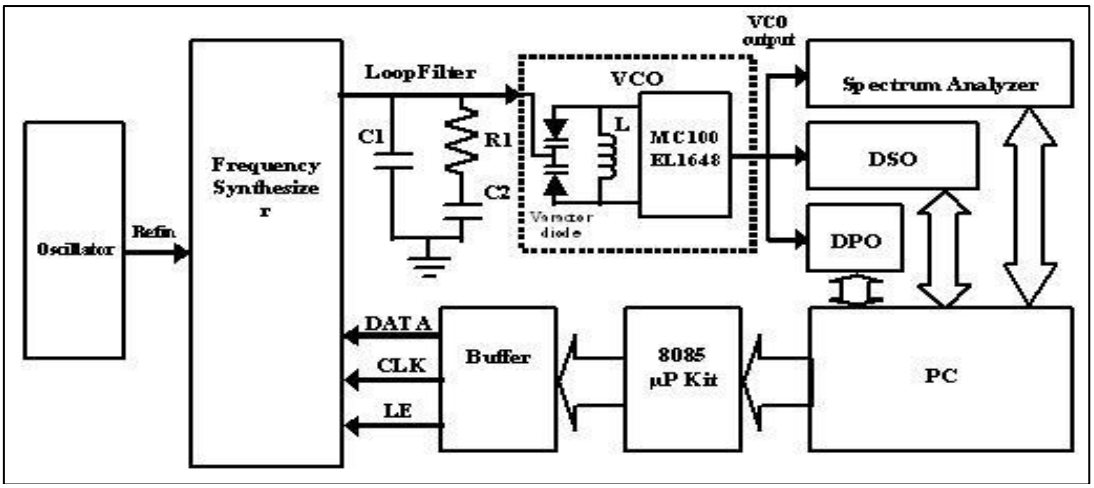

Figure 1. The block diagram of the proposed PLL frequency synthesizer

A. The Hardware Design &Fabrication

The system hardware is designed based on surface mount device (SMD) technology. The schematic of the printed circuit board (PCB) for the system is designed on Novarm Dip Trace PCB design software platform.

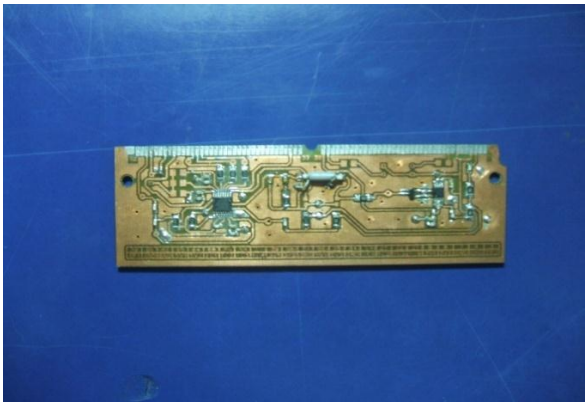

Figure 2. PLL synthesizer

The layout of the PCB is printed on one side of a double sided glass epoxy copper cladding through tonner transfer method. The other side of the PCB is then colored so as to keep the copper cladding intact during etching. The PCB is etched by using $FeCl_3$ solution at room temperature. The SMD components are mounted and soldered on the PCB by using SMD RE-WORK station (Model: MAX-7805) through hot air method. The fabricated PCB is shown in Fig. 2. The other side of the PCB is grounded to minimize noise effect of the system. An instrument module and a buffer unit are also fabricated. The instrument module consists of a single in-line memory module (SIMM) to mount the synthesizer board, a 5V regulated power supply unit to feed power to different units, and different input output (I/O) connectors for the system. The synthesizer board mounted on SIMM along with the buffer and µP unit is shown in Fig. 3.

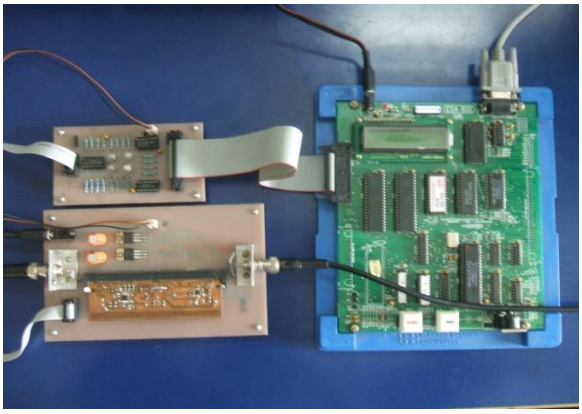

Figure 3. PLL synthesizer mounted on SIMM

B. The Software

The program for the system is developed on OshonSoft 8085 µP simulator integrated development environment (IDE) having user-friendly graphical development environment for Windows. The platform has integrated simulator, basic complier and assembler, de-assembler and debugger for Intel 8085 µP. The program is transferred to µP from PC through RS232 serial port. The complete algorithm of the program developed for the system is given below.

TABLE I. THE ALGORITHMS

STEPS	INSTRUCTIONS	STEPS	INSTRUCTIONS
1	Initialize ports	11	Decrement C register content by 1
2	Store data into memory location	12	Repeat step 7 to 11 till value of C
3	Initialize register D to 4		Register become 0
4	Initialize register E to 3	13	Increment memory location
5	Load 8-bit data from memory	14	Decrement E register content by 1
	Location to accumulator A	15	Repeat step 5 to 14 till value of E
6	Initialize the counter C to 8		Register become 0
7	Rotate content of accumulator	16	O/P 1 in LE
	Left by one position	17	O/P 0 in LE
	Through Carry flag	18	O/P 0 in CLK
8	O/P 0 in CLK	19	Decrement D register content by 1
9	If there is a carry, O/P 1 in data	20	Repeat step 4 to 19 till value of D
	O/P port otherwise 0		Register become 0
10	O/P 1 in CLK	21	End program

III. DEVICE CONFIGURATION & TESTING

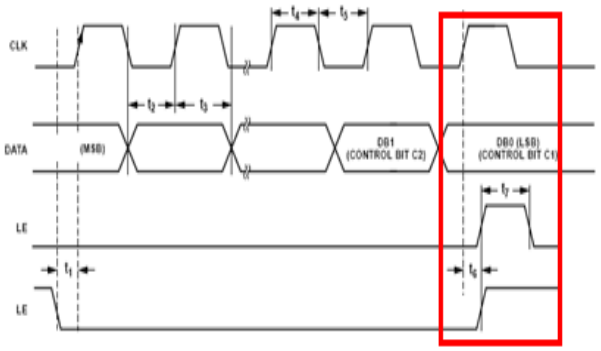

Figure 4. Timing diagram of the chip [9]

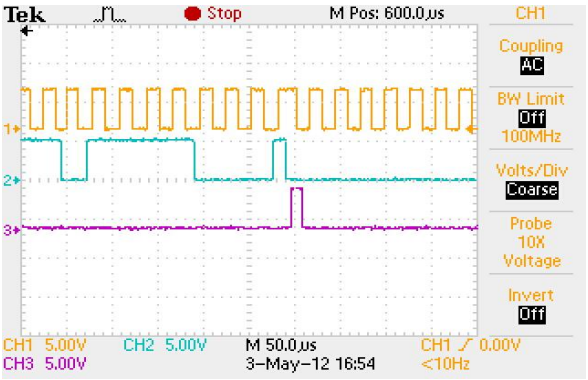

Figure 5. Timing signal generated by µP 8085

The device can be configured through programming by three different methods, namely: (i) initialization latch, (ii) chip enable (CE) and (iii) counter reset method. The initialization latch method is used to configure and test the present synthesizer system. In this method, data for initialization latch is clocked first by setting the LSB to binary 11. Then the data for function latch, R and N divider are clocked by setting LSB to 10, 00 and 01 respectively. The timing signal for configuring the device is shown in Fig. 4, where t_1 = DATA to CLK setup time, t_2 = DATA to CLK hold time, t_3 = CLK high duration, t_4 = CLK low duration, t_5 = CLK to LE setup time, t_6 = LE pulse width [11]. The timing signal generated by µP for CLK, DATA and LE to configure and test the system and recorded by DSO is shown in Fig. 5. Once the timing signal generated by µP is transferred to the device, it will be automatically configured and ready for operation.

IV. RESULTS & DISCUSSION

A low power VCO with a supply voltage of 5V is used to power the system. The gain of the VCO is 31 MHz/V and tuning range is set at 128 MHz to 256 MHz for test. A second order LF is used in the loop and hence forms a third order system. The loop BW is selected to optimize the output PN and to maintain reasonable settling time and spur rejection. The loop BW of the system is set at 3.5 KHz and the phase margin (PM) is 46˚. The CP current is set at 2.5 mA. Output frequency spectrum of the system (Fig. 6) shows that the output power is –8.26 dBm when the system is locked at 254.6MHz. The recorded PN is –80.9dBc/Hz and –107.8dBc/Hz at 10 kHz and 1 MHz offset respectively from the carrier for the same locked state. Fig. 7 and Fig. 8 show the PN spectra of the system.

Again the measured output power is –8.94 dBm and PN is –59.79 dBc/Hz and –109.1dBc/Hz respectively at 10 kHz and 1 MHz offset from the carrier when the system is locked at output frequency of 240.4 MHz. Fig. 9 shows the output power profile and Fig. 10 and Fig. 11 show the output PN profile at 10 kHz and 1 MHz offset respectively when the system is locked at 240.4 MHz. Fig. 12 shows the time taken by the system to change the output frequency from 240.4 MHz to 254.6 MHz and the recorded time is 3.2 mS. The overall PN spectrum for the system is shown in Fig. 13 when the system is locked at 226.3 MHz, 240.4 MHz and 254.6 MHz respectively. The observed PN and Figure of Merit (FOM) of the system are summarized in the Table. I.

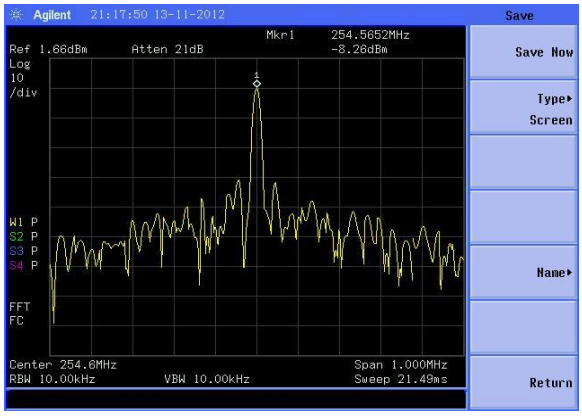

Figure 6. Output spectrum of the frequency synthesizer at 254.6 MHz.

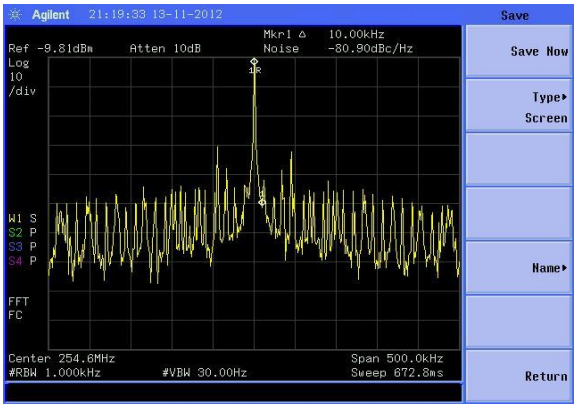

Figure 7. Phase noise at 10 kHz offset from the carrier when system is locked at 254.6 MHz

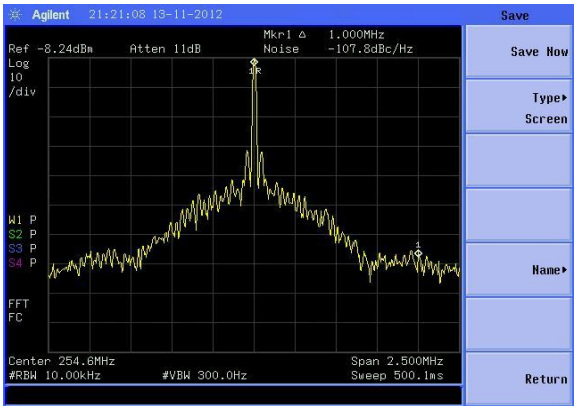

Figure 8. PN at 1 MHz offset from the carrier when system is locked at 254.6 MHz

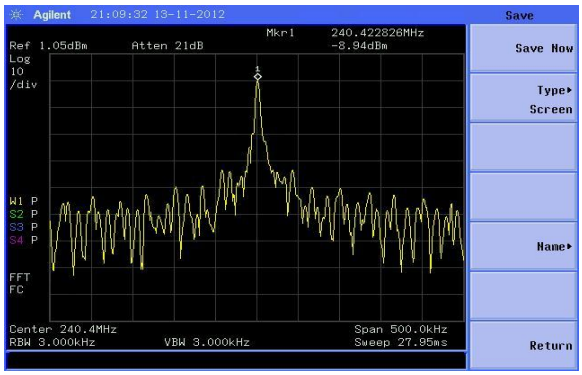

Figure 9. Output spectrum of the frequency synthesizer at 240.4 MHz.

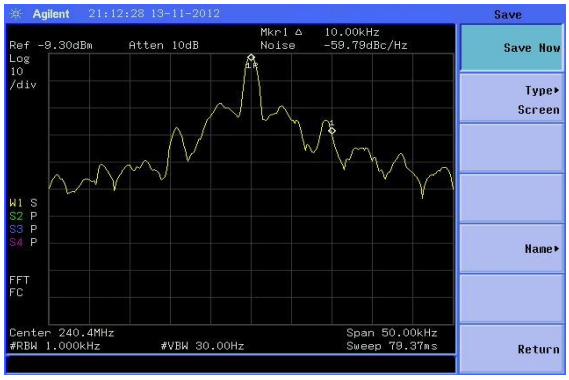

Figure 10. PN at 10 kHz offset from the carrier when system is locked at 240.4 MHz.

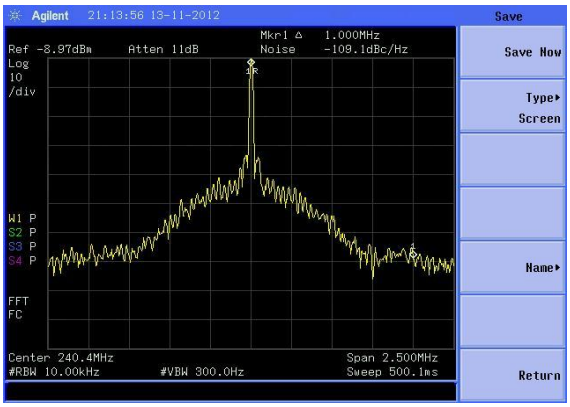

Figure 11. PN at 1 MHz offset from the carrier when system is locked at 240.4 MHz.

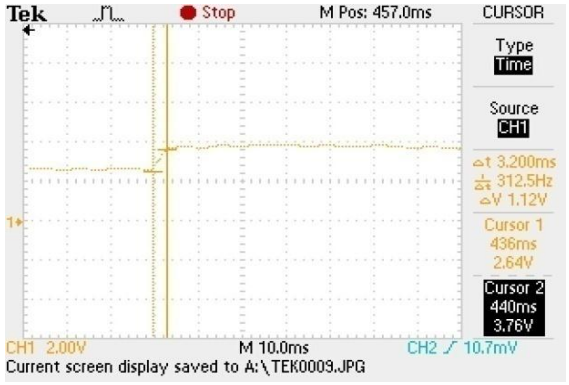

Figure 12. Time taken by the system for changing output frequency from 240.4 MHz to 254.6 MHz.

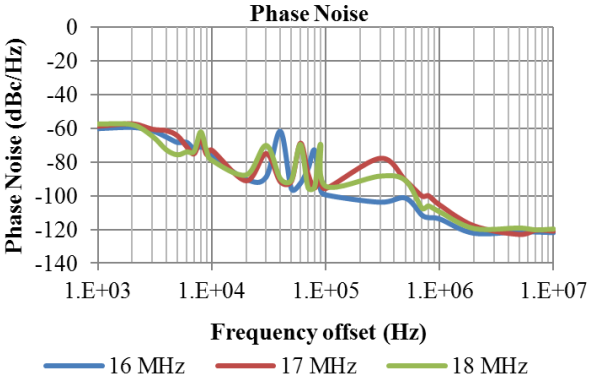

Figure 13. Measured PN spectrum when the system is locked at frequencies 226.3 MHz, 240.4 MHz and 254.6 MHz.

TABLE II. THE PN MEASUREMENT SUMMERY OF THE SYSTEM

Locked frequency (MHz)	PN @ 1 KHz (dbc/Hz)	PN @ 100 KHz (dbc/Hz)	PN @ 1 MHz (dbc/Hz)	FOM (dbc/Hz)
226.3	-60.14	-99.45	-113.7	-181.072
240.4	-58.72	-95.64	-105.4	-181.336
254.6	-57.41	-94.35	-109.5	-181.584

V. CONCLUSION

The VCO produces a wide range of output frequency as varactor controlled LC circuit is used which changes the equivalent parallel resistance of the LC circuit in a wide range across the full operating voltage of the power supply. But the capacitive component of the LC circuit includes the input capacitance of the VCO device, other circuit and parasitic elements. In the present system, the PLL synthesizer frequency range is from 128 MHz to 256 MHz for the control voltage ranging from 1 to 5 Volt. The equivalent resistance of tank circuit varies widely over the tuning range. For high frequency, the current of the device is reduced and thereby reduces power consumption. Measurement shows that the PN is below-100 dBc/Hz @ 1 MHz offset for all the cases. The PN at lower frequencies is better than at higher frequencies. Fig. 13 shows that within the loop BW of 3.5 KHz, the PN is dominated by noise added from the frequency divider (FD) and PD. Below the loop BW the PN plot typically flattens out resulting in-band PN floor. From Fig. 13, the in-band PN floor is estimated approximately to be -60dBc/Hz. The FOM or 1 Hz normalized PN Floor is calculated and shown in the Table. II. The measured FOM ranges from–181.072 dBc/Hz at lower frequencies to–181.584 dBc/Hz at the upper limit of the frequency range. So, although the basic PN is worse at higher frequencies, the observed FOM is better. The PN Floor can be decreased by increasing the PFD comparison frequency. Some spurious signal or spurs are visible in Fig. 13. This spurs may come from different sources such as PLL reference spurs, some internal or external signals coming through bias and control interface circuits. It is observed that the spurs are located at the multiple of PFD comparison frequency. Hence it may be due to reference frequency. The synthesizer can tuned to produce frequencies up to 1.1GHz with minimum noise, and hence can be used in FM, television broadcasts, line-of-sight ground-to-aircraft, aircraft-to-aircraft communications, Land Mobile, Maritime Mobile communications, amateur radio, and weather radio communication systems.

ACKNOWLEDGEMENT

Authors are thankful to the All India Council of Technical Education (AICTE), Government of India for funding the work. They are also thankful to Analog Devices, USA, for supplying few SMD components free of cost and time to time technical support towards implementation of the work.

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