2-1, 2-2 and 2-1-1 MASH Delta-Sigma Modulator for 18-Bit Audio Digital to Analog Converter

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***Abstract*—MASH modulators are cascaded low order modulators that are designed to increase the fidelity of the output signal at the receiving end of the transmission medium. One sigma-delta third order dual truncation 2-1 MASH and two sigma-delta fourth order dual truncation 2-2 and 2-1-1 MASH modulators with 18-bit input format are successfully implemented in TSMC 0.13μm Logic CMOS Technology. Both the third-order and fourth-order delta-sigma MASH modulators are generated using RTL code by the aid of MATLAB and Verilog Compiler Simulator. The total area is 800.25μm^2 for 2-1, 1205.75μm^2 for 2-2 and 1064.5μm^2 for 2-1-1 while the total cell area is 903.473167μm^2 for 2-1, 1360.541228μm^2 for 2-2 and 1204.5855μm^2 for 2-1-1. Furthermore, the total dynamic power of the circuit for 2-1, 2-2, and 2-1-1 are 1.7496 μW, 2.8821μW and 3.3002μW respectively. The resulting signal-to-noise ratio was below 100dB. However, by the aid of the third-order Butterworth filter the original signal can be reconstructed.**

***Index Terms*—MASH, modulator, noise shaping, DAC**

I. Introduction

Delta-sigma modulation is a method for encoding high resolution or analog signals into lower-resolution digital signals. The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. The low-resolution signal typically changes more quickly than the high-resolution signal and it can be filtered to recover the high-resolution signal with little or no loss of fidelity. This technique has found increasing use in modern electronic components such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), frequency synthesizers, switched-mode power supplies and motor controllers. [1], [2]

Noise shaping conversion method has become the main technology for high resolution A/D or D/A conversion for use in audio and telecommunications. This method attains high linearity by oversampling and noise shaping, which decreases the quantization noise in the signal band by emphasizing the noise in the out signal band. MASH (Multistage noise shaping) is a technology where theoretically, does not have limit to noise shaping order, thus making it easier to design highly accurate converters. [2]

Thus, in this study, the researchers aims to implement 2-1, 2-2, 2-1-1 Multistage Noise Shaping modulators that can be applicable for audio DAC applications using TSMC 0.13μm Logic CMOS technology.

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II. Design Architecture

Delta-sigma modulation is a method for encoding high-resolution or analog signals into lower-resolution digital signals. The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. The low-resolution signal typically changes more quickly than the high-resolution. The 2-1, 2-2 and 2-1-1 MASH (Multistage Noise Shaping) modulators that will be developed in this research are cascaded low-order modulators which are combined to guarantee stability and to produce a larger signal-to-noise ratio compared to 1st or 2nd-order modulators only. Also, in this research, the designs are based on the dual-truncation ΔΣ noise-shaping loop concept since each stage has its own truncator or quantizer. The dual-truncation ΔΣ noise-shaping loop is illustrated in Fig. 1. However, the drawback of this design is a complex digital circuitry. [3]

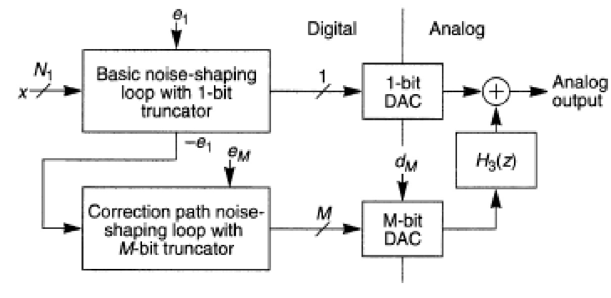

Figure 1. A dual-truncation ΔΣ noise-shaping loop

A. 2nd Order MASH

The basic block used in the first stage architecture is the 2nd order modulator presented in Fig. 2. The input to the circuit feeds to the two cascading integrator which is composed of accumulators and delay blocks. Output of

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the 2nd stage accumulator is feed to quantizer. The quantized output is feeds back, to subtract from the input signal. The feedback forces the average value of the quantized signal to track the average input. [2], [3]

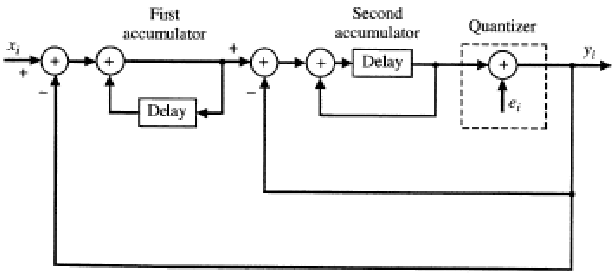

Figure 2. 2nd Order MASH Architecture

B. 2-1 MASH Modulator for 2nd Stage

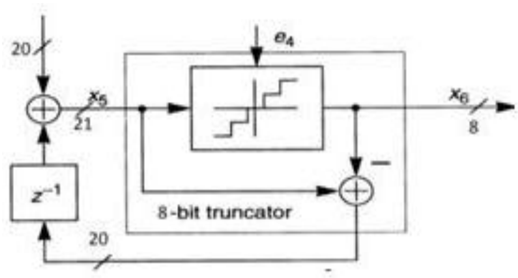

Figure 3. 2nd stage of 2-1 MASH modulator

The 2-1 modulator's 2nd stage is implemented using Fig. 3. The data coming from the 1st stage is added together with data stored in the 2nd stage register. The sum is then forwarded to the 8-bit quantizer to produce an 8-bit output. [2]

C. 2-2 MASH Modulator 2nd Stage

The 2-2 MASH modulator's 2nd stage differ from the 2-1 MASH 2nd stage [4]. It uses a 2nd order modulator instead of a 1st order. MASH 2-2 architecture is presented in Fig. 4.

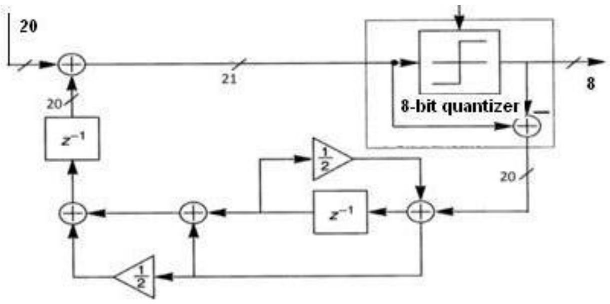

Figure 4. 2nd stage of 2-2 MASH modulator

Data coming from the 1st stage is added together with the previous data stored in the 2nd register of this stage. The sum is given to the 8-bit quantizer to form the 2nd stage's output. Also, the 8-bit quantizer forms another output that will fed to its correction path. The data in this path passes through 2 integrators to form the next data that will be added to the data coming from the 1st stage.

D. 2-1-1 MASH Modulator 2nd to 3rd Stage

Fig. 5 is similar to Fig. 3 in its 2nd stage. However, in this architecture, another 1st order is attached to act as a 3rd stage. This 3rd stage follows the same implementation as the 2nd stage. Yet, its input is the data coming from the 2nd stage. [2]

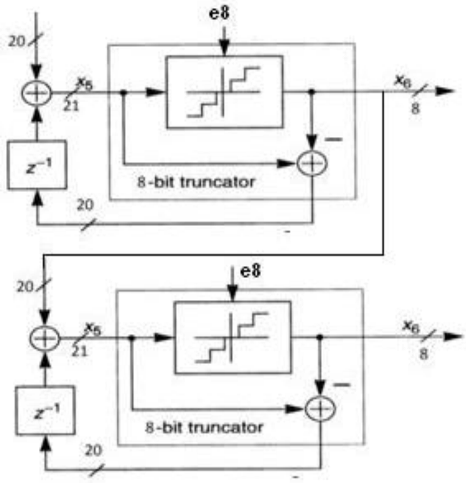

Figure 5. 2nd to 3rd stage of 2-1-1 MASH modulator

III. Circuit Design Implementation

To fully understand the true behavior of the MASH architecture, the performance is evaluated first using Mathlab simulator. Then, when all the design specifications satisfied, the actual implementation is design using verilog code run in the Synopsys tools environment.

A. H Behavioural Implementation

To simplify the discussion of the three different MASH architectures, this paper focuses only on the discussion of MASH 2-1 architecture.

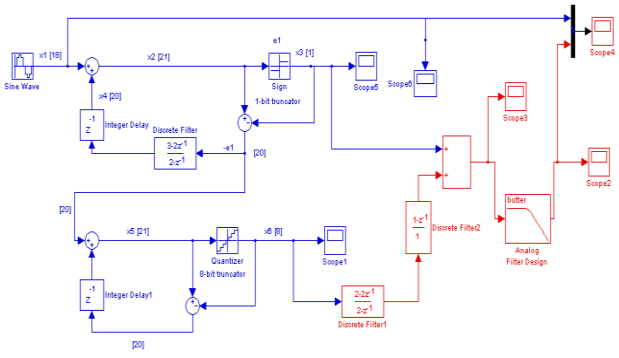

Figure 6. 2-1 MASH behavioural implementation

Fig. 6 illustrates the behavioural model of the 2-1 MASH architecture. It consists of simplified z-transforms of the 1st stage 2nd order and 2nd stage 1st order modulators. The blocks in blue comprise the modulator while the blocks in red are analog implementation [5] which' is outside the scope of this study. They are only used for reconstruction purposes.

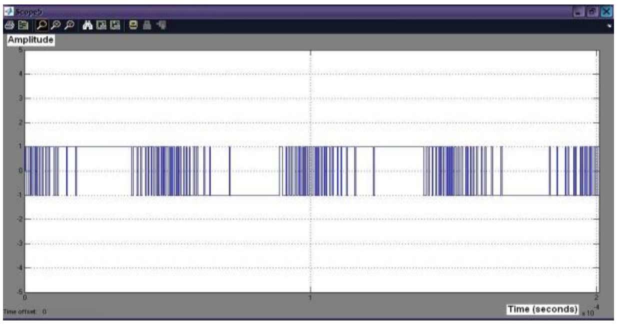

Figure 7. 1-bit truncator behavioural output (2-1)

Fig. 7 displays the expected output of the 1-bit truncator. This output should be the primary goal in designing MASH sigma-delta modulators since the truncator output holds the most significant bit (MSB). The MSB is the one responsible for obtaining the closest approximate to the true value.

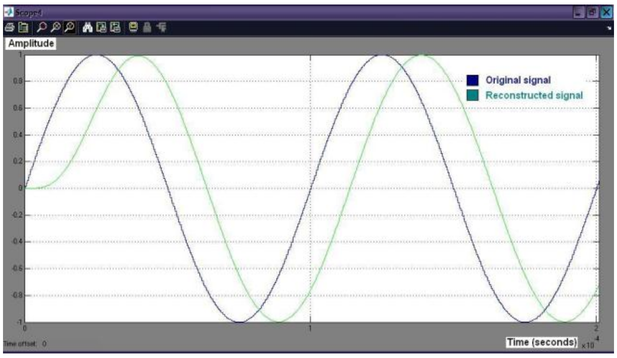

Figure 8. Reconstructed signal for 2-1 MASH modulator

Fig. 8 shows the expected output after the 2-1 MASH modulator's output is dumped to the reconstruction blocks in MATLAB. Obtaining this output means a step closer to successful reconstruction of the signal.

The implementation of 2-2 MASH modulator [4] is similar to the 1st behavioural model, Fig. 6. They differ only in the 2nd stage where in this architecture, a 2nd order modulator is used instead of a 1st order. Also 2-1-1 MASH modulator is similar to 2-1 MASH modulator and only differs in 1st order additional stage.

B. MASH Modulators Actual Implementation

Initially, the initial output of the truncator is subtracted from the initial data input as shown in shown in Fig. 9. The difference is then fed to the adder as its addend along with the initial value of register.

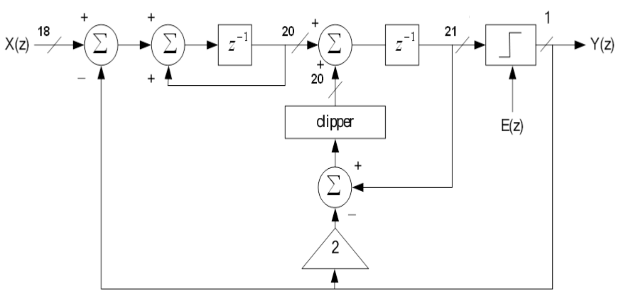

Figure 9. Block diagram of first 2nd-order sigma delta modulator

The output is then stored in the register for 1 clock cycle. This output is then forwarded to another adder along with the clipper's output which is initially zero too to produce the sum that will be stored to the next register. This sum will again be stored for 1 clock cycle. Truncation of the MSB will then follow.

The truncated MSB will be subtracted from the next data input to get the next difference that will be added to the 1st register's previous data and also be shifted 1 bit to the left then subtracted to the previous 2nd register's value to form the clipper's output. The clipper will remove the LSB of its input to form a 20-bit data that will be added to the adder.

This cycle will repeat continuously until all data input has been accommodated.

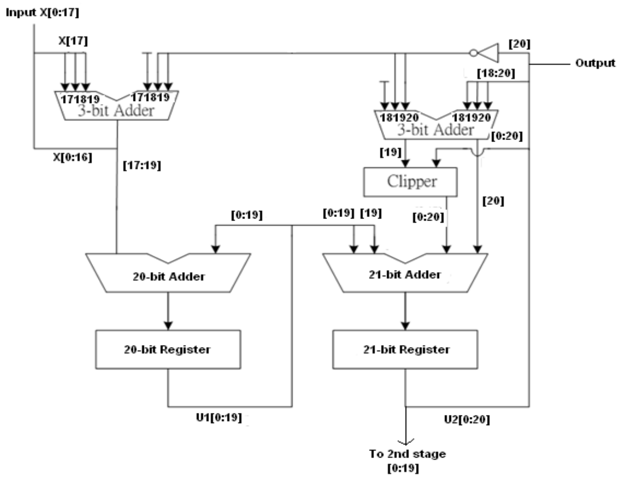

Figure 10. Circuit implementation of 1st & 2nd-order modulator

The block diagram in Fig. 9 is implemented using the circuitry in Fig. 10. Instead of using subtractors, 3-bit adders are used to simplify the circuitry. The result of the 3-bit adders without the overflow is similar to the output of the subtractors.

C. 8-Bit Quantizer

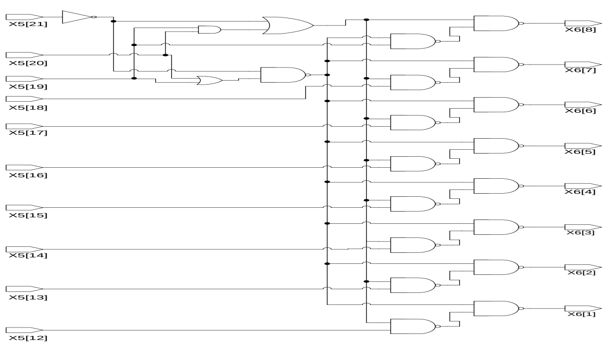

Figure 11. Circuit implementation of the 8-bit quantizer

The 8-bit quantizer is used for all 3 architecture which functions as a digital quantizer and amplitude limiter. Having an 8-bit quantizer improves the signal-to-quantization noise ratio. The circuit implementation is shown in Fig. 11. [2]

IV. SIMULATION RESULTS

Results are obtained after execution in Verilog Synopys Simulator. The designed modulators' outputs are dumped to their respective ideal digital-to-analog converters then passed through an ideal 3rd order Butterworth lowpass filter having a passband of 24kHz in MATLAB.

A. 2-1 MASH Modulator Simulations

Fig. 12 is the result of simulation of the 2-1 MASH modulator design using Verilog Compiler Simulator (VCS). It shows the original signal in analog form is reconstructed to 1-bit truncator signal output. To check if the truncator output is correct, the reconstructed pulse width of a 1-bit data would depend on the amplitude of the original signal. Also, Table I portrays the bit stream generated for the 1st 7 sampling periods. This output bit stream for the 2nd stage is used as an error signal to reduce the truncation error.

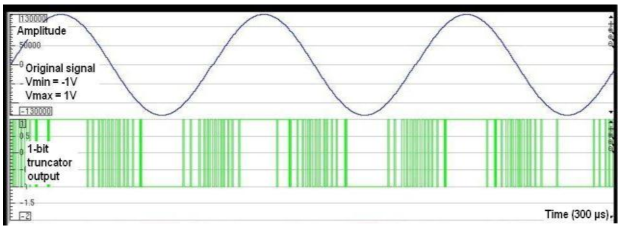

Figure 12. Verilog compiler simulator result for 2-1 MASH modulator

TABLE I. FIRST 7 OUTPUT BIT STREAM OF THREE STAGES

Truncated 1-bit	8-bit quantizer output							
1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0	0
0	0	1	1	1	1	1	1	1

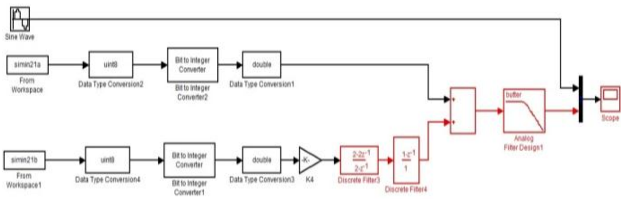

Figure 13. Reconstruction model (2-1 MASH modulators)

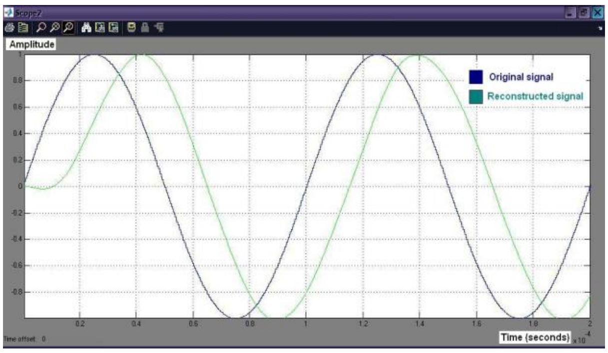

Figure 14. Reconstructed 2-1 modulator output in MATLAB

The verilog simulated dumped data is reconstructed using the model in Fig. 13, the reconstructed signal is displayed in Fig. 14. The reconstructed signal shows same results as compared to simulation in matlab behavioural model in Fig. 8 having a delay of approximately 16µs. This is due to several stages of filter blocks that cause the delay.

The same methodology in 2-1 MASH modulator is being done to 2-2 and 2-1-1 MASH modulator.

B. SNR and Power Simulation Result

Fig. 15 shows the FFT power spectra of the reconstructed data for the three architectures. It is also shown that the Signal-to-Noise Ratio (SNR) of the 2-1 MASH modulator is below 100dB with the absence of the filter. Thus, the filter is vital in reducing the noise. Also, below 100 db is being measured on 2-2 and 2-1-1 MASH modulator.

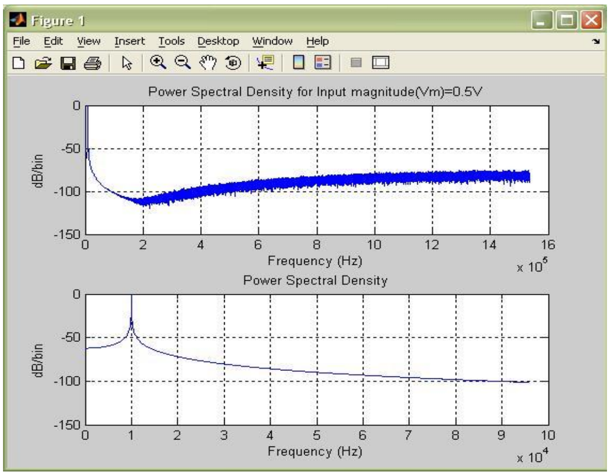

Figure 15. Output power spectrum of 2-1 MASH modulator

Among the three modulator designs made, the 2-1 MASH modulator has the same SNR with the other three modulator designs but has the lowest noise shaping capability.

On the other hand, the SNR and noise shaping capability of the 2-2 MASH modulator design has a better noise shaping due to the higher order second stage. Hence, the 2-1-1 MASH modulator design has the best noise shaping capability among the three modulator designs.

C. Actual Digital Layout

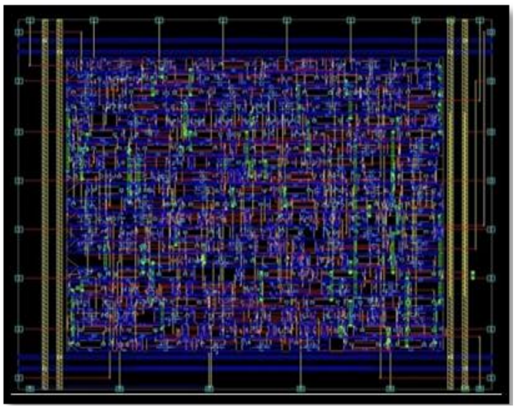

Figure 16. Block level layout of 2-1 MASH MODULATOR

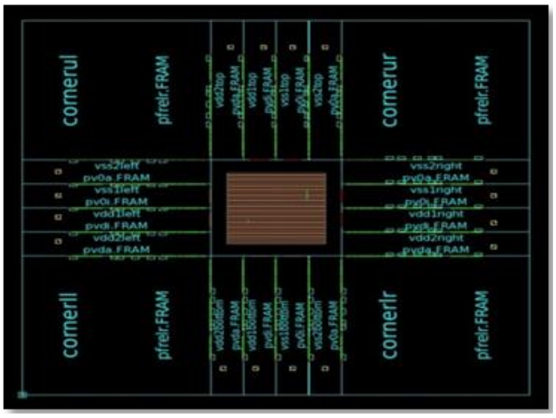

Figure 17. Chip level layout of 2-1 MASH MODULATOR

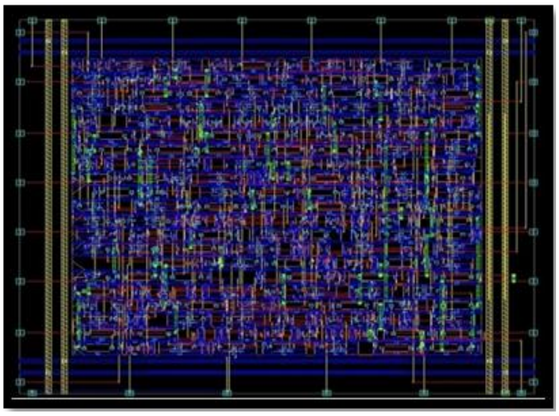

Figure 18. Block level layout of 2-2 MASH MODULATOR

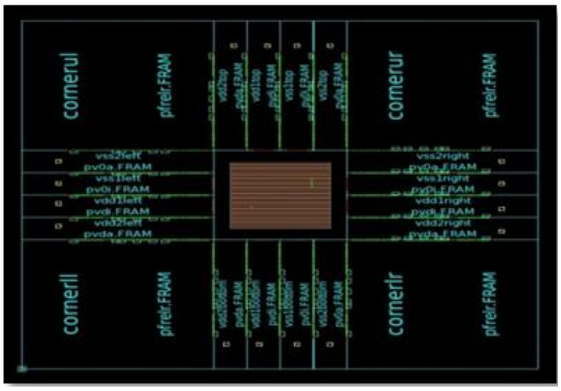

Figure 19. Chip level layout of 2-2 MASH MODULATOR

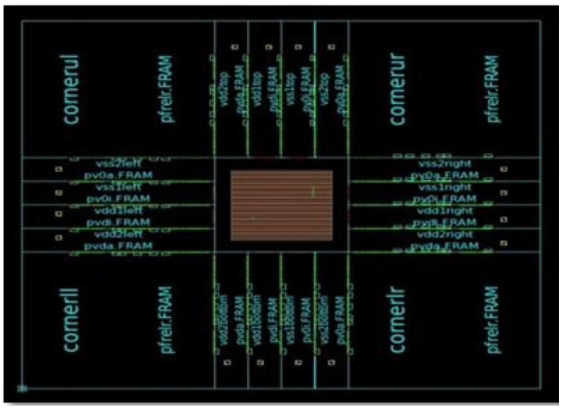

Figure 20. Chip level layout of 2-1-1 MASH MODULATOR

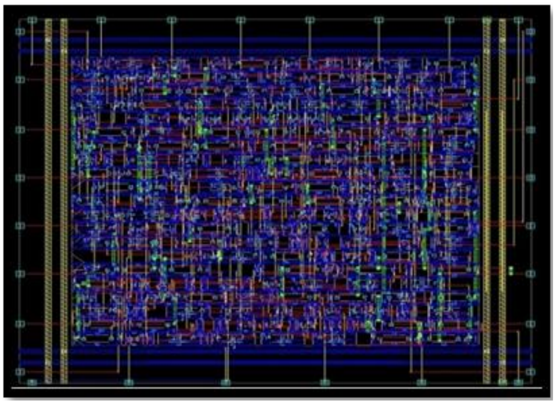

Figure 21. Chip level layout of 2-1-1 MASH MODULATOR

The digital block level layout and chip level lay-out of the three modulators architectures are presented in Fig. 16 to Fig. 21 using TSMC 0.13 μm Logic CMOS Technology. Design specification and comparison with other study is shown in Table II.

TABLE II. DESIGN SPECIFICATIONS

Parameter	Reference Paper	Research Design		
Order	3	3 (2-1)	4 (2-2)	4 (2-1-1)
Input Data	16 bits	18 bits	18 bits	18 bits
Bandwidth	44.1 kHz	48 kHz	48 kHz	48 kHz
Output SNR	110 dB	<100 dB	<100 dB	<100 dB
Modulator Sampling Rate	2.82MHz	3.07MHz	3.07MHz	3.07 MHz
OSR	64	64	64	64
Output Data	1bit/ 4bits	1bit/ 8bits	1bit/ 8bits	1bit/ 8bits

V. CONCLUSION

An 18 bit audio MASH 2-1, 2-2 and 2-1-1 modulator architectures for delta-sigma D/A converter is analyzed and has been successfully implemented. The fundamentals of modulator block of a delta-sigma DACs and special aspects when they are used in audio applications are discussed in detail in different sections of this paper. Thus, the conclusion and analysis of this research are formulated and summarized as follows:

MASH 2-1, 2-2, and 2-1-1 modulator architectures were successfully implemented by combining single stage delta-sigma loops and second-order delta-sigma loop. Simulated results are presented and all simulations are based on ideal and actual behaviors. Furthermore, the actual simulation shows that the digital part is working and is effective since the digital message which is the original signal has been reconstructed after passing through the lowpass filter. Thus, these architectures could be a great used in the implementation of D/A blocks with minimum time delay.

The total area is 800.25 μm^2 for 2-1, 1205.75 μm^2 for 2-2 and 1064.5 μm^2 for 2-1-1 while the total cell area is 903.473167 μm^2 for 2-1, 1360.541228 μm^2 for 2-2 and 1204.5855 μm^2 for 2-1-1 using the TSMC 0.13 μm Logic CMOS Technology. Also, the slack time for the three modulator designs (2-1, 2-2 and 2-1-1 MASH modulators) are 287.69ns, 287.66ns and 284.69ns respectively. This indicates that the design is good in terms of timing because the data arrives before the clock changes from logic high or logic low.

ACKNOWLEDGEMENT

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REFERENCE

[1] R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press Wiley Interscience A Jhon Wiley & Sons, 2005.

[2] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters*, IEEE Press, 1997.

[3] F. Medeiro and B. Perez-Verdu, *Top-Down Design Modulator Architectures*, Kluwer Academic Publishers, 1997.

[4] W. R. Liou, Y. H. Yang, H. W. Huang, and S. H. Chang, "Design of a MASH 2-2 4th-order delta-sigma A/D converter with efficient programmable digital filter," in *Proc. 2002 VLSI Design/CAD Symposium*, Taitung, Taiwan, 2002, pp. 10-13.

[5] M. L. Yeh, W. R. Liou, and B. M. Tseng, 1997, "A high-performance differential difference amplifier and application for a 10-bit A/D converter," in *Proc. 12th Technological and Vocational Education Conference*, Taichung, Taiwan, 1997, pp. 291-296.

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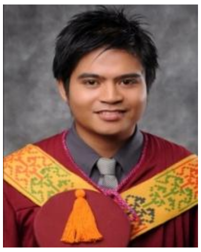

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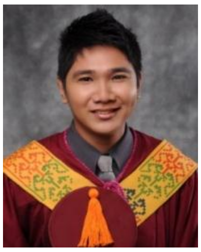

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