A 3.5 GHz Low-Noise Amplifier in 0.35 µm GaN HEMT on Si-Substrate for WiMAX Applications

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Abstract—This paper presents an 3.5 GHz low noise amplifier that uses a two-stage configuration, using 0.35 μ m AlGaN/GaN HEMT on silicon substrate technology. The first stage has a cascode topology to achieve high gain, better stability and well reverse isolation. The second stage has a RC-feedback topology for wideband matching. The Tmatching network is used for broadband output matching. The results show a maximum gain of 14.4 dB, a minimum noise figure of 3.3 dB, and an input/output return loss greater than 10 dB. With good power-handling capabilities of GaN HEMT devices, the third-order input intercept point at 3.5 GHz is +2.5 dBm and the unit consumes 170 mW of power. Good agreement between the simulated and measured results is found.

Index Terms—low-noise amplifier (LNA), AlGaN/GaN HEMT on Si, minimum noise figure (NF_{min})

I. INTRODUCTION

Gallium Nitride (GaN) devices are of great interest for System-on-Chip (SOC) technology, because of their suitability to high power applications. AlGaN/GaN high electron-mobility transistor (HEMT) technology has found widespread use in such applications, because of its high electron velocity (> 1×10^{7} cm/s), its bandgap (3.4 eV), its breakdown voltage (>100 V) and its sheet carrier concentration $(n_s > 1 \times 10^{13} \text{ cm}^{-2})$. Most AlGaN-GaN HEMTs are grown on sapphire [1], [2], or SiC substrates [3]-[5]. The sapphire substrates are cheap, but inefficient in dissipating heat because of their poor thermal conductivity. GaN HEMTs on semi-insulating SiC have excellent crystalline quality and thermal dissipation, because there is reduced lattice mismatch and high thermal conductivity (4.9 W/cm·K). The disadvantages of GaN-on-SiC are its higher cost and unstable crystal quality. Currently, there is increasing interest in growing AlGaN-GaN HEMT structures on Si substrates [6]-[11], which has the advantages of low cost, a large-size substrate and good thermal conductivity (1.5W/cm·K). The main challenge in GaN-on-Si is the cracking of the GaN film due to stress. Recently, several authors have presented studies of the power of AlGaN-GaN HEMTs on a silicon substrate, at different frequencies [6]-[11]. The good power-handling capabilities make this technology suitable for receiver electronics. The high degree of linearity of circuits based on AlGaN/GaN HEMTs ensures a large dynamic range for the receiver electronics. The low noise amplifier (LNA) is an important element of a wireless transceiver. The lownoise amplifier (LNA) is the first stage in the receiver. It must provide good input impedance matching low power consumption, low noise performance, sufficient gain with good S/N for the following stages, and small size over the entire frequency band. Several different approaches have been proposed to establish a universal standard for such applications, such as distributed amplifier (DA), LC ladder, current-reused, shunt feedback [12]-[20]. The cascade topology is one of the suggestions to build an RF front-end and minimize its power dissipation. However, to the authors' best knowledge, very few GaN-based LNA have been produced [21]-[25]. This study proposes a two-stage LNA using 0.35 µm GaN-on-Si HEMT technology, which operates at 3.5 GHz. The LNA has a maximum gain of 14.1 dB and a minimum noise figure of 3.3 dB. The input IIP3 at 3.5 GHz is 2.5 dBm and the unit consumes 170 mW of power. Good linearity is possible in a AlGaN-GaN HEMT because of its inherently wide bandgap, which allows high power levels, because of its high breakdown field.

II. DEVICE EPI-STRUCTURE AND PROCESS

Fig. 1 shows the cross-section photo of GaN HEMTs. The devices used in this work were grown on silicon (111) substrate, using molecular beam epitaxy. The resistivity of the Si substrate was about $10^4 \Omega \cdot cm$. The epi-layer contained an AlN/GaN nucleation layer, a 1.8-um-thick layer of unintentionally doped GaN buffer, a 1-nm-thick AlN space layer, a 18-nm-thick Al_{0.27}Ga_{0.73}N barrier and a 1-nm-thick unintentionally doped GaN cap layer. Hall measurements confirmed a sheet-carrier density of 1.03×10^{13} cm⁻² and an electron mobility of 1,534 cm²/V-s. Following mesa etching, ohmic contacts were prepared, using evaporated Ti-Al-Ni-Au multilayer metals, followed by annealing. A mushroom-shaped gate, based on Ni-Au metallization, is defined by a tri-layer resist scheme. The surface was passivated with SiO₂. The thickness of the silicon substrate was reduced to 100 µm, for better DC and RF power performance. The circuit design is microstrip line structure. The chip backside is ground shielding using Aurum. The via-hole technology is used to connect circuit ground to backside. All the

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HEMTs have a gate length of 0.35 μ m. The HEMT devices display a maximum drain current density of 576 mA/mm and dc extrinsic transconductance of 150 mS/mm. The unity current gain cutoff frequency and maximum oscillation frequency of the devices are 14.9 and 46.6 GHz. The maximum output power density of at 3.5 GHz is 1.33 W/mm (V_{ds} =10 V). Fig. 2 shows the saturation P_{out} of 23 dBm, a power gain of 8.5 dB and the maximum PAE of 28.8% are achieved at V_{ds} =10V and V_{gs} =-1.5V at 3.5 GHz for 2×75 μ m transistor.



Figure 1. The (a) structure and (b) SEM photograph of GaN HEMT.



Figure 2. Simulated RF output power, gain and PAE, for 2×25 μ m GaN HEMT, at 3.5 GHz.

III. CIRCUIT DESIGN

The LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption. The LNA needs to have a good input mating over the whole band to capture the transmitted RF energy efficiently. A schematic diagram of the proposed LNA is shown in Fig. 3. The LNA circuit is composed of $M_1 \sim M_3$, $C_1 \sim C_5$, C_F , R_1 , R_2 , R_F , L_1 , L_2 , L_s , L_{d1} , L_{d2} , and L_o . The width of M_1 and M_2 are 2×75 µm and M_3 is 2×25 µm. The first stage is a cascode topology that provides high gain, better stability and well reverses isolation. The

output stage is a RC-feedback topology to pull up high frequency gain and T-matching network that gives broadband out impedance of 50 Ω for measurement purposes.



Figure 3. Schematic of the two-stage LNA using 0.35 µm AlGaN/GaN HEMT on Si-substrate technique.

A. Input Matching

The first stage uses cascode topology, which provides high gain, better stability and good reverse isolation. In the input port, matching network with source inductance degeneration is used for matching. Fig. 4 shows the equivalent circuit for the input stage. The value of Z_{in} is derived as:

$$Z_{in} = s(L_1 + L_2 + L_s) + \frac{1}{sC_{as}} + \omega_T L_s$$
(1)

where

$$\omega_T = \frac{g_m}{C} \tag{2}$$

$$f_o = \frac{1}{\sqrt{C_{gsl}(L_1 + L_2 + L_3)}} = 3.5 \, GHz$$
(3)



Figure 4. Equivalent circuit of input matching network with source inductance degeneration.

The imaginary part of Z_{in} is set zero to operate at 3.5 GHz. The input impedance becomes $Z_{in} \approx \omega_T L_s$ is 50 Ω for matching. The transistor size M_I and inductors $(L_I, L_2,$ and $L_s)$ can be determinate to achieve good input matching. The size of transistors and bias conditions also determine the power dissipation. We evaluate the size of the transistors and bias conditions to meet the impedance and noise within limited current.

B. Output Matching

The C_3 provides signal coupling between the two stages. Fig. 5 shows the equivalent circuit for the output stage. The output stage uses a RC feedback topology, to improve the gain and for output matching. An output stage with RC-feedback topology is used. The output terminated connected input stage by R_f and C_f series connection to form a feedback network. L_{d2} , R_f and C_f components are chosen to allow a high gain. The Tmatching network is also used for wide output matching. The values of voltage gain and output impedance are derived as:

$$A_{\nu} = \frac{Z_L - g_{m,eff} Z_f Z_L}{Z_L + Z_f}$$
(4)

$$Z_{out} = Z_L //[Z_f + (Z_{in} // R_s)]$$
 (5)

where $Z'_{in} = 1/sC_{gs3}$,

$$\begin{split} &Z_f = (1/sC_{gd3}) / / (R_F + 1/sC_F) \\ &Z_L = [(s(C_4 + C_5)L_{d2}L_o] / [L_o(C_4 + C_5) + C_4L_{d2}] \\ &g_{m,eff} \approx g_{m3} \end{split}$$

We can select Z_f (R_I and C_I components) to achieve high gain and Z_L for good output matching.



Figure 5. Equivalent circuit of RC-feedback of output stage.

C. Minimizing NF

The noise figure is dominated of the first stage for the multi-stages amplifier due to the NF_{tot} is derived from [26]:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \dots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}}$$
(6)

The LNA is the first stage of the receiver system. Therefore, the noise figure is the key parameters of the LNA. In order to minimize the NF of the LNA, the size of the transistor is chosen to match the impedance and noise requirements with a limited current. Fig. 6 shows the noise figure (NF_{min}) and drain current (I_D) for 0.35 µm GaN HEMT devices of W = 2×75 µm gate width. To minimize the noise figure the input transistor, the operation biases of M₁ are V_d =10V and V_g =-1.5V.



Figure 6. Simulated minimum noise figure (NF_{min}) and drain current (ID) of 2×75 µm gate width of GaN HEMT devices.

IV. RESULTS AND DISCUSSION

The LNA was simulated using Advance Design System software. The layout is vital to RF circuit performance, because of the lossy Si substrate. Therefore, EM simulation is required to optimize LNA performance, for circuit design. The parameter for EM simulation is the use of 0.35 μ m AlGaN/GaN HEMT technology. Fig. 7 shows a photograph of the S-band LNA chip, where the total area is 2.25 mm². The LNA was tested via on-wafer probing. A network analyzer and ATN-NP5B noise-parameter system meter were used to measure the small-signal S-parameters and NF over the frequency range from 1 to 7 GHz.



Figure 7. Chip photograph of the two-stage GaN LNA.

Fig. 8 shows the measured and simulated S-parameters. The measured S_{11} was lower than -10 dB for input matching across the frequency band of 3.3~4.3 GHz. The measured S_{22} was less than -10 dB for output matching over a 3.3~4.3 GHz range. The measured forward gains (S_{21}) displays a maximum gain of 14.4 dB at 3.8 GHz and the range of S_{21} value is 11.4~14.4 dB over the 3.3~4.3 GHz frequency band. In order to optimize the performance, the transistors are sized to provide good noise characteristics, while allowing good matching of the input impedance over the required bandwidth. The drain voltage from 7 to 11 V also achieved high gain than 11.8 dB. The variations of drain voltage are small.



Figure 8. Simulated and Measured S21 of the two-stage GaN LNA.

Fig. 9 shows the measured and simulated NF values of the implemented amplifier. The measured noise figure is approximately 3.3-3.6 dB, over the 3.3-4.3 GHz range. Figs. 8-9 also show that the measured and EM simulation S_{21} and noise figure correspond to these values. Figure 10 shows the two-tone test for third-order intermodulation distortion of the LNA circuit. The third order input intercept point (IIP3) is +2.5 dBm at 3.5 GHz. The total power consumption of the chip is 170 mW, using a 10 V DC supply. It is noted that the input impedance is optimized for a low noise figure while the corresponding return loss is maintained at an acceptable level. Table I summarizes the performance of the GaN LNA, as detailed in published reports [21]-[25] and this work.



Figure 9. Simulated and Measured minimum noise figure *NF_{min}* of the two-stage GaN LNA.



Figure 10. Measured IIP3 of the two-stage GaN LNA.

TABLE I. COMPARISON OF LNA CIRCUIT PERFORMANCE: PUBLISHED AND THIS WORK.

GaN Technology (µm)		BW (GHz)	S ₂₁ (dB)	NF _{min} (dB)	IIP3 (dBm)	P _{diss} (W)	Area (mm ²)
[21]	0.25	8 - 11	20	2.0	-	0.6	3.52
[22]	0.2	1 - 25	13	4.6	28.5	0.8	1.44
[23]	0.18	0.1 - 4	17	1.5	-	1.25	4.89
[24]	0.2	1 - 8	18	1.3	20	0.7	4.59
[25]	-	2.6 - 6	22	1.5	-	0.32	4.9
This work	0.35	3.3- 4.3	14.4	3.3	2.5	0.17	2.25

V. CONCLUSION

We demonstrate the potential of large GaN HEMT devices on Si substrate for monolithic microwave integrated RF circuit. A 0.35 μ m GaN HEMT 3.5 GHz LNA that uses a two-stage configuration is designed. This exhibits a high 14.4 dB gain, a low 3.3 dB *NF_{min}*, an input/output return loss greater than 10 dB, and the IIP3 is +2.5 dBm at 3.5 GHz, while only 170 mW power dissipation. The proposed LNA satisfies WiMAX system requirements. The future will scale down the device size for higher frequency applications.

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