Design of a 8-bits Digitally Controlled Oscillator with Low Power Consumption

Qichao Zha, Tiejun Lu, Jianhui Zhang, and Yu Zong
Beijing Microelectronics Tech. Institution (BMIT), Beijing, China
Email: {zha.qi.chao, Lu_Tie_Jun, flyingchang}@163.com, zongyu@sohu.com

***Abstract*—In this paper, a low power consumption 8-bits CMOS digitally controlled oscillator (DCO) design is presented. The CMOS DCO design is based on the logic of SR trigger and the capacitors charging time from input current. Simulations of the proposed DCO using XFAB 0.35μm CMOS processes achieve controllable frequency range of 0~8MHz with a wide range of linearity. It operates over a supply voltage range from 1.8V to 3.6V, a temperature range from -45 to 80℃. Spectre simulation demonstrates that when the frequency of output signal is 8MHz the power consumption of the proposed DCO is 31.78 μA and 7.3 μA at 1MHz.**

***Index Terms*—digitally controlled oscillator, SR trigger, capacitor charging, low power consumption**

I. Introduction

In all of consume electronic systems, clock system is indispensible and practically generated by crystal oscillator or analog phase-locked loop (PLL). Crystal oscillator increases the cost and the area of the electronic systems. Recently on-chip reference oscillators are required for low-cost single-chip applications including biomedical sensors, MCU, and Socs, especially the wearable devices. RC oscillators were developed to realize on-chip oscillators with standard CMOS process.

Typical analog PLLs include a phase-frequency detector, a charge pump, a loop filter, a voltage controlled or current controlled oscillator, and a frequency divider [1], [2]. In the core of PLL, the controlled oscillator is the key component. Recently, efforts have been made toward the development of fully digital PLLs. Compared to their analog counterparts, fully digital PLLs exhibit better noise immunity and they are invulnerable to DC offset and drift phenomena [3]. The digitally controlled oscillator (DCO) is a replacement of the conventional voltage or current controlled oscillator in the fully digital PLLs. Comparatively, they are more flexible and usually more robust than the conventional VCO. Furthermore, the design compromise for the frequency gain in voltage or current controlled oscillator is not necessary in DCOs because the immunity of their control input is very high.

Manuscript received January 10, 2014; revised February 11, 2014.
This work was supported by the Beijing Microelectronics Tech. Institution (BMIT).

There are two main techniques for the DCO design as shown in Fig. 1. One technique changes the driving strength dynamically using the fixed capacitance loading [4], [5], while the other uses shunt capacitor technique to tune the capacitance loading [6], [7]. Although they both have a good linear frequency response and a reasonable frequency operating range, the power dissipation hasn't been taken into consideration. Moreover, for the DCO design, there is a tradeoff between the operating range and the maximum frequency that DCO can achieve. As a result, the increase of the operating range by adding more capacitance loading will result in a lower maximum frequency and higher power consumption. Since power consumption is of extreme concern for the portable battery charged computing systems, the reduction of the power consumption has become a major concern.

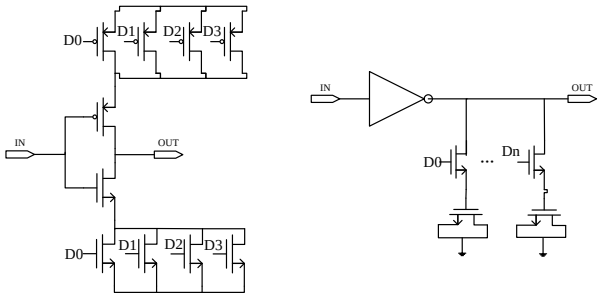


Figure 1. Standard cell of digitally controlled oscillator. (a) Driving strength controlled. (b) Shunt capacitance controlled

This paper proposes a new structure of DCO circuit with reduced power consumption using SR trigger. The proposed circuit composed of current controlled oscillator (ICO) and digitally controlled current source (DCI). The DCO is designed and simulated using the 0.35 μm XFAB CMOS process.

II. The Digitally Controlled Oscillator Circuit

The functional block diagram of DCO circuit proposed in paper is shown in Fig. 2. It is composed of current controlled oscillator and digitally controlled current source. F0~F1 is the Coarse Code of tuning the output current from the digitally controlled current source, while N0~N4 is the Fine Code. The controlled bits F0~F1 and

doi: 10.12720/ijeee.3.1.66-70

N0~N4 influence the value of output current so as to determine the frequency of the output clock signal from the current controlled oscillator.

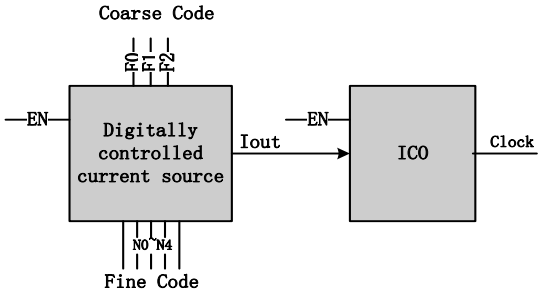


Figure 2. The functional block diagram of DCO proposed in this paper

A. Current Controlled Oscillator

This current controlled oscillator is the core of DCO and is designed based on the logic of SR trigger and the capacitors charging time from input current. The circuit proposed is shown in Fig. 3. The oscillation is simply performed as follows:

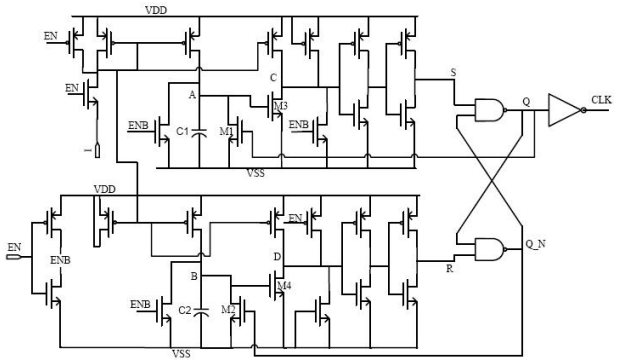


Figure 3. The current controlled oscillator circuit.

Fig. 4 illustrates the oscillator waveform signal. When EN is "low" while ENB is "high", so that V_C always maintain "low" level state while V_D is "high" all the time, these result in that V_S and V_{Q_N} are "low", nevertheless V_R and V_Q is "high", and the output sign CLK of oscillator is "low".

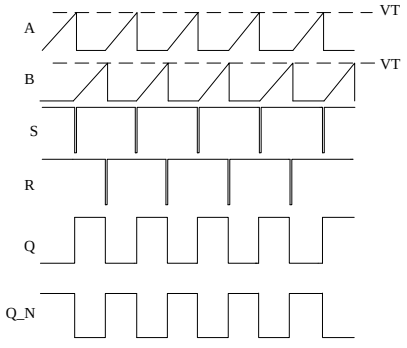


Figure 4. The oscillator circuit schematic waveform signal

When EN is "high" and ENB is "low", V_Q is "high" initial, V_A is pulled down to "low" for the MOSFET M1 is conductive and then M3 becomes cut-off bring on that V_C start to rise up to "high" from "low" and V_S is "high". On the other hand, V_{Q_N} is "low" initial, the mirror current from the Digitally controlled current source charges the capacitor C2 so that the voltage V_B rises up to the threshold voltage of M4 gradually. When V_B exceeds the threshold voltage, M4 is conductive, V_D begin to drop down and V_R complete the transition from high to low. At present, V_R is "low" while V_S is "high" result in that V_Q is "low" while V_{Q_N} is "high", the oscillator complete the flip of output sign CLK.

When V_Q is "low" while V_{Q_N} is "high", V_B is pulled down to "low" rapidly because M2 is conductive so that V_R changed back to "high" quickly. On the other hand, M1 is cut-off so that the mirror current from the Digitally controlled current source charges the capacitor C1, V_A rises up to the threshold voltage of M3 gradually. When V_A exceeds the threshold voltage, M3 is conductive, V_C begin to drop down and V_S complete the transition from high to low. At present, V_S is "low" while V_R is "high" result in that V_Q is "high" while V_{Q_N} is "low", the oscillator complete the flip of output sign CLK.

So that C1 and C2 capacitors are alternately charging and discharging in the circle, and R, S change their "high" and "low" level with 180 degree phase difference by RS flip-flop. The oscillator produces a fixed frequency clock signal CLK finally. The period of the oscillator is determined by charging time of capacitors C1 and C2. The calculation formula of the oscillation periodic time is given by

$$T = 2\int_0^{V_T} \frac{C}{I} dV$$

C is the capacitance of capacitor C1 and C2 (C1=C2), I is the input currents. So the frequency control mechanisms of DCO are based upon the control of the input currents.

B. Digitally Controlled Current Source

It is mentioned that the frequency of DCO is determined by the input currents in last part. The digitally controlled current source is pivotal

Fig. 5 shows the digitally controlled current source circuit proposed in paper. It is composed of enable controlled circuit, bias current source, voltage reference with low-power consumption and current mirrors.

As for EN is "low", M12 and M13 are cut-off, bias current source can't provide current to the mirror branch; When EN is "high", the circuit work effectively. The current mirrors mosfets is composed of M19~M24 and M30~M32. The size ratios of M19~M24 are increased by two times while size ratios of M30~M32 are unchanged.

In the current reference circuit which uses low-voltage cascode structure provide a low voltage supply accommodation. In the circuit shown in Fig. 5, the gate of M8 and M9 is connected with the drain of M13, while the gate of M10 and M11 is connect with the output Vb of voltage reference with low-power consumption. At this low voltage cascode structure compared with ordinary cascode structure, it occupies a voltage margin is reduced from 2Vgs to Vgs, to accommodate low voltage supply conditions.

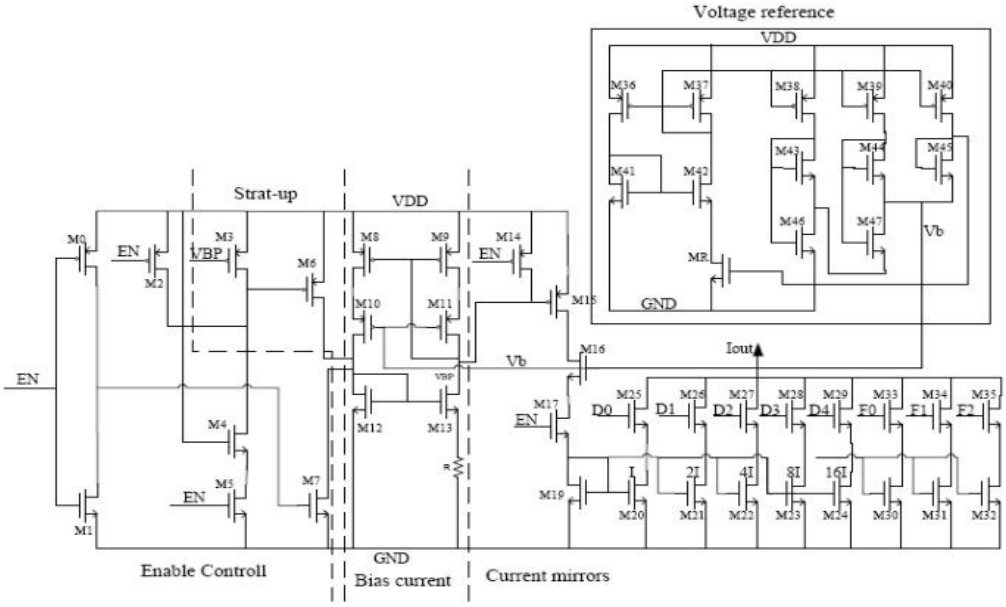


Figure 5. The digitally controlled current source circuit proposed in paper.

In the consideration of low power consumption, it is prerequisite to design special voltage bias circuit for low voltage cascode to provide bias voltage Vb. The circuit is illustrated in Fig. 6.

The circuit consists of a current source sub-circuit and a bias-voltage sub-circuit. The current source sub-circuit is a modified β multiplier self-biasing circuit that uses a MOS resistor MR instead of ordinary resistor. The bias-voltage sub-circuit consists of a transistor (M46) and two source-coupled pairs (M43-M47 and M44-M45). The gate-source voltages of M42 and M46 in the bias voltage sub-circuit and MR in the current source sub-circuit and current mirror form a closed loop [4]. All the MOSFETS in bias-voltage sub-circuit and current source sub-circuit except for MR are operated in the sub-threshold region for nA-level current consumption

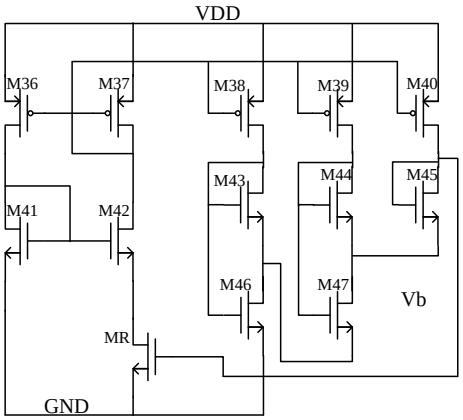


Figure 6. The voltage reference circuit with low power consumption

The subthreshold drain current of a MOSFET is an exponential function of the gate-source voltage Vgs and the drain-source Vds. The function is shown in Eq. (1).

$$I_d = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \times (1 - \exp(-\frac{V_{DS}}{V_T})) \quad (1)$$

$$I_0 = \mu C_{ox}(\eta - 1)V_T^2 \quad (2)$$

where μ is the carrier mobility, Cox is the gate-oxide capacitance, Vt is the thermal voltage and η is the subthreshold slope factor. For Vds > 0.1V, current Id is almost independent of Vds and given by

$$I_d = K \times I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad (3)$$

MOSFETS M36, M37, M38, M39 and M40 make up the current mirror. And the value of each current branch is given by Eq. (4).

$$I_P = \frac{V_{DSR1}}{R_{MR}} = \frac{V_{GS41} - V_{GS42}}{\frac{1}{K_{MR}\mu C_{ox}(V_{ref} - V_{TH})}}$$

$$= K_{MR}\mu C_{ox}(V_{ref} - V_{TH})\eta V_T \ln\left(\frac{K_{42}}{K_{41}}\right) \quad (4)$$

Therefore, we find that voltage of Vb of the circuit is given by Eq. (5). κ is the temperature coefficient of V_{TH}.

$$V_b = V_{GS46} - V_{GS43} + V_{GS47} - V_{GS44}$$

$$= V_{GS46} + \eta V_T \ln\left(\frac{2K_{43}K_{44}}{K_{47}}\right)$$

$$= V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_{38}I_0}\right) + \eta V_T \ln\left(\frac{2K_{43}K_{44}}{K_{47}}\right)$$

$$= V_{TH0} - \kappa T + \eta V_T \ln\left(\frac{3I_P}{K_{38}I_0}\right) + \eta V_T \ln\left(\frac{2K_{43}K_{44}}{K_{47}}\right) \quad (5)$$

III. Simulation

We accomplished the simulations by spectre in XFAB 0.35 μ m CMOS process and Fig. 7 shows the transient waveform of output clock signal in common supply voltage (3V), temperature (27°C) and corner (tm) by the

Coarse control bits is 110 and Fine control bits 00010. The frequency is 4.269MHz.

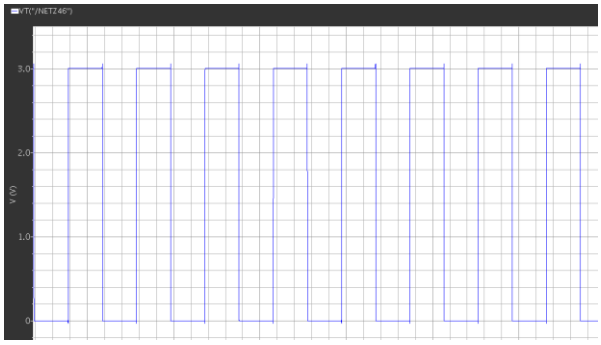


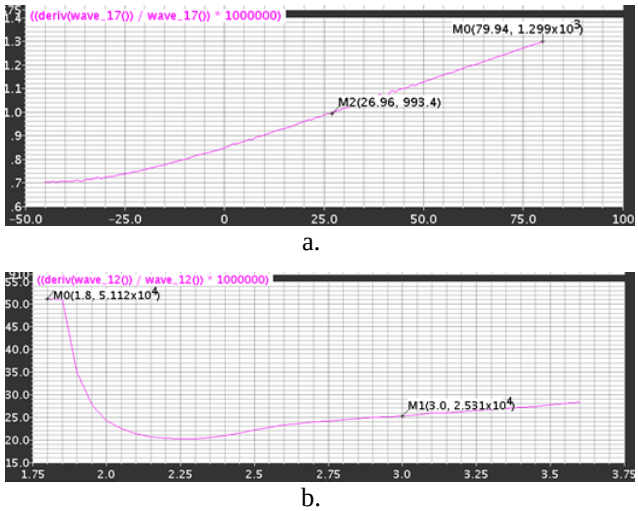
Figure 7. the transient waveform of output clock signal(F2~F0=110,N4~N0=00010,f=4.269MHz)

TABLE I. FREQUENCY IN DIFFERENT CONTROL BITS

Controll bits		Frequency (MHz)	Controll bits		Frequency(MHz)
F2~F0	N4~N0		F2~F0	N4~N0	
000	10000	1.006	110	00001	4.138
100	00000	2.004	110	00010	4.269
110	00000	4.008	110	00011	4.394
111	00000	6.009	110	00100	4.519
111	11111	8.009	110	00101	4.644

Table I shows frequency in different control bits. The coarse control bits F2~F0 increase the frequency by 2MHz when F2~F0 increase one bit effective. The fine control bits N4~N0 tunes the frequency between 0~2MHz, 2~4MHz, 4~6MHz and 6~8MHz. We can find that the frequency ranges of the coarse and fine tuning have a good linearity, which is a key factor of PLL performance.

Fig. 8 (a) shows the curve of frequency variation with voltage supply at 1MHz. Fig. 8 (b) shows the curve of frequency variation with temperature at 1MHz. The DCO proposed in this paper have a better temperature coefficient of variation than VDD coefficient of variation.



a.

b.

Figure 8. The curve of frequency variation with voltage supply(a) and temperature(b)

Table II show the comparison of performance parameters reported in some low power consumption oscillators in silicon. The current consumption in this paper is only 7.3 μ A at 1MHz and 31.8 μ A at 8MHz which are far than less the others. It shows that the DCO circuits proposed in this paper have an obvious advantage in the current consumption.

TABLE II. COMPARISON OF REPORTED LOW POWER CRYSTAL OSCILLATOR

	This work		[8]	[9]	[10]
Process(μm)	0.35		0.25	0.5	0.35
VDD(V)	3		2.5	3	1.8
Frequency(MHz)	1	8	7	11.6	5
Current Consumption(uA)	7.3	31.78	600	133	20
Variation with vdd(%)	±2.53@1.8-3.6V		±0.31@2.4-2.75V	±0.8@3V-5.5V	±0.95@1V-1.3V
Variation with temp(%)	±0.13@-40-85℃		±0.84@-40-125℃	±2.5@-40-125℃	±0.7@-20-60℃

IV. CONCLUSION

A low power 8-bits digitally controlled CMOS oscillator (DCO) design for low power consumption is presented. The presented DCO demonstrates a good robustness to process, voltage, and temperature variations and low power consumption comparing to the other designs. Simulation of the proposed DCO using 0.35 μ m XFAB CMOS Transistor Model achieves a frequency of 0MHz~ 8MHz and current consumption of 31.78 μ A at 8MHz, 7.3 μ A at 1MHz. Generally speaking, it can be applied for many low power consumption electronic systems.

REFERENCES

[1] R. E. Best, *Phase-Locked Loops: Theory, Design, and Applications*, New York: McGraw-Hill, 1984.

[2] B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design*, Wiley. com, 1996.

[3] C. C. Chung and C. Y. Lee, "An all-digital phase-locked loop for high-speed clock generation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 347-351, 2003.

[4] R. B. Staszewski and P. T. Balsara, "Phase-domain all-digital phase-locked loop," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 3, pp. 159-163, 2005.

[5] M. Saint-Laurent and G. P. Muyshondt, "A digitally controlled oscillator constructed using adjustable resistors," in *Proc. 2001 Southwest Symposium on Mixed-Signal Design*, 2001, pp. 80-82.

[6] P. Raha, *et al*., "A robust digital delay line architecture in a 0.13 μm CMOS technology node for reduced design and process sensitivities," in *Proc. 2002 IEEE International Symposium on Quality Electronic Design*, 2002, pp. 148-153.

[7] J. Zhao and Y. B. Kim, "A 12-bit digitally controlled oscillator with low power consumption," in *Proc. 2008 51st Midwest Symposium on Circuits and Systems*, 2008, pp. 370-373.

[8] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 433-442, 2006.

[9] A. V. Boas and A. Olmos, "A temperature compensated digitally trimmable on-chip IC oscillator with low voltage inhibit

capability," in *Proc. 2004 IEEE International Symposium on Circuits and Systems*, 2004, vol. 1.
[10] K. Lasanen, E. Raisanen-Ruotsalainen, and J. Kostamovaara, "A 1-V, self adjusting, 5-MHz CMOS RC-oscillator," in *Proc. 2002 IEEE International Symposium on Circuits and Systems*, vol. 4, 2002.

Qichao Zha was born in Jiujiang, Jiangxi province of China. He received the Bachelor of Science in microelectronics from Sichuan University. Now he is studying in Beijing Microelectronics Institute to get a Master degree in micro-electronics. His current research interests are the clock system of MCU in low power and low power line dropout regulator.

Tiejun Lu is a research associate in Beijing Microelectronics Institute. He is the chief engineer of BMIT now. He works mainly in the area of system architectural and low power design technology.

Yu Zong is a research associate in Beijing Microelectronics Institute. He works mainly in the area of low power design technology .He also has a lot of experience in USB interface design field.