# A Novel Two-Split Capacitor Array with Linearity Analysis for High-Resolution SAR ADCs

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***Abstract*—A novel two-split capacitor (T-SC) array structure for Successive Approximation Register (SAR) analog-to-digital converter (ADC) is proposed. When used as digital –to-analog converter (DAC), this circuit reduced the chip area by 27.7% in comparing with the conventional Split Capacitor (SC) at resolution=14. The area reduction effect can be more significant with the increasing resolution of ADC. The capacitor mismatch and parasitic effects of this proposed structure are analyzed in theory. Behavioral simulations were performed to demonstrate the effectiveness of this proposed structure. This simulation was only performed for capacitor mismatch. Simulation results show that T-SC array could achieve good binary-weighted performance and the standard deviation of its DNL was 0.51LSB when the standard deviation of capacitor was 0.025%. Furthermore, the analysis in this paper is provided for designers to make a tradeoff among resolution, CMOS process, circuit structure and capacitor size in their design of SAR ADC.**

***Index Terms*—capacitor DAC, capacitor mismatch, nonlinearity, SAR ADC, small area**

## I. Introduction

Recently, the Successive Approximation Register (SAR) analog-to-digital converter (ADC) has attracted more attentions again for that it features low power and area consumption due to its simple structure and least usage of analog circuit. Thus, it is used widely in today's System-on-Chip (SOC) solutions [1], [2], where requires low power, low cost, high speed and high density. As we all know, capacitor array DAC (CDAC) is used popularly in SAR ADC. For a binary-weighted capacitor array, as the resolution increases, a problem comes up: the total number of capacitors in CDAC will has an exponential increase. This will lead to increasing chip area, power dissipation as well as reducing speed due to a large charging time-constant. Obviously, it does not match case of SOC's requirements. To mitigate this problem, split capacitor array is used, which can reduce total number of capacitors. However, when the resolution is higher, this problem still exists and cannot be ignored.

This paper presents a novel two-split capacitor (T-SC) array structure based on conventional SC array. When used as digital-to-analog converter (DAC), this circuit reduced the chip area by 27.7% in comparing with the conventional Split Capacitor (SC) at resolution=14. Notably, the high speed performance advantage did not go away. The area reduction effect can be more significant with the increasing resolution of ADC. Thus, it can be used widely in high-speed and medium-to-high resolution SAR ADC. Because the data of the capacitor mismatch are usually available in statistical data, such as standard deviation [3], it is more practical to clarify the relationship between the standard deviation of the capacitor mismatch and the achievable ADC accuracy. In this paper, a statistical analysis has been made on the effect of capacitor mismatch on the SAR ADC resolution for these two capacitor array structure. Also, the roughly analysis of parasitic effect is included in this paper.

Manuscript received April 25, 2014; revised June 27, 2014.

## II. Overview of SAR ADC Operation

The architecture of a SAR ADC is shown in Fig. 1, consisting of a series of a CDAC, a comparator and successive approximation (SA) control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The CDAC is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage.

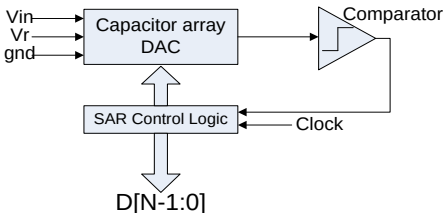


Figure 1. Simplified block diagram of a SAR ADC architecture

## III. Capacitor Array Structure and Analysis

### A. Structure

1) Conventional SC array

To solve the problem of capacitors spread resulting from the resolution increases, a popular SC array


doi: 10.12720/ijeee.3.3.177-181

structure was implemented to save the chip area and consequently mitigate the large power dissipation and low speed issue. Fig. 2 shows a SC array structure with N=h+m resolution, which utilizes an attenuation capacitor Ca to split the capacitor array into h bits 'H-segment' and m bit 'M-segment'. To improve matching performance, we choose integral multiples of unit capacitor Cu as Ca.

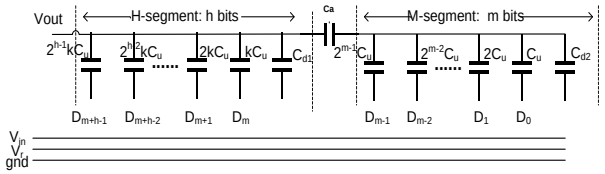


Figure 2. Conventional SC array

To satisfy binary-weighted requirements, we should assure

$$dV_m = 2dV_{m-1} \tag{1}$$

where $dV_m$, $dV_{m-1}$ is the variation of $V_{out}$ when $D_m$, $D_{m-1}$ equals 1, respectively. (That $D_m$, $D_{m-1}$ equals 1 means their corresponding capacitor connects to the reference voltage $Vr$).

Easily, we can calculate $dV_m$, $dV_{m-1}$ as

$$\begin{aligned} dV_m &= \frac{kC_u(C_a + C_{Mt})}{C_aC_{Mt} + C_{Ht}C_a + C_{Ht}C_{Mt}} \bullet V_r \\ dV_{m-1} &= \frac{2^{m-1}C_uC_a}{C_aC_{Mt} + C_{Ht}C_a + C_{Ht}C_{Mt}} \bullet V_r \\ C_{\mathrm{Ht}} &= (2^h - 1)kC_u + C_{d1} \\ C_{Mt} &= (2^m - 1)C_u + C_{d2} \end{aligned} \tag{2}$$

where $C_{Ht}$, $C_{Mt}$ represent the total number of capacitors in H-segment and M-segment, respectively. Then we could get the following equation, which ensures good performance of binary weight along with $Ca$ equaling integral multiples of $C_u$.

$$\frac{C_{d2}}{C_u} = \frac{2^m - k}{k}\frac{C_a}{C_u} - 2^m + 1 \tag{3}$$

From (3), we can conclude that the performance of binary weight has nothing to do with the value of $C_{d1}$ and h. That is to say, to achieve good linearity performance of CDAC, we just ensure that the value of $C_{d2}/C_u$, $k$, $C_a/C_u$, m is integer.

Meanwhile, to reduce the number of input capacitor, we can choose $C_{d1}=kC_u$ as sample capacitor instead of all capacitor in M-segment, which can cause only a gain error and no influence on linearity performance.

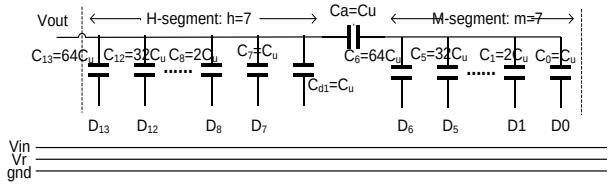


Figure 3. An example of 14-bit SC array DAC

An example of 14-bit SC array DAC is shown in Fig. 3. To achieve the smallest total number of capacitor, we choose h=m=7, k=1, Cd1=Cu, $C_{d2}$=0, Ca=Cu based on (3).

2) Novel T-SC array

Although SC array can reduce area of capacitor array, the area of capacitor array is still large when the resolution of CDAC is high. To achieve smaller total number of capacitors, we can modify the conventional SC array to a new T-SC array.

Design Highlights: The new design adds another array of capacitors by borrowing the capacitors from $C_{d2}$.

With the resolution of N=h+m+l, the T-SC array is illustrated in Fig. 4. It consists of three segments (H-(H-segment, M-segment and L-segment) and two attenuation capacitors ($C_{a1}$, $C_{a2}$). The parameters of k1, k2 represent the ratio of smallest capacitor in adjacent segment.

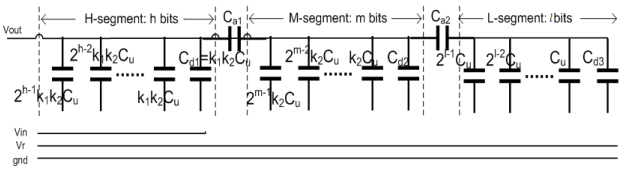


Figure 4. The T-SC array DAC

To ensure the value of $C_{a1}/C_u$, $C_{a2}/Cu$ is integer, we can design H-segment and M-segment first based on (3). The equation is as follows.

$$\frac{C_{d2}}{k_2C_u} = \frac{2^m - k_1}{k_1}\frac{C_{a1}}{k_2C_u} - 2^m + 1 \tag{4}$$

Then we can borrow $xC_u$ from $C_{d2}$, where $x$ is an uncertain integer and design M-segment and L-segment by use of (3) again.

$$\begin{aligned} \frac{\left[C_{d3} + (2^l - 1)C_u\right] \times C_{a2}}{C_{d3} + (2^l - 1)C_u + C_{a2}} &= xC_u \le C_{d2} \\ \frac{C_{d3}}{C_u} &= \frac{2^l - k_1}{k_1}\frac{C_{a2}}{C_u} - 2^l + 1 \end{aligned} \tag{5}$$

To make clear the following formulas, we define that $C_{a1}/C_u=a$, $C_{d2}/C_u=b$, $C_{a2}/C_u=p$, and $C_{d3}/C_u=q$. After simplifying formulas (4), (5), we can get formulas as follows, when we choose $p=2^l$.

$$\begin{cases} p = 2^l, \\ q = \dfrac{4^l}{k_2} - 2^{l+1} + 1, \\ x = 2^l - k_2, \\ b = \dfrac{(2^m - k_1)a}{k_1} - (2^m - 1)k_2 \end{cases} \tag{6}$$

where the condition is $0<x\le b$, and the value of $q$, $x$, $b$ is integer. Note that b is the value of $C_{d2}/C_u$ before borrowing. After we borrowing x from b, $C_{d2}/C_u$ equals $(b\text{-}x)$.

An example of 14-bit T-SC array DAC is shown in Fig. 5. To achieve the smallest total number of capacitor, we

choose h=6, m=5, l=3, $C_{d1}=C_u$, k1=k2=1, a=2, b=p=8 and q=49 based on (6).

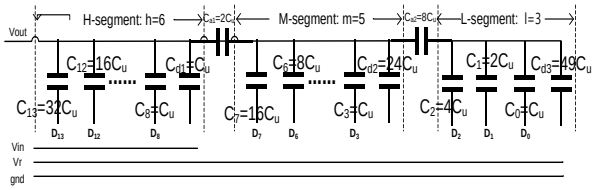


Figure 5. An example of 14-bit T-SC array DAC

where Ct is the total number of capacitors in CDAC.

TABLE I. OTHER DIVISION METHODS AT N=14

| | h | m | l | k1 | k2 | a | b-x | p | q | $C_t/C_u$ |
|---|---|---|---|---|---|---|---|---|---|---|
| N=14 | ***6*** | ***5*** | ***3*** | ***1*** | ***1*** | ***2*** | ***24*** | ***8*** | ***49*** | ***185*** |
| | 7 | 5 | 2 | 1 | 1 | 2 | 28 | 4 | 9 | 205 |
| | 6 | 6 | 2 | 1 | 1 | 2 | 60 | 4 | 9 | 205 |
| | 7 | 4 | 3 | 1 | 1 | 2 | 8 | 8 | 49 | 217 |
| | 6 | 5 | 3 | 1 | 1 | 3 | 55 | 8 | 49 | 217 |
| | There are many others not listing. | | | | | | | | | |

3) Comparation of total capacitors in two CDAC

In Fig. 3 and Fig. 5, the T-SC array can get $Ct=185C_u$, with area reduction of 27.7% in comparing with $Ct=256C_u$ in conventional SC array. The available smallest total capacitors Ct normalized by the unit capacitor versus the resolution of CDAC is plotted in Fig. 6. As we can see in Fig. 6, it is obvious that with the increasing resolution of CDAC, the area reduction effect can be more significant in theory.

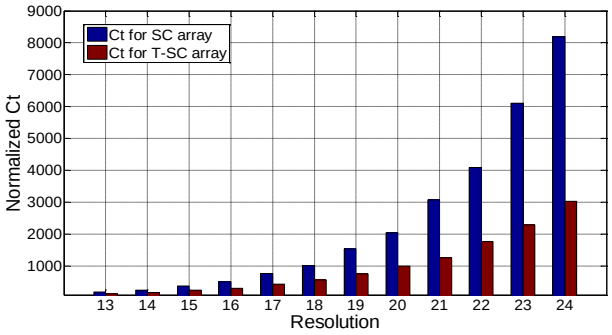


Figure 6. Normalized Ct versus the resolution of CDAC

## B. Linearity Analysis

1) Mismatch nonlinearity effect

The analysis of capacitor mismatch has been made in recent years [4], [5]. Since the effect of the capacitor mismatch in the L-segment is reduced to about $1/2^{m+h}$ and $1/2^h$ for T-SC and SC array respectively, the one in the H-segment dominates [5]. Therefore, as shown in Fig. 7, the following analysis only focuses on H-segment in 14-bit CDAC. For simplicity, it is assumed that all capacitors except in H-segment are connected to the ground and the initial charge is zero. The maximum error of $V_{out}$ caused by mismatch occurs during the code transition from '011…1' to '100…0' at the midpoint where the number of capacitors that change their state is maximal. To meet the ADC accuracy, this error must be smaller than a half least significant bit (LSB)($Vr/2^{14+1}$).

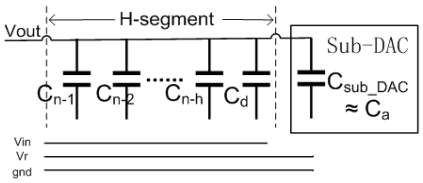


Figure 7. Simplified block focusing on H-segment

Then we can get the relation between capacitor mismatch requirement and resolution.

$$\text{T-SC array: } \frac{V_{DNL\_STD}}{V_r}=\frac{\sqrt{(2^h-1)k_1k_2}}{2^hk_1k_2+C_{a1}/C_u}\bullet\frac{\Delta C}{C_u}<\frac{1}{2}LSB=\frac{1}{2^{N+1}} \quad (7)$$

$$\text{SC array: } \frac{V_{DNL\_STD}}{V_r}=\frac{\sqrt{(2^m-1)k}}{2^mk+C_a/C_u}\bullet\frac{\Delta C}{C_u}<\frac{1}{2}LSB=\frac{1}{2^{N+1}} \quad (8)$$

where $\Delta C$ is the standard deviation of the unit capacitor and $V_{DNL\_STD}$ is the standard deviation of $V_{DNL}$.

Based on (3), (6), (7), (8), the required capacitor matching versus resolution plot for these two CDAC can be seen in Fig. 8. Curve 1 and curve 2 shows $\Delta C/C_u$ at smallest Ct in a conventional SC and T-SC array, respectively; and curve 3 shows the optimum $\Delta C/C_u$ of T-SC array when Ct of T-SC array is smaller than that of SC array.

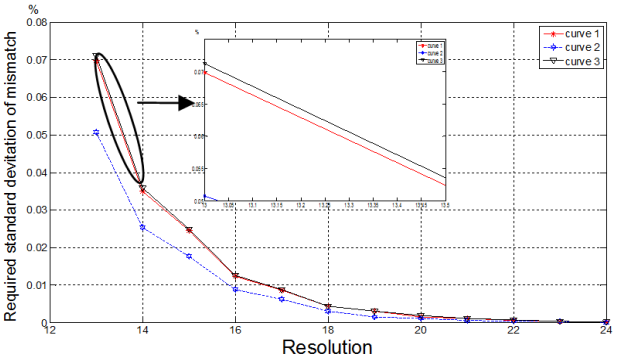


Figure 8. Required capacitor matching versus resolution for these two CDAC

As shown in Fig. 8, if reasonable values of h, k1, k2 and $C_{a1}$ are selected, T-SC array can achieve much smaller area than that of SC array, without the increase of mismatch requirement.

Also, compared with curve 3, curve 2 means smaller area, but stricter matching requirements. To relax the required capacitor matching, a segmented capacitor array [5] or capacitor calibration techniques [6] can be used.

2) Parasitic nonlinearity effect

Lots of efforts have been made on parasitic nonlinearity effect in SC array [4], [7], as is illustrated in Fig. 9(a).

The results in [4], [7] show that, the parasitic capacitance $C_{p2}$ degrades the linearity of the SAR ADC, while $C_{p1}$ can cause only a gain error and have no effect on the linearity performance. By reducing the number of bits in the M-segment, the size of $C_{Mt}$ can be minimized;

thus the nonlinearity effect can be alleviated. But this will enlarge the capacitor spread in H-segment.

As we all know, bottom-plate parasitic capacitance of a capacitor is bigger than that of top-plate. Thus, using results in [4], [7], capacitors in T-SC array can be distributed in Fig. 9(b), which can reduce the parasitic effect. To alleviate the parasitic effect further, the number of bits in the L-segment and M-segment should be chosen carefully with other parameters.

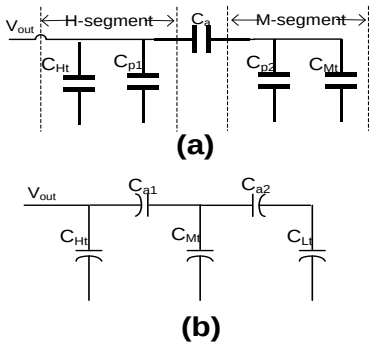


Figure 9. Analysis of parasitic nonlinearity effect in SC and T-SC array

## IV. Simulation Results

### A. Binary-Weighted Performance

To verify binary-weighted performance of T-SC array, the example in Fig. 5 is simulated at Vr=1V from D='00…01', '00…10' to '10…00'. As shown in Fig. 10, the results match the theoretical analysis perfectly.

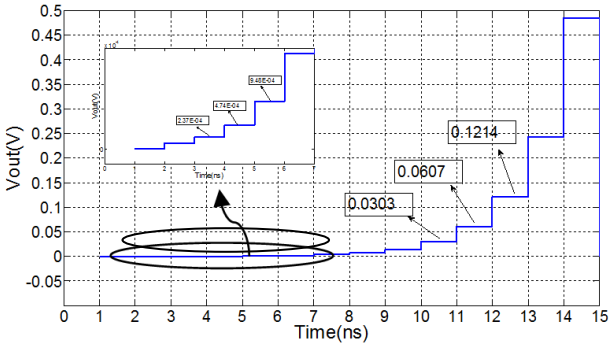


Figure10. Binary-weighted performance

### B. Behavioral Simulation For Capacitor Mismatch

In Fig. 5, to ensure $V_{DNL\_STD}$ is smaller than 1/2LSB, the theoretical value of capacitor mismatch is ΔC /Cu <0.025% for T-SC array.

Behavioral simulation of T-SC array in Fig. 5 is performed to verify the previous analysis. In simulation, it is assumed that the unit capacitor has a Gaussian distribution with standard deviation of 0.025% (ΔC /Cu <0.025%). Fig. 11 shows the result of 3000-time Monte Carlo runs, where the standard deviation of DNL and INL is plotted versus input code of CDAC. As expected, the maximum value of DNL is 0.51LSB, a little bigger than 1/2LSB.

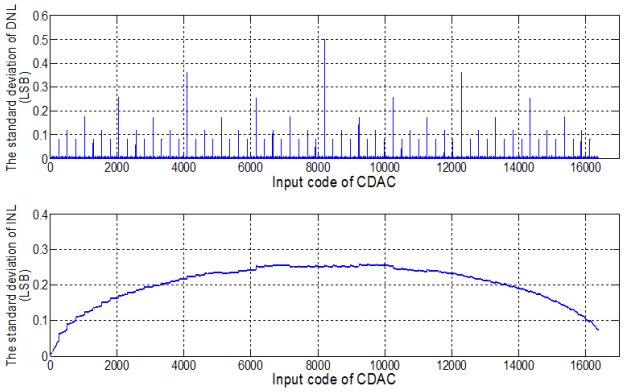


Figure 11. The standard deviation of DNL, INL versus input code of CDAC

## V. Conclusion

A novel two-split capacitor array has been proposed which can achieve area reduction effect in comparison with SC array. Theoretical analysis of the linearity performance was verified by comparing with the Monte-Carlo simulation results. Furthermore, the analysis in this paper is provided for designers to make a tradeoff among resolution, CMOS process, and capacitor area in their design of SAR ADC.

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