A Low-Quiescent Current Low-Dropout Regulator with Wide Input Range

Xueshuo Yang
Beijing Microelectronics Tech. Institute, Beijing, China
Email: yang74741@yeah.net

Tiejun Lu, Jianhui Zhang, and Yu Zong
Beijing Microelectronics Tech. Institute, Beijing, China
Email: lu_tie_jun, flying_chang}@163.com, zongyv@sina.com

***Abstract*—Low-quiescent current low-dropout regulator based on a two-stage amplifier with wide input range is presented. Every branch only consumes a little quiescent current by developing an extremely low current bias of 40nA. In addition, the stability of bandgap reference depends on the loop of LDO, which can simplify the circuit and reduce the number of branches to reduce current consumption. The proposed LDO can output a steady voltage of 3V as input voltage varies between 3.5V-24V. Thus it is an excellent choice for both battery-powered systems as well as industrial applications that see large line transients. And the quiescent current is virtually constant over the complete load current and ambient temperature range. The LDO with the proposed structure has been implemented in a 0.35-*um* Bi-CMOS process. It is able to deliver up to 150*m*A load current and only dissipates 3.6*u*A quiescent current at no-load and full-load condition. Good line regulation and load regulation are also achieved with max deviation voltage at output under 18*m*V.**

***Index Terms*—LDO, low-quiescent current, wide input range, line regulation, load regulation**

I. Introduction

In recent years, low-dropout liner regulator is widely used in the portable battery-powered electronic devices. It is especially suitable for applications that require low-noise and precision supply voltages with few off-chip components. Strong requirement on low power from portable electronic devices prompts LDO to develop with low quiescent current. In analog circuits, there are many current mirrors to control current consumption in every branch. Therefore, current bias decides the minimum quiescent current on some degree. Due to the emerging need of low-quiescent current LDO, many researchers have recently proposed many advanced methods to reduce bias current. For example, Filanovsky I.M. *et al.* proposed that MOSFET operating on subthreshold region replaces bipolar for power reduction [1]. Ka Nang Leung *et al.* proposed using different gate-source voltage between PMOS and NMOS [2]. Blauschild R *et al.* proposed a method combining depletion transistor and enhanced transistor which has opposite temperature coefficient [3]. In addition, wide input range can expand application scope of the LDO, not only on battery-powered systems but also on industrial products that see large line transients.

As a result, low-quiescent current, fast-transient and wide input range LDO should be developed. Solving the correlated tradeoffs on static-current, precision, recovery speed and space is the main challenge of the LDO design. The proposed circuit architecture is based on a two-stage amplifier and a PMOS transistor as the pass device to source high load current while achieving low dropout voltage. And the current reference operates on subthreshold region, and hence, the static current can be reduced significantly with easy integration.

In this paper, the proposed LDO structure will be given on section II, and then the bandgap reference and error amplifier will be introduced in section III, where the stability conditions and circuit design considerations are explained in detail, as well as the transient response enhancement circuits to reduce the time from full-load to no-load. Finally, the measurement results on some important specifications of the proposed LDO will be presented in section IV.

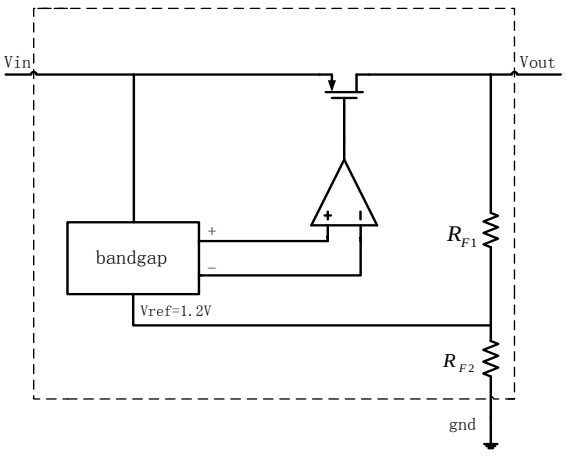

Figure 1. Structure of proposed LDO

II. Structure of Proposed LDO

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The structure of the proposed LDO, as shown in Fig. 1 is composed of a voltage reference, an error amplifier, a PMOS transistor, a feedback resistor network.

The bandgap reference can output a steady voltage of 1.2V and decide the output voltage of 3V based on the proportional relationship of feedback resistor network.

Only that the output voltage of bandgap is 1.2V, can the output current from two branches of bandgap reference be equal. If the current from the two branches are different, the differential current will magnify with the help of error amplifier and driver the power transistor. Then the power transistor provides corresponding output voltage by changing its conduction situation.

The proposed structure is quite different from traditional one which is shown in Fig. 2. The modules in two LDO structures are basically same. But in the traditional one, the error amplifier is a voltage amplifier while a transresistance amplifier is adopted in the proposed LDO. In the traditional one, there is another amplifier in the bandgap to ensure a steady reference voltage, thus it will dissipate more quiescent current compared with the proposed structure. From the standpoint of low-power, the proposed LDO is meaningful.

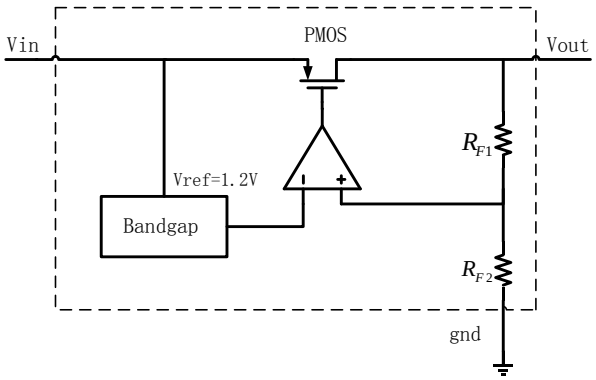

Figure 2. Structure of the traditional LDO

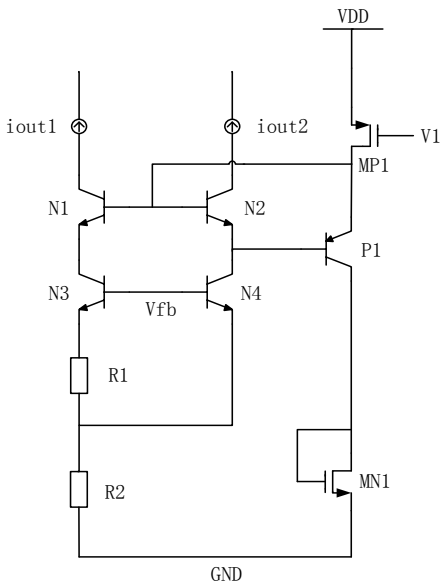

Figure 3. Bandgap reference

III. Module Design

A. Bandgap Reference

A bandgap reference which is free from temperature and voltage supply needs two parameters with opposite temperature coefficient to add together on proper weight. If two bipolar transistors operate in different current density, then ΔV_{BE} is proportional to temperature while the forward voltage of P-N junction diode has a negative temperature coefficient [4]. The structure of proposed bandgap reference is shown in Fig. 3.

Due that the base voltage of N3 and N4 is certain when their collector current is equal, it is chosen as the feedback point. When its voltage is not 1.2V, in other words, the voltage of output is not 3V, *iout1* and *iout2* will be different and the error amplifier will magnify the differential signal until the output voltage of LDO achieves the stable voltage of 3V.

Assuming that the collector current of N3 and N4 is equal, the voltage drop on resistance R1 is then given by

$$\Delta V_{BE} = V_T \ln N \tag{1}$$

The value of N is 8. So the current of resistance R_1 and reference voltage can be given by

$$I_1 = V_T \ln N / R_1 \tag{2}$$

$$V_{REF} = V_{be} + 2(R_2 / R_1) V_T \ln N \tag{3}$$

At room temperature,

$$\partial V_{be} / \partial T \approx -1.5mV / {}^{\circ}C \tag{4}$$

$$\partial V_T / \partial T \approx 0.087mV / {}^{\circ}C \tag{5}$$

If the temperature coefficient of reference voltage is zero, then α can be given as

$$\alpha = 2(R_2 / R_1) \ln N = 17.2 \tag{6}$$

Under this condition, the value of reference voltage is constant and it can be given by

$$V_{REF} = V_{be} + 17.2 V_T = 1.2V \tag{7}$$

B. Error Amplifier and Stability Analysis

The schematic of error amplifier and power stage is shown in Fig. 4. A bandgap reference is integrated together with the LDO to provide differential current to the input of error amplifier. In this LDO, PNP and NPN transistors are adopted to reduce *1/f* noise. But in the current mirror used to provide current and voltage bias, PMOS and NMOS are preferential for their low leakage current. Moreover, the use of a PNP transistor to implement emitter-follower as second stage is extremely critical to minimize the value of r_{o2}. As for the power stage, PMOS has obvious advantages compared with other type transistors for its low dropout voltage and low quiescent current [5].

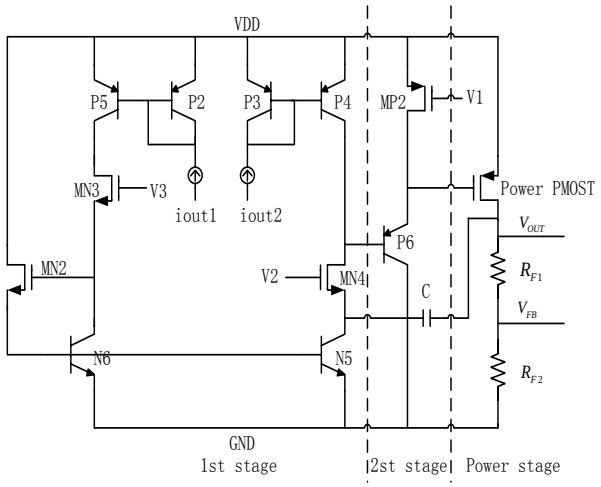

Figure 4. Error amplifier and power stage

The resulting structure can be viewed as a three-stage amplifier which is designed to have three separate poles. The stability of the proposed LDO is studied for two cases: $I_{OUT}=0$ and $I_{OUT}\neq 0$. When $I_{OUT}=0$, the transconductance g_{mp} and the output resistance r_{op} of the power PMOS is at the minimum and maximum, respectively. This is the worst case stability of the proposed compensation scheme. By setting proper parameters, the location of two non-dominant poles are both higher than the unity-gain frequency of the loop-gain transfer function in both the two cases, which guarantees the proposed LDO to achieve good phase margin and also can simplify the circuit to reduce quiescent consumption. But it is a tradeoff to achieve good phase margin both in the two load conditions as mentioned above.

C. Transient Response Enhancement Circuits

Due to low quiescent current in every branch, the slew rate of error amplifier is inevitably decreased. Load transient response is critical when there is a sudden change in load current, and a good load transient response results in minimal overshoots, as well as undershoot, and fast recovery time. In fact, the response time of an LDO depends on the slew rate at the gate drive of the power transistor and the loop-gain bandwidth. In this paper, two methods have been proposed to reduce the response time. The first method is illustrated in Fig. 5.

When the circuit operates on a certain state, N7 is cut off. But the moment load current changes from heavy-load to under-load, the gate voltage of power PMOS needs to be higher quickly because of less drain current of power PMOS. N7, a NPN transistor, as an emitter-follower can raise the gate voltage of power PMOS at a high speed. The parasitic capacitance of power PMOS is extremely large as a result of its large size. So the response time will be very long without the help of N7.

The second method is shown in Fig. 6. N9, N10 and N8 can be viewed as a differential amplifier. When this circuit operates on a certain state, the base voltage of N9 is much higher compared with Vo1 which is the output of first stage of the error amplifier. Therefore, the emitter current of N9 makes up the majority of the collector current of N8. But the moment load current changes from heavy-load to under-load, Vo1 will be higher than the base voltage of N9 and the emitter current of N10 makes up the majority of the collector current of N8.

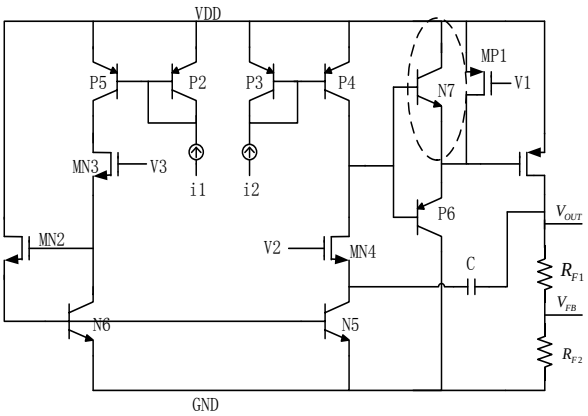

Figure 5. The first method to reduce transient response time

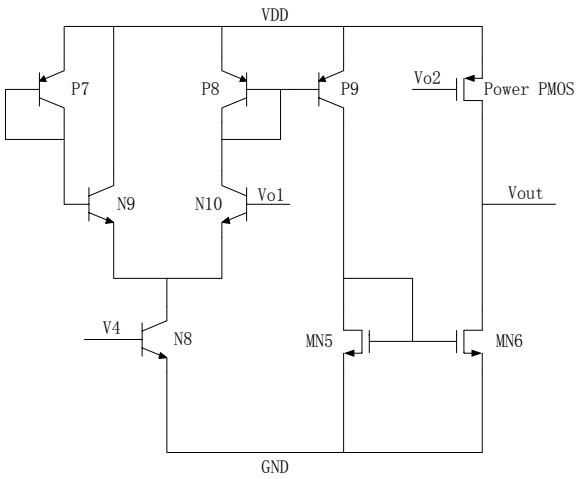

Figure 6. The second method to reduce transient response time

In addition, P9 mirrors the current of N10 and MN6 mirrors the current of P9 at an amplifying ratio. In this condition, MN2 can discharge the output capacitance quickly and enhance the transient response speed. The reason why choosing a relatively great mirror ratio is that N8 always works and distributing a smaller current to N8 can reduce quiescent current of the LDO. In this way, fast transient response and low static current will be achieved at the same time.

IV. Simulation Result and Conclusion

The proposed LDO has been implemented in a 0.35-*um* Bi-CMOS process and its micrograph is shown in Fig. 7. The chip area is 1048 *um**755*um* with high voltage Dongbu TiTek process. The LDO is capable of operating on a wide input range from 3.5V to 24 V and only consuming 3-4 *uA* ground current independent of load conditions, which is shown in Fig. 8. And it can output a steady voltage of 3V with little deviation which is demonstrated in Fig. 9. Fig. 10 shows the simulated phase

margin of the loop-gain transfer function under different load currents. The minimum phase margin is always larger than 55° for the entire range of the load current. The detailed performance of the LDO is summarized in Table I.

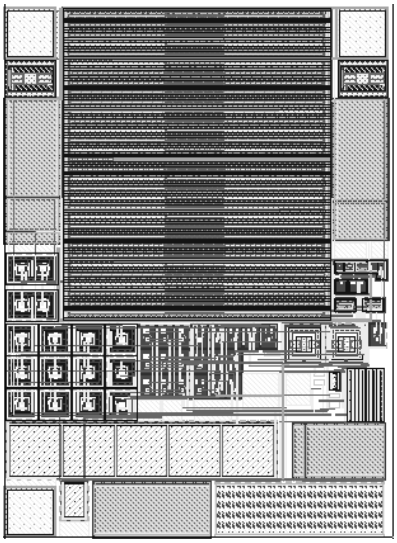

Figure 7. Micrograph of the proposed LDO

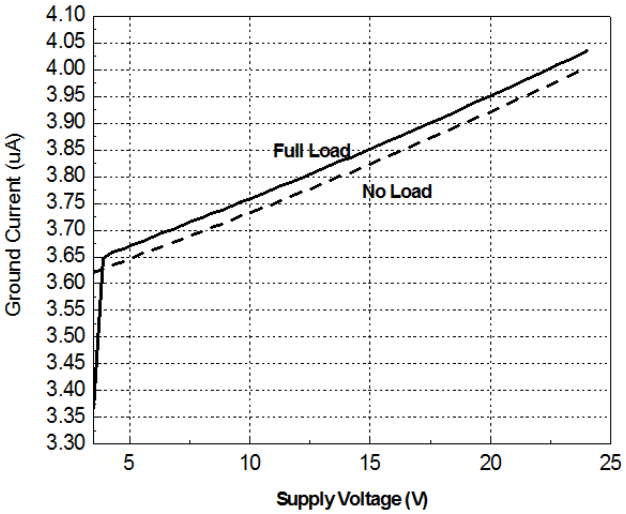

Figure 8. Ground current under different input voltage and load condition

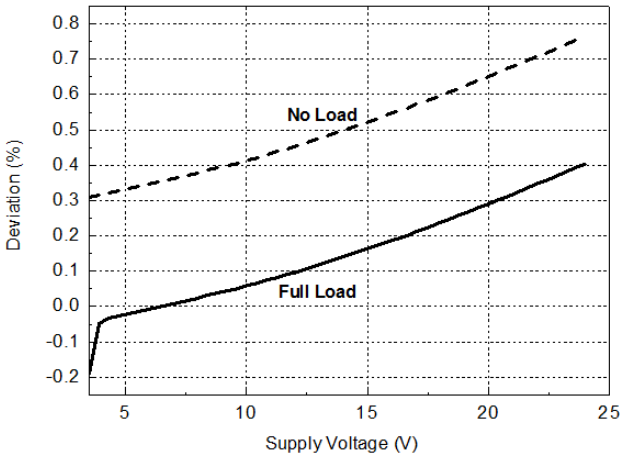

Figure 9. Simulated line and load regulations

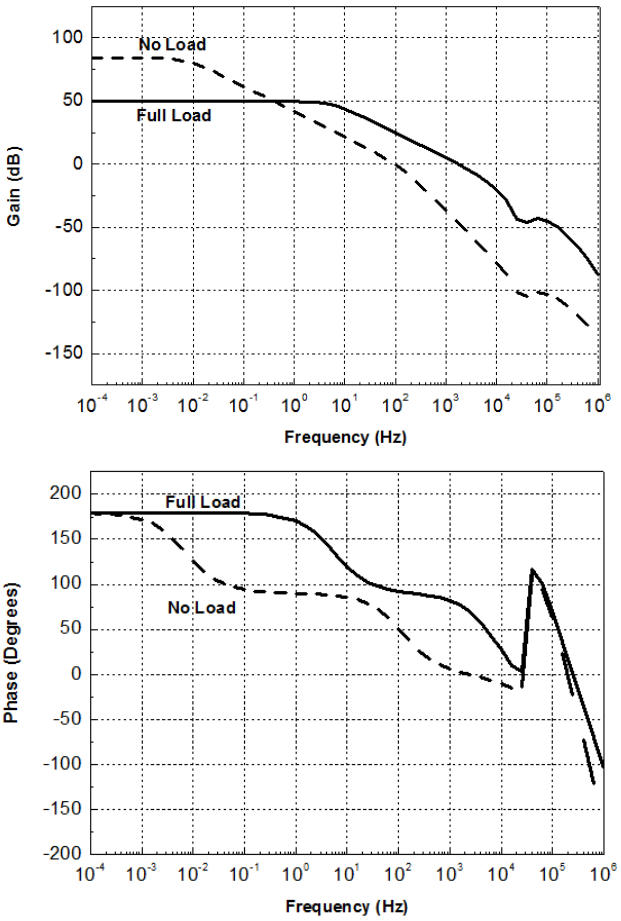

Figure 10. Simulated loop-gain transfer function of proposed LDO

The obvious advantage is the low static current consumption with such wide input range and basically independent of load conditions. Another innovation point is a new LDO structure as mentioned in Fig. 1. And it has been taped out.

TABLE I. SUMMARY OF SIMULATION RESULT

parameter		value
Technology		Dongbu TiTek 0.35um Bi-CMOS
Input Voltage		3.5V to 24V
Temperature Range		-40 °C ~125 °C
Output Voltage		3V
Output Current		1.5uA to 150mA
Dropout Voltage		200mV@150mA
Ground Current		3.649uA@1.5uA and V_{IN}=5V 3.673uA@150mA and V_{IN}=5V
Output Capacitance		10uF
Line Regulation		0.88mV/V@150mA
Load Regulation		-0.067mV/V@V_{IN}=5V
Loop Gain		84.48dB@1.5uA 49.88dB@150mA
Load Transient Response		360mV@1.5uA to 150mA
Line Transient Response		91mV@V_{IN}=3.5V to 24V
PSRR	f=2kHz	43.78dB@1.5uA 19.79 dB@150mA
	f=100kHz	103.17 dB@1.5uA 59.28 dB@150mA
Active Chip Area		1048 um*755um

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Xueshuo Yang was born in 1989, China. She is currently pursuing the M.S. in Microelectronics Engineering at Beijing Microelectronics Tech Institution. She focuses on low-power and area reduction design. In just two years, her talents and work have been recognized by leaders in this field.

Tiejun Lu was born in 1963, China. He has received PhD degree and currently serves as the chief engineer at Beijing Microelectronics Tech Institution.

Jianhui Zhang was born in 1978, China. He is dedicated to the research of power management in integrated circuits at Beijing Microelectronics Tech Institution.

Yu Zong was born in 1973, China. He is dedicated to the research of MCU at Beijing Microelectronics Tech Institution. He has brought along industry insight and an upper level system view.