Designing Phase Locked Loop by Design of Experiments

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***Abstract*—Designing of Phase Locked Loop (PLL) by Design of Experiments (DOE) using Response Surface Methodology (RSM) is presented. Dependence of various design parameters on the three performance characteristics of interest that are Root-Mean-Square-Jitter (RMS-Jitter), Reference Spur level, and Lock time was investigated. Second-order models for RMS-Jitter and Reference Spur level in addition to a first-order with interaction model for Lock time were fitted. Optimization was done to minimize all the three output responses simultaneously using desirability function method and the optimized design was justified experimentally. Experiments were done by simulation using ADIsimPLL provided from Analog Devices.**

***Index Terms*—design of experiments, response surface methodology, RMS-jitter, spurs, lock time**

I. Introduction

In Phase Locked Loop (PLL) circuit design there are many performance characteristics to be satisfied simultaneously e.g. Root-Mean-Square-Jitter (RMS-Jitter), Spurs, Lock time etc. While taking all these characteristics into account, choosing the design parameters of the loop is one of the most difficult steps in PLL circuit design, Fig. 1 shows the basic PLL. There are many of the formulas that are commonly used for PLL design [1], [2]. However even after the analytical calculations to obtain the best result for an output response, the results may vary in simulations. In addition there is no specific method for choosing the design parameters of the PLL circuit that will optimize more than one response output simultaneously. This can be done by Design of Experiments (DOE).

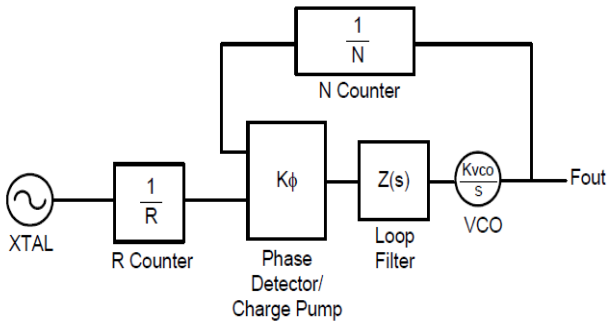

Figure 1. The basic PLL.

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In this paper the use of DOE and Response Surface Methodology (RSM) to investigate the dependence of various design parameters on RMS-Jitter, Reference Spur, and Lock Time of PLL is presented. Therefore in section II a brief review of DOE and its basic statistical analysis tools and the commonly used second-order response surface designs is given. Then in section III the use of D-optimal design to fit second-order models between the design parameters and two of the performance characteristics of interest that are RMS-Jitter and Reference Spur in addition to a first-order with interaction model for the third that is Lock time is illustrated. The associated statistical analysis and optimization to minimize all the three output responses simultaneously along with the results of the justification experiment are also shown in this section. The conclusion and suggestions for future work are given in section IV.

II. Design of Experiment

DOE has been widely and successfully used in a variety of scientific and engineering fields to identify those design parameters (factors) that significantly affect the performance of a system, and to develop a statistical relationship between the factors and the performance characteristic. In general, such a relationship is unknown but can be approximated by a low-degree polynomial model. After the experiments, the parameters of the fitted model can be estimated by the Ordinary Least Square (OLS) method and the effects of the factors can be calculated by Analysis of Variance (ANOVA) [3].

RSMis a collection of mathematical and statistical techniques useful for the modeling and analysis of problems in which a response of interest is influenced by several factors and the objective is to optimize this response [4], [5]. The standard response surface designs such as the central composite design, the Box-Behnken design, and their variations (such as the face-centered cube) are widely used for fitting a second-order model because they are quite general and flexible designs [6]. Occasionally, an experimenter may need to reduce the number of runs required by a standard response surface design. Computer-generated designs can be used for this purpose [7]. Much of the development of computer-generated designs is an outgrowth of work by Kiefer (1959, 1961) and Kiefer and Wolfowitz (1959) in the theory of optimal designs [8].There is several popular design optimality criteria, perhaps the most widely used

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is the D-optimality criterion. A design is said to be D-optimal if $|(X'X)^{-1}|$ is minimized, where X is the model matrix [9].Simultaneous consideration of multiple responses involves first building an appropriate response surface model for each response and then trying to find a set of operating conditions that in some sense optimizes all responses or at least keeps them in desired range. A useful approach to optimization of multiple responses is to use the simultaneous optimization technique that makes use of desirability functions [10].

TABLE I. DESIGN PARAMETERS AND THEIR VALUES AT DIFFERENT LEVELS

factor	Name	Unit	Type	Low	High	Mean
A	Bandwidth	kHz	Numeric	265	755	510
B	Divider N		Numeric	300	500	400
C	Phase Margin	deg	Numeric	40	60	50
D	CP Current	mA	Numeric	2.19	4.06	3.13
E	Filter Order		categoric	2	4	3

TABLE II. D-OPTIMAL DESIGN ARRAY USED FOR SIMULATIONS

Std	Run	Bandwidth	Divider	Phase margin	CP Current	Filter Order
2	1	265.00	300.00	40.00	2.19	4
28	2	510.00	400.00	45.00	3.13	2
1	3	755.00	500.00	60.00	4.06	4
23	4	265.00	300.00	60.00	2.19	3
3	5	265.00	500.00	60.00	4.06	3
4	6	755.00	500.00	40.00	4.06	3
24	7	755.00	500.00	60.00	2.19	3
8	8	755.00	300.00	40.00	4.06	4
7	9	755.00	500.00	40.00	3.13	2
29	10	510.00	300.00	40.00	2.19	3
10	11	755.00	300.00	50.00	4.06	2
13	12	265.00	500.00	50.00	2.19	2
15	13	755.00	300.00	60.00	4.06	3
27	14	510.00	500.00	50.00	3.13	4
14	15	265.00	300.00	40.00	4.06	3
33	16	755.00	500.00	40.00	3.13	2
18	17	755.00	400.00	50.00	3.13	3
34	18	755.00	500.00	40.00	2.19	4
19	19	755.00	500.00	40.00	2.19	4
20	20	755.00	300.00	60.00	2.19	4

TABLE III. SIMULATION RESULTS OF EXPERIMENTS

Run	RMS-Jitter (deg)	Reference Spur (dBc)	Lock Time (usec)
1	0.75	-26	80.2
2	1.03	5	84.4
3	1.1	18	80
4	0.65	-17	80.2
5	0.8	-5	80.2
6	1.34	13	80
7	1.1	23	80
8	1.06	-2.6	80.1
9	1.34	16	Did not lock
10	0.96	-6	80.1
11	0.95	3.1	83.4
12	0.84	3.7	86
13	0.86	3	80
14	1.1	9.3	80.1
15	0.74	-28	80.3
16	1.34	16	Did not lock
17	1.08	11	80
18	1.35	19	80
19	1.35	19	80
20	0.88	8.2	80

III. PLL AND DOE

A. Performance Characteristics and Factors

The Performance characteristics for the analysis are RMS-Jitter, Reference Spur, and Lock Time. The affecting factors were chosen by the design. All factors are 3 level numerical factors, except for the Filter Order factor that is categorical 3 level one. The five design parameters are Bandwidth (kHz), Divider (N), Phase Margin (degree), Charge Pump (CP) Current (mA), and Filter Order. Table I shows the values at different levels for these design factors.

The standard full CCD design used for fitting a second-order model of the design parameters will require $2^4(16)$ factorial points, 5 center points, and 8 axial points, a total of 29 runs for the numeric factors. This design will be duplicated for every combination of the 3 levels of the categorical factor yielding a design with 87 runs. Also the small (fractional) CCD design will require $2^{4-1}(8)$ factorial points, 5 center points, and 8 axial points, a total of 21 runs for the numeric factors, duplicated for every combination of the 3 levels of the categorical factor, a design with 63 runs yields. However the models have at most 25 terms, so we want a design with fewer trials. Computer-generated designs can be used for this purpose. A D-Optimal deign consisting of 35 runs was used for fitting a second-order model for RMS-Jitter and Reference Spur and a first-order with interaction model for Lock time. Table II shows some of the runs of the constructed design. Results of the corresponding simulations are shown in Table III. There are three outputs shown in Table III which are RMS-Jitter, Reference Spur, and Lock Time. The design is generated using Design-Expert software package.

From Table III we see that there are cases for which the PLL did not lock. These have been treated as missing data and the corresponding treatment combinations have been ignored in the analysis of Lock time output.

B. Statistical Analysis

ANOVA was used to determine the significance of the control factors, and OLS to estimate the parameters of the following suggested models for the three performance characteristics of interest:

$$RMS\text{-}Jitter = \alpha_0 + \sum_i \alpha_i X_i + \sum_{i<j} \alpha_{ij} X_i X_j + \sum_i \alpha_{ii} X_i^2 \quad (1)$$

where α's are the model parameters to be estimated and X's are the affecting factors.

$$Reference\ Spur = \beta_0 + \sum_i \beta_i X_i + \sum_{i<j} \beta_{ij} X_i X_j + \sum_i \beta_{ii} X_i^2 \quad (2)$$

where β's are the model parameters to be estimated and X's are the affecting factors.

$$Lock\ Time = \delta_0 + \sum_i \delta_i X_i + \sum_{i<j} \delta_{ij} X_i X_j \quad (3)$$

where δ's are the model parameters to be estimated and X's are the affecting factors.

Table IV, V, and VI show the parameters estimate of the significant model terms along with their standard

error and 95% confidence limits for RMS-Jitter, Reference Spur level, and Lock Time respectively.

TABLE IV. RMS-JITTER SIGNIFICANT TERMS

Term	Parameter Estimate	df	Standard Error	95% CI Low	95% CI High
Intercept	0.99	1	3.144E-3	0.98	0.99
A	0.16	1	1.085E-3	0.15	0.16
B	0.11	1	1.040E-3	0.11	0.11
C	-0.082	1	1.184E-3	-0.085	-0.079
D	-2.465E-3	1	1.163E-3	-5.057E-3	1.274E-4
E [1]	-9.699E-3	1	1.570E-3	-0.013	-6.2E-3
E [2]	-3.371E-4	1	1.393E-3	-3.442E-3	2.768E-3
AB	0.020	1	1.256E-3	0.017	0.023
AC	0.028	1	1.223E-3	-0.031	-0.026
AE [1]	6.676E-003	1	1.719E-3	2.846E-3	0.011
AE [2]	-1.539E-3	1	1.536E-3	-4.961E-3	1.882E-3
BC	-0.010	1	1.179E-3	-0.013	-7.5E-3
CD	-3.238E-3	1	1.152E-3	-5.804E-3	-6.71E-4
DE [1]	4.233E-003	1	1.862E-3	8.524E-5	8.381E-3
DE [2]	1.956E-003	1	1.592E-3	-1.591E-3	5.503E-3
A^2	-0.059	1	3.501E-3	-0.067	-0.051
C^2	0.014	1	3.067E-3	7.371E-3	0.021

TABLE V. REFERENCE SPUR SIGNIFICANT TERMS

Term	Parameter Estimate	df	Standard Error	95% CI Low	95% CI High
Intercept	3.08	1	0.22	2.60	3.57
A	11.32	1	0.075	11.15	11.49
B	7.69	1	0.072	7.53	7.85
C	2.26	1	0.082	2.08	2.44
D	-2.70	1	0.081	-2.88	-2.52
E [1]	3.35	1	0.11	3.10	3.59
E [2]	-1.04	1	0.096	-1.26	-0.83
AB	-0.82	1	0.087	-1.02	-0.63
AE [1]	-3.00	1	0.12	-3.27	-2.74
AE [2]	0.87	1	0.11	0.64	1.11
BE [1]	-1.37	1	0.10	-1.60	-1.13
BE [2]	0.29	1	0.10	0.069	0.52
CE [1]	-0.58	1	0.13	-0.86	-0.30
CE [2]	0.23	1	0.11	-8.278E-3	0.47
A^2	-3.07	1	0.24	-3.61	-2.53
D^2	-0.65	1	0.25	-1.21	-0.085

TABLE VI. LOCK TIME SIGNIFICANT TERMS

Term	Parameter Estimate	df	Standard Error	95% CI Low	95% CI High
Intercept	81.33	1	0.27	80.73	81.94
A	0.7	1	0.3	0.036	1.37
E [1]	2.48	1	0.47	1.43	3.52
E [2]	-1.24	1	0.33	-1.98	-0.5
AE [1]	1.67	1	0.5	0.56	2.79
AE [2]	-0.9	1	0.36	-1.71	-0.085

The fitted model in Table IV can be used to estimate the RMS-Jitter at any setting of the design parameters in the design region. From this model it is clear that with narrower bandwith and smaller divider value, significant reduction in RMS-Jitter can be obtained. This result coincide with the results from the theoretical studies about RMS-Jitter. The fitted model will be used in the subsequent optimization procedure.

The fitted model in Table V can be used to estimate the reference spur level at any setting of the design parameters in the design region. From this model it is clear that bandwidth, divider value, phase margin, CP-current, and filter order all affect significantlly the reference spur level with bandwidth and divider value the most important. This result coincide with the results from the theoretical studies about reference spur level. The model will be used in the subsequent optimization procedure.

The fitted model in Table VI can be used to estimate the lock time at any setting of the design parameters in the design region. From this model it is clear that with wider bandwidth and filter order 3 or 4, a significanr reduction in lock time can be obtained. The other design parameters have nonsignificant effect on lock time. This result coincide with the results from the theoretical studies about lock time. The model will be used in the subsequent optimization procedure.

C. Optimization

Optimization of the three outputs was done by the simultaneous optimization technique popularized by Derringer and Suich (1980). This procedure makes use of desirability functions**.** The general approach is to first convert each output y_i into an individual desirability function d_i that varies over the range $0 \le d_i \le 1$, where if the output y_i is at its goal or target, then $d_i = 1$, and if the response is outside an acceptable region, $d_i = 0$. Then the design parameters are chosen to maximize the overall desirability $D = (d_1 . d_2 . d_3)^{1/3}$. As the target for the output is a minimum value:

$$d = \begin{cases} 1 & y < T \\ \left(\frac{U-y}{U-T}\right)^r & T \le y \le U \\ 0 & y > U \end{cases} \quad (4)$$

With weight r = 1 to obtain linear desirability function, T = 0.6, -28, and 80, U = 1.35, 23, and 86, for the output responses RMS-Jitter, Reference Spur, and Lock Time respectively. The Design-Expert software package was used to solve this optimization problem using the desirability function approach. Table VII shows the first three suggested solutions.

TABLE VII. THE FIRST THREE SUGGESTED SOLUTIONS

N	Bandwidth	Divider	Phase margin	CP Current	Filter Order	RMS-Jitter	Reference Spur	Lock Time	Desirability
1	**265**	**300**	**57.97**	**4.06**	**L4**	**0.65323**	**-26.6398**	**80.2778**	**0.952**
2	265.28	300	55.54	4.06	L4	0.65941	-27.4016	80.3571	0.949
3	265	300	55.14	4.02	L4	0.660571	-27.3921	80.3662	0.948

D. Justification Experiment

The first suggested solution was justified using the ADIsimPLL. Table VIII and Fig. 2 show the results for phase noise at 3.00 GHz. These results are equivalent to phase jitter using brick wall filter from 1.0 Hz to 1.0 MHz equal to 0.66 degrees rms. Fig. 3 shows the results for the first three spurs' levels which are -26 dBc, -49 dBc, and -62 dBc respectively. And Fig. 4 shows the results for time to lock to 46.8 MHz that is 80.2 usec. The obtained results are very close to those obtained by optimization which suggests the correctness of the method.

TABLE VIII. PHASE NOISE TABLE

Freq	Total	VCO	Ref	Chip	SDM	SDM
100	-81.4	-131.0	--	-81.40	--	-167.2
1.0k	-90.94	-129.3	--	-90.94	--	-147.2
10.0k	-97.85	-127.7	--	-97.86	--	-127.3
100k	-98.41	-120.1	--	-98.64	--	-111.8
1.00M	-112.6	-132.3	--	-113.0	--	-123.2

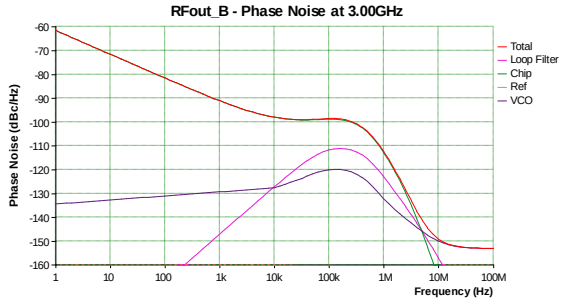

Figure 2. Phase noise at 3.0GHz.

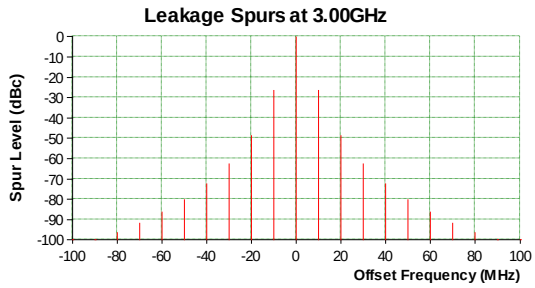

Figure 3. Leakage spurs at 3.0 GHz.

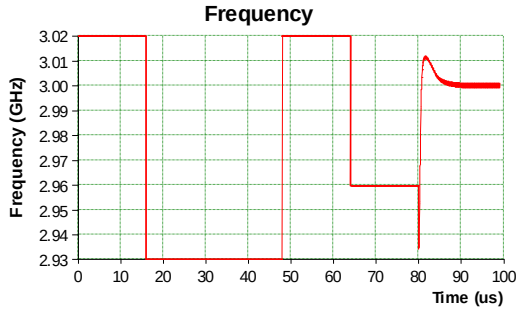

Figure 4. Time to lock to 46.8 MHz.

IV. CONCLUSION AND FUTURE WORK

Design of Experiments and Response Surface Methodology were used in designing phase locked loop to choose the design parameters values that will simultaneously minimize the three performance characteristics of interest that are RMS-Jitter, Reference Spur, and Lock Time. Analysis of Variance (ANOVA) was used to determine the significance of each of the design parameters, and Ordinary Least square (OLS) to estimate the parameters of the fitted models. Desirability function approach was used to simultaneously minimize the three outputs. Experiments were done by simulation using ADIsimPLL, and a justification experiment was done for the first solution suggested by optimization. The results were very close. In this work all the affecting factors were design factors. A future work could be done to take noise factors such as thermal noise and vibration-induced noise into account to obtain an optimized PLL system that will also be robust to noise conditions.

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