

A Linear CMOS Low Drop-Out Voltage Regulator in a 0.6 μm CMOS Technology

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Abstract—In most of integrated circuits, especially in Analog/Digital mixed ICs, low dropout voltage regulators are needed to provide a robust, reliable and capable voltage supply. In this paper, a very low dropout and adjustable voltage regulator design in a 0.6 μm CMOS technology is presented. Along with theoretical background, design steps, building blocks and simulation results were explained. Our designed voltage regulator works with 8V supply voltage and can give 3V-5V user selectable output voltage with 50 mA load current capability. Output dropout is 0.5mV for maximum load. For temperature range of -40C^0 to 85C^0 , output change is less than 5mV, and for a $\pm 10\%$ supply change, output change is less than 0.02mV.

Index Terms—low dropout (LDO) voltage regulator, bandgap reference, opamp, analog integrated circuit

I. INTRODUCTION

Voltage regulation is the process of holding a voltage steady under conditions of changing applied voltage, load currents, temperature and etc. Many electronic systems like phones, MP3 players, digital cameras and laptops require a stable power supply voltage. Besides, for the applications such as RF IC, audio IC and some interface electronics which require low noise designs, suitable voltage regulator are essential [1], [2].

Low dropout (LDO) regulators provide high current efficiency, low noise, high accuracy, fast response performance, clean power sources at a cheaper cost, and low standby current due to the absence of switching.

Today's higher complexity in portable electronic devices and distributed power sourcing systems, define many important problems which should be solved in the power management to guarantee the correct operation of the circuit.

LDO voltage regulators are used in many parts of the circuits and if they cannot turn loads on and off anytime in the circuit, system's power consumption will be increased and reversely the battery lifetime will be decreased. Hence, in order to provide a well regulated output current at the given voltage, a fast transient response and a decreased supply voltage are required.

The typical structure of a LDO voltage regulator with series-shunt negative feedback is shown in Fig. 1. It consists of a reference voltage for scaling the output voltage and comparing it to the reference, a series pass

transistor (bipolar or FET) and an error amplifier with feedback resistors R1 and R2 which their voltage drop is controlled by the amplifier to maintain the output at a required value and constitute the regulation loop.

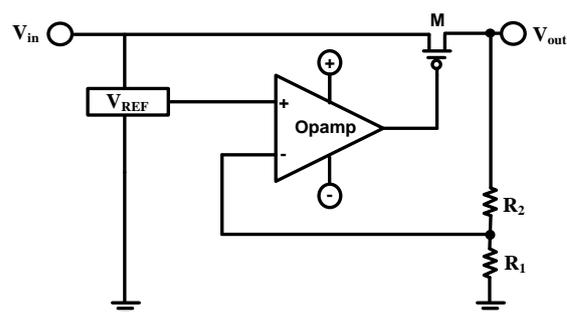


Figure 1. LDO voltage regulator

The reference voltage which can be a zener diode or bandgap reference provides a stable DC bias voltage with limited current driving capabilities. The zener diodes are suitable in high voltage circuits since bandgap references are used for low voltage and high accuracy applications. Low drift references and low input offset voltage amplifiers are preferred, because the temperature dependency of the reference and the amplifier's input offset voltage define the overall temperature coefficient of the regulator.

The error amplifier and PMOS transistor form a voltage-controlled current source. The output voltage, V_{OUT} , is scaled down by the voltage divider (R_1 , R_2) and compared to the reference voltage (V_{REF}) while the error amplifier's output controls an enhancement-mode PMOS transistor.

The drop-out voltage can be defined as the difference between the output and input voltages at which the circuit quits regulation with further reductions in input voltage. The output voltage drop-out depends on load current and junction temperature of the pass transistor.

In this paper we propose a very low-dropout, precision voltage regulator, which is designed in 0.6 μm CMOS technology and is supposed to generate 3V or 5V depending on user configuration, from the nominal 8V supply input.

II. PROPOSED LDO VOLTAGE REGULATOR

The proposed low dropout voltage regulator in this paper consists of an output stage, an error amplifier

opamp, a bandgap reference circuit and a startup circuit. The basic building blocks and their theoretical backgrounds have been introduced in this section.

A. Opamp

Opamp is a very important part of many analog electronic circuits. In low dropout regulators, opamps are used in output stages as the error amplifier in negative feedback configuration or in bandgap reference to provide good supply rejection. For a good performance, designed opamps should have high gain, low input offset voltage, high output swing and good stability. In the proposed regulator circuits, opamp is designed in folded cascode topology. Folded cascode is chosen because it provides good output swing and stability [3]. Fig. 2 shows the designed folded cascode opamp.

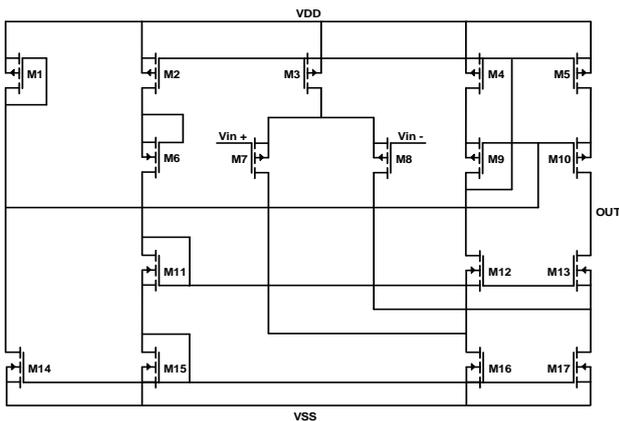


Figure 2. Schematic of designed folded cascode opamp circuit

In proposed topology, M7 and M8 are PMOS input transistors. Although, they decrease the gain, PMOS inputs used in folded cascode widely because of their low noise characteristic and low leakage current [3]. The M7 and M8 are designed as large devices to provide high gain. Most of the times cascoded current mirrors are used in folded cascode opamps. In traditional cascoded PMOS current mirrors, the output swing is limited by the $V_{DD} - 2V_{OV} - V_{TH}$ in the upper side. In this opamp, a low voltage cascode current mirror is implemented [3]. Low voltage cascode mirror needs an external biasing to operate properly. With correct biasing, the voltage swing increases to $V_{DD} - 2V_{OV}$ which is two threshold voltages higher than the old configuration [4]. The M4, M9, M5 and, M10 are the transistors for the low voltage cascode mirror. The biasing has been done using M1 and M14. For the correct biasing, the same current is obtained at the current mirror and biasing transistors.

TABLE I. SIZE OF THE OPAMP TRANSISTORS

	M1	M2	M3	M4	M5	M6
W (μm)	12.5	3	22	50	50	1
L (μm)	3	0.6	3	3	3	10
	M7	M8	M9	M10	M11	M12
W (μm)	100	100	50	50	2	40
L (μm)	3	3	3	3	0.6	3
	M13	M14	M15	M16	M17	
W (μm)	40	20	2	20	20	
L (μm)	3	6	0.6	3	3	

The size of M1 has been chosen one quarter of M4 and M5 to provide $2V_{OV}$ for the gates of M9 and M10. M2, M6, M11 and, M15 transistors constitute the self-biasing stage which is used for the biasing of the opamp. The sizes of the transistors are given in the Table I.

The gain, phase and output swing of the designed opamp were obtained using some simulations. For AC simulation a 2pF load capacitor was used. The gain and phase response of the opamp have been shown in Fig. 3. The gain of the opamp is 82dB with the gain bandwidth product of 23.4MHz, and the phase margin is 60° . Since we have a load capacitor which is larger than 2pF, this phase margin ensures the stable operation of the opamp. The output swing characteristic can be seen in the Fig. 4. From the DC simulation it can be seen that, output can swing up to 7.5V in the upper side and, 1.5V in the lower side for 8V supply. For the opamp, the upper side of our regulator is more important than the lower side, because we control a PMOS pass element in the output and opamp must go to high levels to cut-off the current for low load currents.

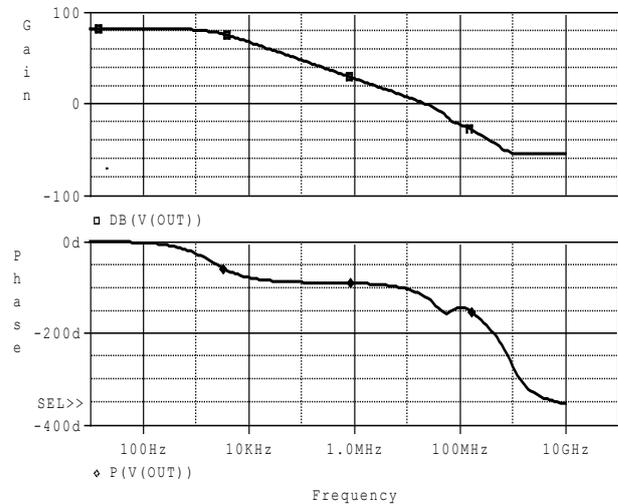


Figure 3. Frequency response of the opamp

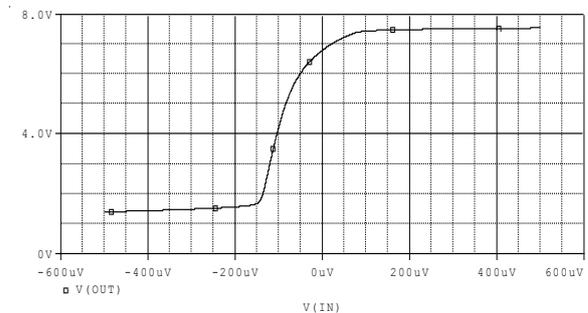


Figure 4. Opamp input/output characteristic

B. Bandgap Reference

Bandgap references are designed to provide temperature and supply insensitive references. Zener diodes are also good voltage references but they provide high voltages and are incompatible with ICs. Bandgap references can be implemented easily in IC technology. The principle behind the bandgap reference is adding up

the voltages which have negative and positive temperature coefficients (TC) to get a zero temperature coefficient output. The negative TC is supplied from a forward biased BJT's base-emitter potential. The positive TC is supplied from a kT/q reference. A kT/q reference can be obtained from differentially taken base-emitter potentials. At the temperature point which the bandgap circuit provides zero TC, the voltage seen at the output of circuit is very close to the bandgap of the silicon (1.22 eV) [5]. The designed bandgap reference circuit for this voltage regulator has been shown in Fig. 5.

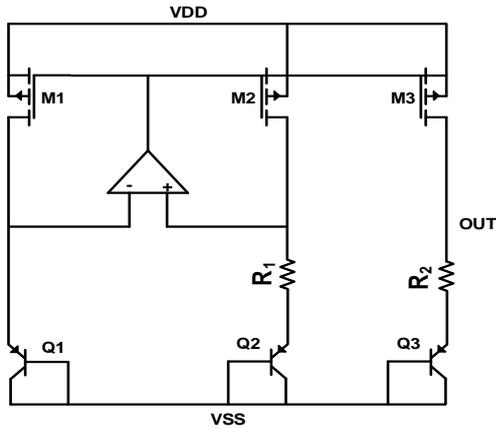


Figure 5. Schematic of designed bandgap reference circuit

For the bandgap reference circuit in Fig. 5, the current flowing from the emitters of Q1, Q2 and Q3 are same since a current mirror which consists of M1, M2, and M3 has been used. The voltages at the drains of M1 and M2 are brought to be same using an opamp. So;

$$R_1 I_{E2} = V_{BE1} - V_{BE2} \quad (1)$$

$$R_1 I_{E2} = \frac{KT}{q} \ln \frac{I_{S2}}{I_{S1}} \quad (2)$$

Since Q1 and Q2 are identical except their junction areas and saturation currents are proportional to the junction areas, we can write;

$$V_{OUT} = V_{BE3} + \frac{R_2}{R_1} \frac{KT}{q} \ln \frac{A_2}{A_1} \quad (3)$$

For a temperature insensitive output voltage;

$$\frac{dV_{OUT}}{dT} = 0 \quad (4)$$

Since;

$$\frac{dV_{OUT}}{dT} = \frac{dV_{BE3}}{dT} + \frac{R_2}{R_1} \frac{KT}{q} \ln \frac{A_2}{A_1} \quad (5)$$

The TC (temperature coefficients) of the V_{BE3} is nearly -1.5 mV/K° but our BJTs have different TCs from this value. By adjusting R_2 , R_1 , A_2 and A_1 we can bring the TC of V_T to cancel out the TC of V_{BE3} . The zero TC

adjustment is found by some simulations. The simulation result for the TC is shown in Fig. 6. TC is set to be zero in 22.5°C with an output voltage of 1.1609V. Another simulation has been done for the supply rejection. Since we want minimum supply rejection, the topology is chosen appropriately. For supply rejection simulation, the supply voltage swept between 7.2V and 8.8V. Simulation results for supply rejection can be seen in the Fig. 7. The maximum output change for the 7.2V-8.8V supply sweep is 0.02mV.

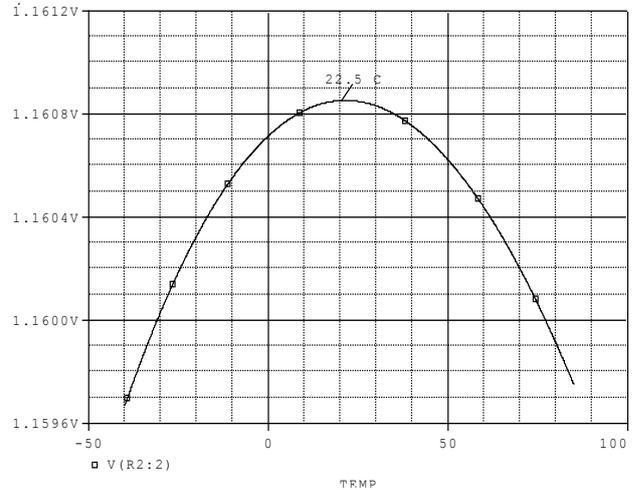


Figure 6. Bandgap reference temperature characteristic

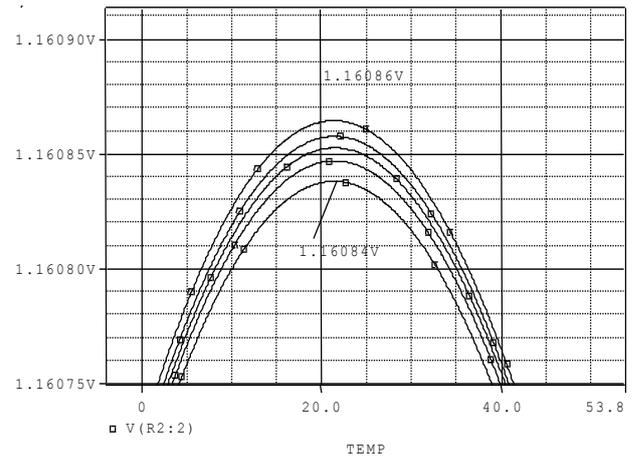


Figure 7. Bandgap reference supply rejection

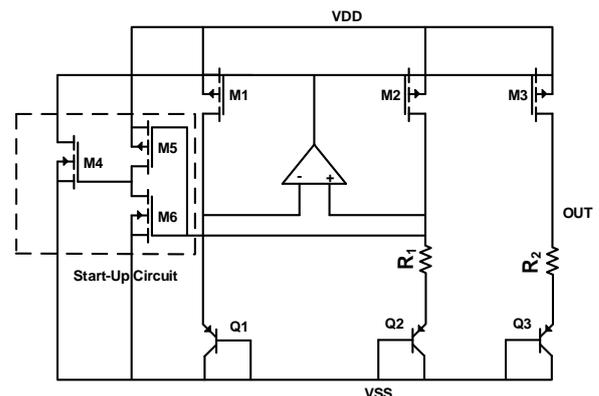


Figure 8. Schematic of the Bandgap reference with start-up circuit

C. Start-Up Circuit

The bandgap references have two different operating points. One is correct operation and other is the zero current operating point which we don't want. To bring the operation of bandgap references to the correct point in zero current case, start-up circuits are used. In this bandgap reference, a very basic start-up circuit was used [6]. Bandgap reference circuit with the start-up topology has been shown in the Fig. 8.

If the bandgap circuit is stuck at zero current operation, opamp input voltages, V_P and V_N will be zero. In this case M6 will work in cutoff region and M5 will work in triode region. In this case gate of the M4 will be brought to V_{DD} and the drain of the M4 will be brought to V_{SS} . Because the gates of M1, M2 and, M3 is brought to V_{SS} , these transistors will start to operate in saturation region and they will pass current. Once the bandgap reference is started, V_P and V_N rise to higher voltages and this will pull the drain of M6 to V_{SS} and cut off the M4.

D. Output Stage

Output stage of the proposed regulator consists of a PMOS transistor as a pass element, an opamp as an error amplifier and a resistive voltage divider as feedback element. The output stage schematic can be seen in the Fig. 9.

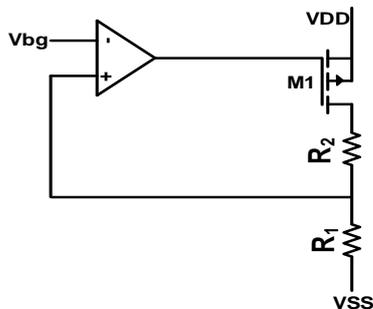


Figure 9. Schematic of the output stage of the voltage regulator

The R1 transistor is used inside the IC and its value is 1kΩ. R2 resistor can be used to obtain adjustable voltage output. Our bandgap reference gives an output voltage of 1.16V. So, for 3V output R2 should be 1.58kΩ and for 5V output R2 should be 3.3kΩ.

The design of the pass transistor is also important. The difference between low dropout regulators and standard regulators is their pass transistor topology. In standard regulators, common drain structure is used but in LDO regulators, connected in common source topology should be used. By this way, the transistor will supply current with a V_{DSAT} dropout voltage. This transistor should be designed to be a large device to supply large loads [7]. In our design, we used a 1000μm/0.6μm PMOS transistor.

III. SIMULATION RESULTS

To simulate overall structure, all designed modules are gathered. Parasitic inductors which are coming from bonding wires are also added. These parasitic effects are modeled as inductors with 1nH inductances.

A. Load Capability

The required load capability for our regulator specified as maximum 50mA with a maximum 10mV. To assess load capability, we swept load current from 0 to 50mA for 3V output and 5V output configurations. Simulation results are presented in Fig. 10 and Fig. 11.

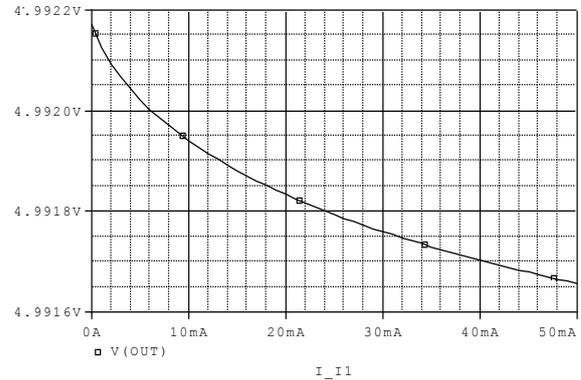


Figure 10. Output dropout voltage versus load current for 5V output

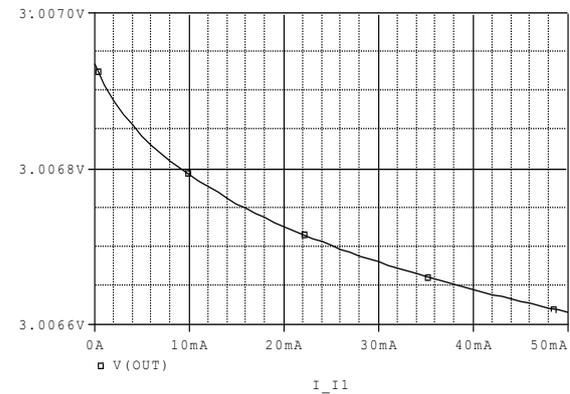


Figure 11. Output dropout voltage versus load current for 3V output

Fig. 10 and Fig. 11 shows that the regulator has a dropout of 0.5mV for 50mA load current in both 3V and 5V outputs. Designed voltage regulator is capable of supplying 440mA current for 3V output and 310mA current for 5V output with 10mV dropout.

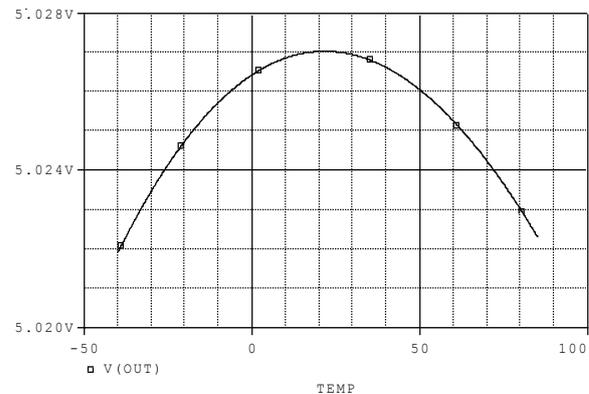


Figure 12. Output voltage versus temperature for 5V output

B. Temperature Sensitivity

To understand the temperature sensitivity of designed voltage regulator, temperature is swept between -40C⁰

and 85C⁰. The temperature simulations have been done using maximum load current (50mA) condition. Simulation results are presented in Fig. 12 and Fig. 13.

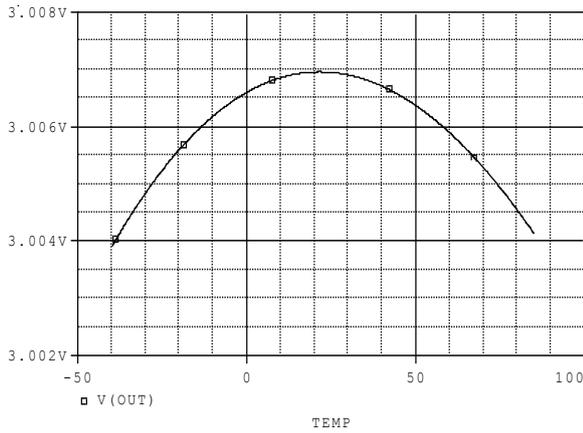


Figure 13. Output voltage versus temperature for 3V output

Fig. 12 shows that for 5V and 3V output, between -40C⁰ and 85C⁰, output voltage change is maximum 5mV and 3mV, respectively. The maximum output voltage change occurs at temperature ranges between -40C⁰ to 22C⁰ and 22C⁰ to 85C⁰. Though, the bandgap designed to show zero temperature coefficients in 22C⁰. Also the minimum voltage changes can be obtained in this temperature.

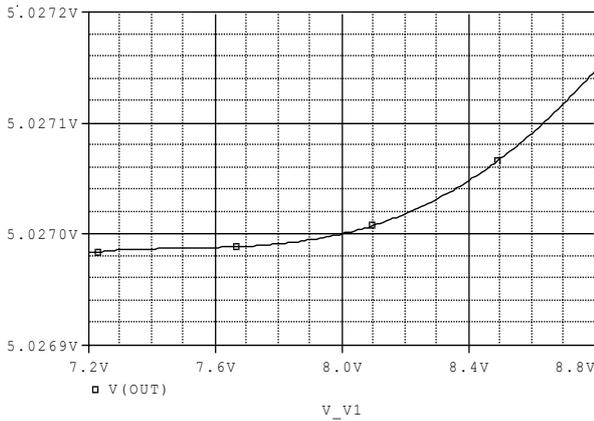


Figure 14. Output voltage versus supply voltage for 5V output

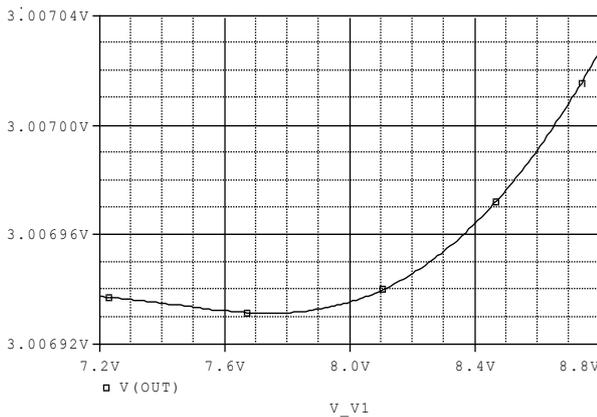


Figure 15. Output Voltage versus supply voltage for 3V output

C. Supply Sensitivity

Supply sensitivity is assessed by changing supply voltage by +/-10%. Our regulator is designed to operate in 8V supply voltage. So in simulations, supply is varied between 7.2V and 8.8V. All supply sensitivity simulations have been done using minimum load (0A) condition. This condition is the worst case because, PMOS pass transistor is very large and it can difficultly controls the low currents. Simulation results are presented in Fig. 14 and Fig. 15.

From Fig. 14 and Fig. 15, it can be seen that the designed voltage regulator has very good supply insensitivity. In the supply voltage range of 7.2V-8.8V, for 5V and 3V configurations, the output voltage change is 0.17mV and 0.1mV, respectively.

Another important parameter for a voltage regulator is Power Supply Rejection Ratio (PSRR). PSRR is a figure of merit which shows how the noise in the supply voltage reflects to the output [5]. PSRR formula is given in Equation 6 where the V_{nSupply} is the supply noise and V_{nOutput} is the output noise.

$$PSRR = 20 \log \frac{|V_{nSupply}|}{|V_{nOutput}|} \quad (6)$$

The PSRR simulation result can be seen in Fig. 16. The PSRR of the designed regulator is 85.6dB for 1 kHz noise bandwidth. This means, the noise in the voltage supply reflects output after being attenuated by 85.6dB in the 1 kHz bandwidth

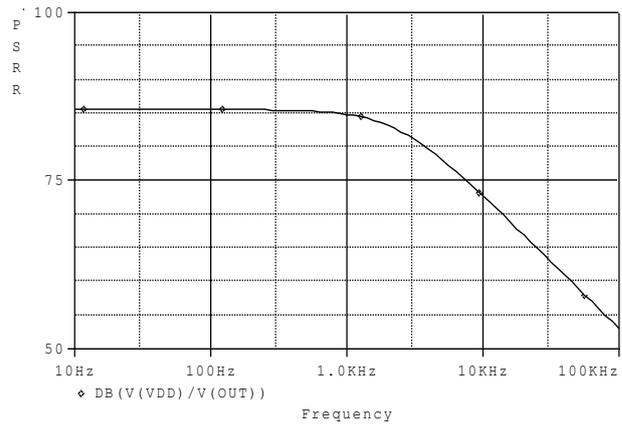


Figure 16. PSRR simulation result

IV. CONCLUSION

A low dropout and adjustable linear CMOS voltage regulator was designed and simulated. Designed regulator can supply 3V to 5V which is user selectable. An opamp, a bandgap reference and a pass transistor were designed. Simulations have been done to assess performance of the regulator. Simulations are based on supply, temperature and load sweeping. Noise performance is also assessed by simulations. Important specifications of the designed regulator are given in the Table II.

TABLE II. LDO VOLTAGE REGULATOR SPECIFICATIONS

Specification	Value
Supply Voltage	8V
Regulated Voltage	3V-5V (user selectable)
Source Current Capability	50 mA
Regulated Voltage Change w.r.t. Temperature (-40C ⁰ to 85C ⁰)	5mV for 3V Output 3mV for 5V Output
Regulated Voltage Change w.r.t. Supply Voltage (+/-10%)	0.10mV for 3V Output 0.17mV for 5V Output
Regulated Voltage Change Under Maximum Load	0.5mV for 3V Output 0.5mV for 5V Output
PSRR	85.6dB for 1kHz Bandwidth

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Mohammad Maadi was born in Macoo, Iran. He received the B.S. degree in 2007 from IAU and the M.S. degree in 2013 from Middle East Technical University; both degrees were in electrical and electronics engineering. From 2007 to 2010, he worked as an electronics engineer and project manager in some private companies of Iran. He could get the membership of the Iranian Inventors Association after registering his B.S. project, "Intelligent Color Recognizer and Analyzer System", as an invention in the General Department of Industrial Ownerships of Iran in 2008. From 2011 to 2013, he got TUBITAK scholarship as a Research Assistant in the Department of Electrical and Electronics Engineering at Middle East Technical University. During his M.S., he mainly focused on integrated circuit design for flip-chip bonded capacitive micromachined ultrasonic transducers (CMUTs). His research interests include integrated circuit design for ultrasound 3D imaging and therapeutic CMUT arrays, design of analog, digital and mixed-signal integrated circuits and design of micro electromechanical systems (MEMS) for medical applications.