Standard Cell Transistor Level ATPG Coverage

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***Abstract*—A study of components field failure rate over the years shows reduction in failure rates of various component [1] while another study [2] shows only 20% the percentage of system meeting reliability requirement from 1996 to 2000. The contradict observation between two studies drives the need to understand the system testability not only from logic gate functional perspective but the true coverage from transistor level as well. In the automotive semiconductors industry, the target tolerated field failure rates is zero percentage and the defect parts per million, DPM for automotive semiconductor is 1DPM. Hence there is a need to put more efforts on device, board and system level testability in order to deliver a consistently reliable and cost effective product to market. This paper will analyze the standard cell's ATPG coverage at transistor level with commercial ATPG tool. Hopefully the finding will benefit the readers.**

***Index Terms*—standard cell, ATPG modeling, transistor**

I. INTRODUCTION

Test is a mechanism to verify the device under test (DUT) is correctly manufactured. Study [1] has shown that the measured field failure rate of different component has improved over the years in Fig. 1 while the study [2] from 1996 to 2000 shows that only 20% of the systems meeting the reliability requirement in Fig. 2.

From Fig. 1 and Fig. 2, it shows that improved components measured field failure rate over the years does not improve the system reliability for operational tests. Hence there is a need to have a more in depth understanding of component coverage improvement over the years.

As each market segments have different reliability requirements, as shown in Table I. A clear understanding of the requirement will help the designer to improve the product reliability to cater the needs of various industries.

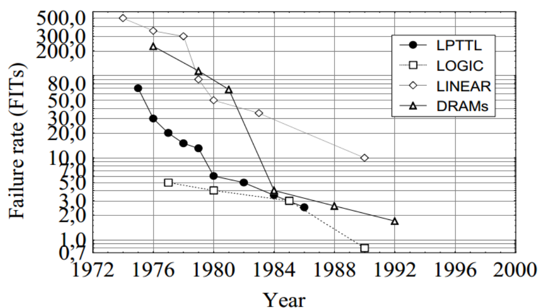

Figure 1. Component's measured field failure rate [1]

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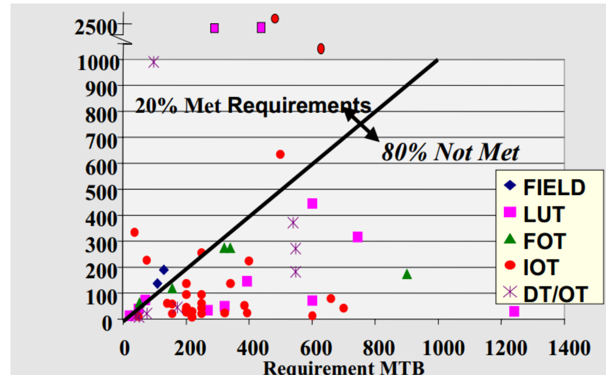

Figure 2. Demonstrated reliability versus requirements for operational tests, 1996-2000 [2]

TABLE I. RELIABILITY REQUIREMENT FOR DIFFERENT MARKET SEGMENT

Segment	Consumer	Industrial	Automotive
Temperature	0^{0}C ->40^{0}C	-10^{0}C -> 70^{0}C	-40^{0}C -> 85^{0}C /155^{0}C
Operation Time	1-3 years	5-10 years	Up to 15 years
Humidity	low	environment	0% -> 100%
Tolerated field failure rates	< 10%	<< 1%	Target: zero failure
Documentation	none	conditional	true
Supply	none	Up to 5 years	Up to 30 years

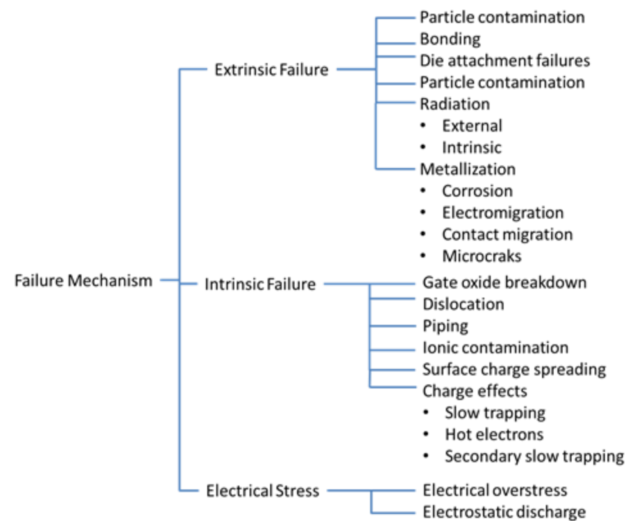

Figure 3. Failure mechanism [3]-[12]

For chip failures, it can be generalized as 3 classes shown in Fig. 3:

- **Extrinsic failure**: Extrinsic failures originate in the packaging and interconnection processes.
- **Intrinsic failure**: Intrinsic failures inherent to the die itself and typically caused during wafer fabrication

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- **Electrical stress failure**: Electrical stress failures are caused by poor design or careless handling

Till now, for stuck at fault coverage, the major idea is to present a gate level model to the automatic test pattern generator including the cell-aware library modeling [13], ATPG tool to generate patterns to detect physical defects as close to the gate model as possible. The library model generation from transistor level equivalent to the gate level representation is done through non-commercial tool like GateMaker [14]. GateMaker is a tool developed by IBM and Intel which generate the gate level models from schematics. GateMaker use path tracing to map groups of transistors to a channel connected component and paths pruning to simplify the circuit to a final equivalent form. The success of GateMaker and the adoption is proven previously [15], [16].

Previous researches on transistor level ATPG fault coverage, mainly focus on the ATPG generation technique at transistor level circuit through [17]-[19]:

- Custom generation tool
- Circuit modification during ATPG generation

In this paper, the scope of discussion will be standard cell transistor level automatic test pattern generator, ATPG coverage correlation using the commercial ATPG tool. The modeling and generation methodology is beyond the scope of discussion in this paper. The analysis of standard cell transistor level coverage will be partition by:

- Universal logic function
- Input's width of logic
- Logic's architecture
- Logic's drive strength

Hopefully, the readers can benefit from the sharing.

II. Transistor Level ATPG Flow

The transistor level ATPG flow is shown in Fig. 4.

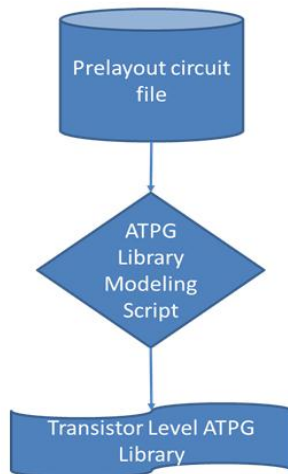

Figure 4. Standard cell transistor level library generator

The transistor level modeling with Z-propagation removal technique in commercial ATPG tool will not be discussed in this paper. Special care is needed in translating the NMOS and PMOS transistor in the circuit file, as the direction of the MOS's drain and source contacts in spice modeling is interchangeable, while the direction for MOS's drain and source contact in Verilog primitive is fixed. The illustration is shown in Fig. 5.

```
Spice Instantiation:
INST DRN GATE SRC BULK NMOS
Verilog Instantiation:
nmos  INST (out,data,control);
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Figure 5. MOS instantiation

The ATPG coverage extraction flow is shown in Fig. 6.

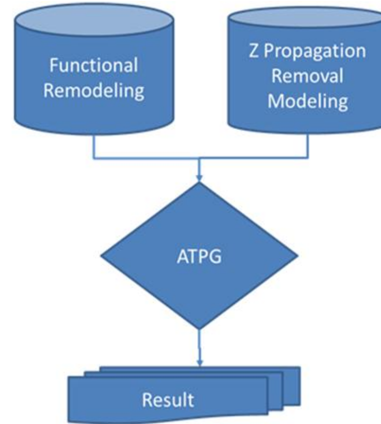

Figure 6. Standard cell transistor level ATPG coverage extraction flow

III. Basic Logic Function

For basic logic function coverage extraction, only the universal cells such as 2 inputs NAND, 2 inputs NOR and Inverter are analyzed. The transistor level coverage for universal cells is shown in Table II.

TABLE II. Universal Logic Cell Transistor ATPG Coverage

	Gate level			Transistor Level		
function	total fault	pattern	coverage	total fault	pattern	coverage
Inverter	4	2	100	12	2	100
2 input NOR	6	3	100	18	3	83.33
2 input NAND	6	3	100	20	3	86.67

From Table II, it is shown that inverter has 100% transistor level automatic test pattern generator, ATPG coverage while the transistor level automatic test pattern generator, ATPG coverage for NAND and NOR gate is 86.67 and 83.33% respectively. The detailed breakdown for universal logic gates automatic test pattern generator, ATPG fault classification is shown in Table III.

TABLE III. Universal Logic Cell Transistor Level Fault Classification

fault class	Inverter	2 Input NOR	2 Input NAND
Detected	8	11	14
Possible detected	0	0	0
Undetectable	4	4	3
ATPG untestable	0	3	3
Not detected	0	0	0
Total faults	12	18	20

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From Table III, the undetectable fault nodes are due to supply or ground connection to the MOS transistor and the transistor's gate off state. The ATPG untestable fault class is caused by series connection of same transistor type. The 2 input NAND gate's ATPG untestable nodes is shown in Fig. 7.

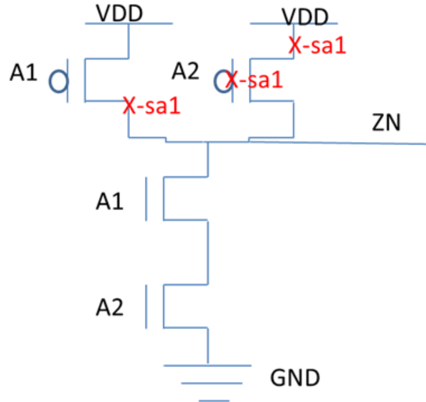

Figure 7. 2-Input NAND gate atpg untestable fault

For the 2-Input NOR gate's ATPG untestable node is shown in Fig. 8.

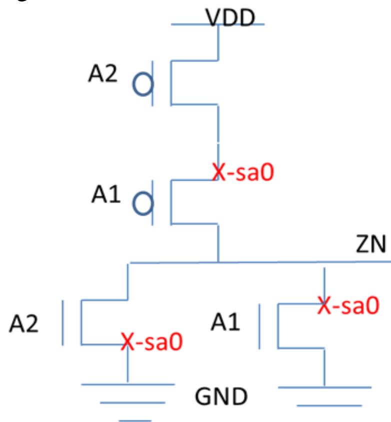

Figure 8. 2-Input NOR Gate ATPG Untestable Fault

From Fig. 7 and Fig. 8, it is concluded that the reported ATPG untestable node is due to the constant supply and ground propagation. It concludes that though at cell level, the ATPG coverage per cell node may be 100%, the actual transistor node coverage is not 100% for universal gate. Constant propagation removal will result in risk of masking off weak short. However, the isolation cannot be achieve through commercial ATPG tool. The fault removal of those nodes also highly depended on the propagation of the supply or ground, special scripting effort is required to remove the false ATPG untestable node.

IV. Input's Width of Logic

The impact of Gate's input width to transistor level DC coverage is shown in Fig. 9.

From Fig. 9, it is observed that transistor level DC coverage reduced as the input width increase, for both NAND and NOR gate. The fault classification for each NAND and NOR gate with different input's width is shown in Table IV.

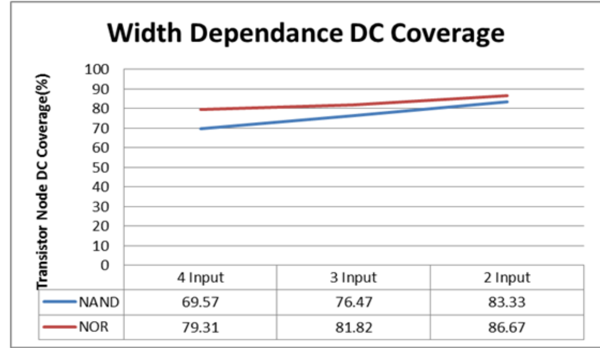

Figure 9. Width dependence transistor level DC coverage

TABLE IV. Width Dependence Transistor Level Fault Classification

fault class	2 Input NOR	3 Input NOR	4 Input NOR	2 Input NAND	3 Input NAND	4 Input NAND
Detected	11	15	19	14	20	26
Possible detected	0	0	0	0	0	0
Undetectable	4	5	6	3	4	5
ATPG untestable	3	6	10	3	6	9
Not detected	0	0	0	0	0	0
Total faults	18	26	35	20	30	40

From Table IV, it is observed that ATPG untestable node increase as the input width of NOR and NAND gate increase. The increase of ATPG untestable nodes is same as Fig. 7 and Fig. 8's explanation.

V. Logic's Drive Strength

The same analysis is repeated on inverter, 2 input NOR gate and 2 input NAND gate with various drive strength and the transistor level stuck-at-fault coverage is shown in Fig. 10.

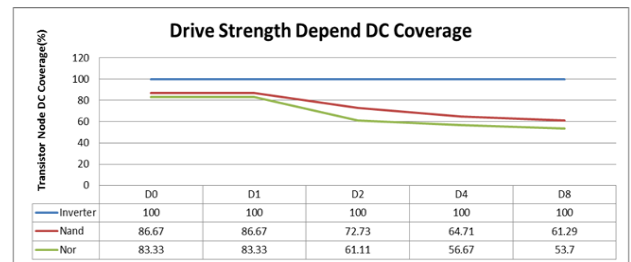

Figure 10. Drive strength dependence transistor level DC coverage

From Fig. 10, it is observed that Inverter gate stuck-at-fault coverage remain 100% regardless of the gate's drive strength. For NAND gate and NOR gate, the transistor level stuck-at-fault coverage reduced as the gate's drive strength increases. The fault classification for drive strength dependence analysis is shown in Table V, Table VI and Table VII.

TABLE V. Inverter's Drive Strength Dependence Transistor Level Fault Classification

fault class	INVD0	INVD1	INVD2	INVD4	INVD8
Detected	8	10	10	12	20
Possible detected	0	0	0	0	0
Undetectable	4	4	8	20	40
ATPG untestable	0	0	0	0	0
Not detected	0	0	0	0	0
Total faults	12	12	18	32	60

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TABLE VI. NAND GATE'S DRIVE STRENGTH DEPENDENCE TRANSISTOR LEVEL FAULT CLASSIFICATION

fault class	NAND2D0	NAND2D1	NAND2D2	NAND2D4	NAND2D8
Detected	14	14	18	22	38
Possible detected	0	0	0	0	0
Undetectable	3	3	6	16	32
ATPG untestable	3	3	8	12	24
Not detected	0	0	0	0	0
Total faults	20	20	32	50	94

TABLE VII. NOR GATE'S DRIVE STRENGTH DEPENDENCE TRANSISTOR LEVEL FAULT CLASSIFICATION

fault class	NOR2D0	NOR2D1	NOR2D2	NOR2D4	NOR2D8
Detected	11	11	11	17	29
Possible detected	0	0	0	0	0
Undetectable	4	4	8	16	32
ATPG untestable	3	3	11	13	25
Not detected	0	0	0	0	0
Total faults	18	18	30	46	86

From Table V, Table VI and Table VII, the total faults count increase as the gate's drive strength increase. The total faults count increase is expected as for the width of the MOS transistor is constrained by the physical height of the standard cell library. The standard cell gate's drive strength increment is done by multi-finger approach since the width of the MOS transistor is uniform.

VI. LOGIC'S ARCHITECTURE

For logic's architecture, the same analysis is repeated on Inverter and buffers for normal buffer, clock buffer, clock buffer with decoupling capacitance, normal inverter, clock inverter and clock inverter with decoupling capacitance. The stuck-at-fault coverage result is shown in Fig. 11.

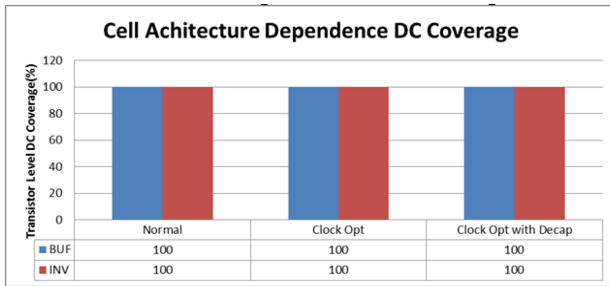

Figure 11. Cell architecture dependence DC coverage

From Fig. 11, the transistor level stuck-at-fault coverage for buffer and inverter remains 100% regardless of the cell's architecture. From Fig. 11, it is concluded that cell architecture has no impact to the buffer and inverter transistor level stuck-at-fault coverage report. The buffer and inverter's fault classification is shown in Table VIII.

TABLE VIII. CELL ARCHITECTURE DEPENDENCE TRANSISTOR LEVEL FAULT CLASSIFICATION

fault class	BUF	CBUF	DCBUF	INV	CINV	DCINV
Detected	46	46	46	36	36	36
Possible detected	0	0	0	0	0	0
Undetectable	57	57	57	80	80	80
ATPG untestable	0	0	0	0	0	0
Not detected	0	0	0	0	0	0
Total faults	103	103	103	116	116	116

From Table VIII, the total faults for each variant of buffer and inverter remain the same as the same drive strength for each variant is used for comparison.

VII. CONCLUSION

The summary of transistor level ATPG coverage for standard cell is shown in Table IX.

TABLE IX. TRANSISTOR LEVEL ATPG COVERAGE FOR STANDARD CELL SUMMARY

Scenario	Comments
Basic Logic Function	Special script is required to filter ATPG untestable node due to constant propagation
Input Width of Logic	The coverage reported from the tool degrade as the inputs' width increase
Logic's Drive Strength	The coverage reported from the tool degrade as the drive strength increase for NAND gate and NOR gate
Logic's Architecture	The ATPG tool is able to report the effective ATPG fault coverage properly

From Table IX, it concludes that:

- A special scripting is required to intelligently filter the power and ground propagation through NMOS and PMOS in order to reflect the effective equivalent gate level DC coverage while transistor level DC coverage may not be 100%
- Transistor level effective DC coverage is 100% correlated with gate level DC coverage for universal cell like Inverter, NAND gate and NOR gate if constant propagation stuck at fault untestable node is removed. The caveat of this assumption is, ignoring the possibility of weak short occurance [20].

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