Improved PSRR and Output Voltage Swing Characteristics of Folded Cascode OTA

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***Abstract*—Mixed and analog systems design with high performance suffers from many difficulties due to supply voltage, power consumption and area overhead. A need for low-voltage low-power operational amplifiers exists and used for some applications. This paper deals an effective OTA design for good PSRR, low-voltage, low-power and wide output voltage swing operational amplifier. Trying to combine an alternative technique of voltage driven-Bulk CMOS with a folded cascade OTA design to improve PSRR and output voltage swing in that circuit by reducing its supply voltage and power consumption. Two principles input voltage for OTA are used and applied at the bulk of the differential pair, showing its advantages and disadvantages, discussing further problems that have to be solved for better performance. The presented Folded Cascode OTA designs; bulk driven and gate driven structure, are implemented using a 0.35µm CMOS technology and the supply voltage 2V. These two architectures have been compared, using cadence spectrum simulations, in this paper along with drawbacks and advantages of each. The obtained results showed the good performances of the Folded Cascode Bulk Driven OTA; this is compared with classic OTA design.**

***Index Terms*—classic folded cascode OTA, folded cascode bulk driven OTA, PSRR, output voltage swing**

I. Introduction

The difference between an Operational Amplifier (Op-Amp) and an Operational Transconductance Amplifier (OTA) is that the op-amp has got an output buffer so that it is able to drive resistive loads. An OTA can only drive capacitive loads.

Operational Transconductance amplifiers are an essential blocks in many mixed-analog systems and sensor interface. Different architectures have been used [1]-[4] to obtain very high gain and impedance at output, high gain bandwidth product and acceptable power supply rejection ratio (PSRR).

To have high output impedance and thereby high gains, cascoding is done, where tow MOSFETs are placed one above the other [5]-[7]. Cascode OTA circuits are widely used in circuit designs at places where high gain and high output impedances are required [8]-[10]. The regular cascode structures are avoided as their use increases the gain of the structure. Folded cascade technique gives better performance even than the cascode technique. The Folded Cascode OTA is usually used in high frequency applications because of its many advantages. Firstly, it provides a high output impedance to give very high output gain and so it is useful in low-voltage design [11]. Secondly, it is easier to frequency compensate; the load capacitor is also the compensation capacitor [12]. Also, unlike the two stage op-amp it does not suffer from frequency degradation of the power supply rejection ratio. Finally, folded cascode OTA is used for high speed applications thanks to its capability to provide high gain and large bandwidth [13].

The remainder of this paper is organized as follows. Basic theory of OTA amplifier and the advantages of Folded Cascode OTA to other structures are presents in Section 2. Section 3 focuses on the design of Folded Cascode Gate Driven OTA and Folded Cascode Bulk Driven OTA; the simulations results obtained under cadence spectrum are devoted. The comparative study and the discussion are provided in Section 4. Finally, Section 5 draws conclusions.

II. Basic Theory

The novel generation of microelectronics circuits allows the integration on some chip with less area overhead complexity electronic systems. These systems are widely used in many applications such as multimedia, medical telecommunications, etc. In these systems, analog parts ensure the functions of amplification and/or filtering.

The operational amplifiers are commonly used for most analog and mixed circuits design. Furthermore, they are usually adapted to sensor interface. Table I illustrated the importance operational amplifiers characteristics.

Operational Amplifier exists in different topology; Table II showing the advantages and disadvantages of divers architectures. The performance of simple OTA architecture; have an acceptable gain, is limited by its input and output voltage swing [14]. To improve the performances of simple OTA and to overcome these limits a Folded Cascode OTA is used. The Telescopic OTA is better operational amplifier architecture for low power consumption and low noise characteristics, but it has a limited input and output voltage swing. In order to alleviate some of the drawbacks of telescopic operational amplifier, a folded cascode OTA based on Wilson mirror

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can be used. In particular, folded casocde OTA structure allows widening output voltage swing compared to unfolded structures; telescopic and classic OTA [15].

TABLE I. AMPLIFIER PERFORMANCE CHARACTERISTICS

Amplifier Performance	
Characteristics	**Description**
A_{md}	Differential Gain
A_{mc}	Common Gain
Z_{in} and Z_{out}	Input and Output Impedance
F_c	Switching Frequency
GBW	Gain Bandwidth Product
Φ_M	Phase Margin
CMR	Common Mode Input Range
V_{out}	Output Voltage Swing
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ratio
Offset	Voltage and Current Offset
P_{cc} and I_{cc}	Power and Current Consumption
SR	Slew Rate
S_{noise}	Noise

TABLE II. COMPARATIVE OTA CHARACTERISTICS

Characteristics/ Type	Simple OTA	Miller OTA	Telescopic OTA	Folded Cascode OTA
Gain	±	+	++	+++
Output Resistance	-	±	+	++
Output Voltage Swing	-	+	-	±
CMR	-	-	±	+
Consumption	-	-	±	±

Legend Levels: - Poor, ± Fair, + Good, ++ Very Good, +++ Excellent

Folded Cascode OTA is better operational amplifier architecture. Firstly, OTA designer occupies small overhead and folded structure allows a low supply voltage to systems where is embedded [3], [4] and low current consumption. Secondly, the PMOS differential pair that converts the input voltage to current deals less noise compared with a NMOS differential pair [16]. In addition, the folded cascode transistors structure deals to OTA amplifier good gain and higher output impedance [17], [18]; this is depend on dynamic parameters g_m and g_{ds} which are improved by the cascade transistors structure. Finally, the folded casocde structure improved the excursion of common mode input range (CMR); it is compared with other structures such as telescopic OTA [19]. The output voltage swing of Folded Cascode OTA structure is improves but it's one of the major drawbacks [10], [15].

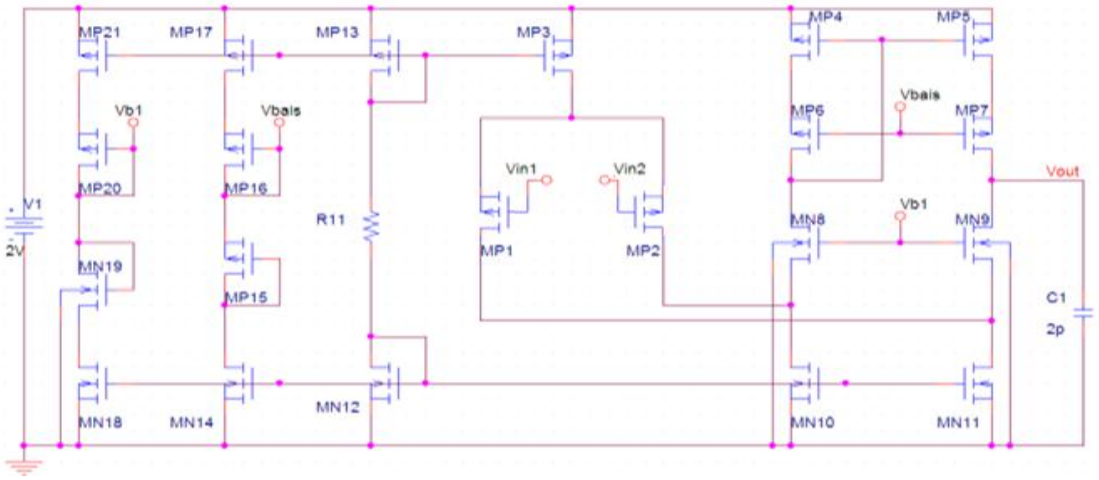

Figure 1. Folded cascode gate driven OTA

III. FOLDED CASCODE OTA

Folded Cascode OTA exists in different topology; Folded Cascode Gate Driven OTA [1], [3], [4] and Folded Cascode Bulk Driven OTA [17], [18], [20]. To improve the characteristics of classic Folded Casocde OTA a Folded Cascode Bulk Driven OTA is used; its input voltages are applied on the bulk of the transistors consisting the differential pair.

A. Folded Cascode Gate Driven OTA

The conventional structure of Folded Cascode OTA using Gate Driven technique is shown in Fig. 1. The basic operation of presented circuit is illustrated below.

1) Bias block

Usually, the bias block is used to generate a bias voltage and current. In major design, the bias current and voltage are provided by simple mirror current in order to polarize in saturation region all transistors consisting the circuit.

The stage consisting by M12, M13 and R1 provides the bias current I_{bias}, V_{gs12} and V_{gs13}.

The stage consist on M14, M15, M16 and M17 is used to generate the bias voltage V_{bias} ; then its applied respectively to the gates of MP4 and MP5 transistors.

The stage consist on M18, M19, M20 and M2 is serves to provide the bias voltage V_{b1} ; then its applied to polarize the cascode transistors MN8 and MN9.

2) Input stage: folded cascode differential pair

The input stages consist on PMOS gate driven differential pair; MP1 and MP2. The cascode transistors; MN8 and MN9, are polarized by V_{b1} at its gates. The folded transistors are MN10 and MN11; represent respectively current sources for MP2 and MN8, MP1 and MN9. These current sources are biased at the same value as the tail current source of MP3.

3) Cascode mirror current

The Folded Cascode differential pair is load by a cascode current mirror. It is formed by two principal transistors are respectively M4 and M5 also two cascode transistors; MP6 and MN7, where are polarized by a fixed voltage (V_{bias}) applied at its gates.

For the presented circuit shown in Fig. 1, the listed equation (1) to (10) covered its importance characteristics.

The differential gain expression becomes:

$$A_{md}=-\frac{g_{m1}}{\frac{(g_{ds1}+g_{ds11})g_{ds9}}{g_{ds1}+g_{ds11}+g_{m9}+g_{ds9}+g_{m9}}+\frac{g_{ds7}g_{ds5}}{g_{ds5}+g_{ds7}+g_{m7}}} \quad (1)$$

Output Impedance is computed:

$$Z_{out}=\frac{1}{\frac{(g_{ds1}+g_{ds11})g_{ds9}}{g_{ds1}+g_{ds11}+g_{m9}+g_{ds9}+g_{m9}}+\frac{g_{ds7}g_{ds5}}{g_{ds5}+g_{ds7}+g_{m7}}} \quad (2)$$

The Switching Frequency of OTA is:

$$F_c=\frac{1}{2\pi Z_{out}C_l} \quad (3)$$

The Gain Bandwidth Product is given by:

$$\text{GBW}=A_{md}W_c=\frac{g_m}{C_l} \quad (4)$$

The Common Mode Input Range can be written as:

- Differential Input 1

Positive CMR:

$$V_{in1}(\max)=V_{dd}+V_{dssat3}+V_{gs1} \quad (5)$$

Negative CMR:

$$V_{in1}(\min)=V_{ss}+V_{dssat11}+V_{gd1} \quad (6)$$

- Differential Input 2

Positive CMR:

$$V_{in2}(\max)=V_{dd}+V_{dssat3}+V_{gs2} \quad (7)$$

Negative CMR:

$$V_{in2}(\min)=V_{ss}+V_{dssat10}+V_{gd2} \quad (8)$$

The Output Voltage Swing can be expressed by:

$$V_{ss}+V_{dssat11}+V_{dssat9}<V_{out}<V_{dd}+V_{dssat7}+V_{dssat5} \quad (9)$$

The Slew Rate can be calculated as:

$$\text{SR}=\pm\frac{dVs(t)}{dt}=\pm\frac{I_{ds3}}{C_l} \quad (10)$$

The presented Folded Cascode Gate Driven OTA, shown in Fig. 1, is designed with 0.35µm BSIM3V3 level CMOS technology and voltage supply 2V. Table III gives the dimension; width and lengths, of different transistors, resistor and load capacitor of the presented circuit.

TABLE III. DESIGN PARAMETERS OF CIRCUIT

Devices	Size	Units
MP1/MP2	50/8	µm/µm
MP3	8/5	µm/µm
MP4/MP5	12/10	µm/µm
MP6/MP7	5/6	µm/µm
MN8/MN9	4/2	µm/µm
MN10/MN11	4/8	µm/µm
MN12	1/16	µm/µm
MP13	3/16	µm/µm
MN14	20/6	µm/µm
MP15	15/2	µm/µm
MP16	30/5	µm/µm
MP17	1/2	µm/µm
MN18	10/30	µm/µm
MN19	10/35	µm/µm
MP20	50/2	µm/µm
MP21	15/9	µm/µm
R_{11}	100	Ω
C_L	2	pF
V_{dd}	2	V

The measurement results of the Folded Cascode Gate Driven OTA are stated below in Table IV. The obtained results are extracted using Cadence spectrum. The folded cascode gate driven OTA has a DC gain of 74.6dB with unity gain bandwidth of 0.655MHz with a supply voltage of 2V. Also, it has a PSRR of 45.26dbB with wide output voltage swing is of the order of 0.501V to 1.32V.

TABLE IV. CHARACTERISTICS OF FOLDED CASCODE GATE DRIVEN OTA

Parameters	Results	Units
A_{d0}	74.6	dB
A_{mc}	-67.64	dB
Z_{out}	697.2	MΩ
F_C	0.122	kHz
GBW	0.655	MHz
CMRR	113.65	dB
Offset	0.001	V
CMR	0.613 to 1.276	V
V_{out}	0.501 to 1.32	V
I_{CC}	12.487	µA
P_{CC}	24.974	µw
PSRR	45.26	dB
SR+/SR-	1.93/-1.35	V/µS

B. Folded Cascode Bulk Driven OTA

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. A Bulk Driven MOSFET is used to overcome the threshold voltage; a reverse bias on the

well-source junction will cause the threshold voltage to increase. Similarly, a forward bias on this junction will cause the threshold voltage to decrease. To overcome the threshold voltage limitation a Bulk Driven transistor has been used as a good solution. Because the Bulk Driven transistor is a depletion type device, it can work under negative, zero, or positive biasing condition.

By using bulk driven technique, proposed Folded Cascode Bulk Driven OTA is designed and simulated. Then, the simulation results are presented below with showing its advantages and disadvantages, discussing further problems that have to be solved for better performance. The Folded Cascode OTA using bulk driven technique structure is shown in Fig. 2 [20]. The basic operation of Folded Cascode Bulk Driven OTA is presented below:

The bias block is used to generate a bias voltage and current to different stage consist the presented circuit, shown in Fig. 2.

The input stage of presented OTA circuit is consisting on PMOS bulk driven differential pair; MP1 and MP2. The differential pair is polarized at its gate with a fixed voltage V_{bias}, rather these inputs voltage is applied at the bulk of PMOS transistors consisting the differential pair stage.

The cascode transistors; MN8 and MN9, are polarized by V_{b1} at its gates.

The Folded Cascode consist the input stage of OTA circuit increase the common mode input voltage range, since we replace a current source MN10 and MN11 instead of a current mirror which it's used typically in the conventional OTA.

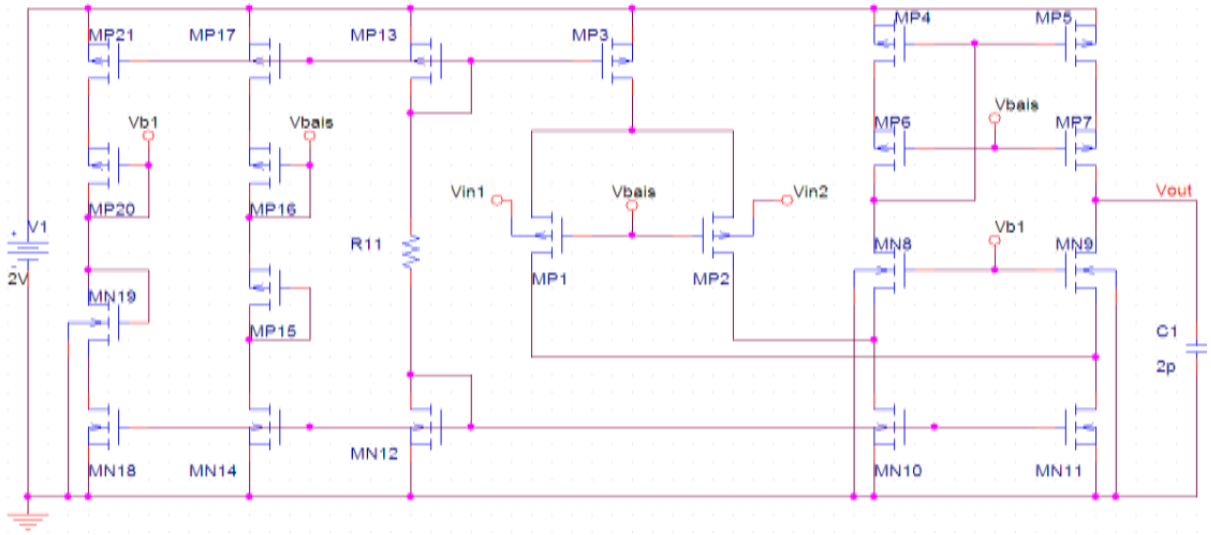

Figure 2. Folded cascode bulk driven OTA

The Folded Cascode consist the input stage of OTA circuit increase the common mode input voltage range, since we replace a current source MN10 and MN11 instead of a current mirror which it's used typically in the conventional OTA.

The Folded Cascode differential pair is load by a cascode mirror current. It is formed by two principal transistors are respectively M4 and M5, also it is consist with two cascode transistors, MP6 and MN7, where are polarized by a fixed voltage (V_{bias}) applied at its gates.

For the presented circuit shown in Fig. 2, the listed equation (11) to (22) covered its importance characteristics.

The Differential Gain can be written as:

$$A_{md}=-\frac{g_{mb1}}{\frac{(g_{ds1}+g_{ds11})g_{ds9}}{g_{ds1}+g_{ds11}+g_{m9}+g_{ds9}+g_{mb9}}+\frac{g_{ds7}g_{ds5}}{g_{ds5}+g_{ds7}+g_{m7}}} \quad (11)$$

The output impedance Z_{out} expression becomes:

$$Z_{out}=\frac{1}{\frac{(g_{ds1}+g_{ds11})g_{ds9}}{g_{ds1}+g_{ds11}+g_{m9}+g_{ds9}+g_{mb9}}+\frac{g_{ds7}g_{ds5}}{g_{ds5}+g_{ds7}+g_{m7}}} \quad (12)$$

The Switching Frequency can be calculated as:

$$F_c=\frac{1}{2\pi Z_{out}C_l} \quad (13)$$

The Gain Bandwidth Product is given by:

$$GBW=A_{md}W_c=\frac{g_{mb}}{C_l} \quad (14)$$

The Common Mode Input Range can be written as:

- Differential Input 1

Positive CMR:

$$V_{in1}(max)=V_{dd}+V_{dssat3}+V_{bs1} \quad (15)$$

Negative CMR:

$$V_{in1}(min)=V_{ss}+V_{dssat11}+V_{bs1}-V_{dssat1} \quad (16)$$

- Differential Input 2

Positive CMR:

$$V_{in2}(max)=V_{dd}+V_{dssat3}+V_{bs2} \quad (17)$$

Negative CMR:

$$V_{in2}(min)=V_{ss}+V_{dssat10}+V_{bs2}-V_{dssat2} \quad (18)$$

The Output Voltage Swing can be expressed by:

$$V_{ss}+V_{dssat11}+V_{dssat9}<V_{out}<V_{dd}+V_{dssat7}+V_{dssat5} \quad (19)$$

The Slew Rate can be calculated as:

$$SR= \pm\frac{dVs(t)}{dt} = \pm\frac{I_{ds3}}{C_l} \quad (20)$$

The Common Mode Rejection Ratio is expressed by:

$$CMRR = 20\log(\frac{A_{md}}{A_{mc}}) \quad (21)$$

The Power Supply Rejection Ratio is given by:

$$PSRR = 20\log(\frac{V_{dd}}{V_{out}}) \quad (22)$$

By using 0.35µm BSIM3V3 level CMOS technology with a supply voltage of 2V, the Folded Cascode Bulk Driven OTA is designed. The simulation results are extracted using Cadence spectrum; Table V lists the experimental results obtained in moderate saturation region. The folded cascode bulk driven OTA has a DC gain of 76dB with unity gain bandwidth of 0.736MHz with a supply voltage of 2V. Also has a PSRR of 70.12dbB with wide output voltage swing is of the order of 0.191V to 1.96V.

TABLE V. CHARACTERISTICS OF FOLDED CASCODE BULK DRIVEN OTA

Parameters	Results	Units
A_{d0}	74.6	dB
A_{mc}	-67.64	dB
Z_{out}	697.2	MΩ
F_C	0.122	kHz
GBW	0.655	MHz
CMRR	113.65	dB
Offset	0.001	V
CMR	0.613 to 1.276	V
V_{out}	0.501 to 1.32	V
I_{CC}	12.487	µA
P_{CC}	24.974	µw
PSRR	45.26	dB
SR+/SR-	1.93/-1.35	V/µS

TABLE VI. COMPARISON RESULTS BETWEEN BULK DRIVEN AND GATE DRIVEN OF FOLDED CASCODE OTA STRUCTURE

Parameters	Gate Driven	Bulk Driven
A_{d0} (dB)	74.6	76
A_{mc} (dB)	-67.64	-60.34
Z_{out} (MΩ)	697.2	697.2
F_C (kHz)	0.122	0.122
GBW (MHz)	0.655	0.736
CMRR (dB)	113.65	142.24
Offset (V)	0.001	0.0003
CMR (V)	0.613 to 1.276	0.420 to 1.593
V_{out} (V)	0.501 to 1.32	0.191 to 1.96
I_{CC} (µA)	12.487	12.487
P_{CC} (µw)	24.974	24.974
PSRR (dB)	45.26	70.12
SR+/SR- (V/µS)	1.93/-1.35	1.23/-1.05

IV. COMPARATIVE STUDY

The following Table VI describes the performance comparison in 0.35µm technology taken in specifications for the design and that resulted after simulations with class folded casocde OTA and folded cascode bulk driven OTA.

The Folded Cascode OTA architecture used bulk driven technique; that the input voltage is applied at the bulk of the transistors consisting the differential pair MP1 and MP2, usually called Folded Cascade Bulk Driven OTA. This type of OTA design dedicates many advantages to Operational amplifiers. Firstly, it is used to increase respectively the input common mode voltage range and the output resistance. Since, it has fair low voltage and low power. Secondly, the output resistance is one of the most important performance parameters; the value of this resistance is almost equal for both gate-driven and bulk driven. Then, a bulk driven folded cascode current MP3 biased by MN12 and MP13 has been used for the OTA design since this type of connection is suitable for lower voltage applications. Finally, the Bulk Driven technique is used for the designer of Folded Cascade OTA to improve the PSSR characteristic (Power supply rejection ratio); because it is compensated by its load capacitance. Trying, to combine bulk driven technique with folded cascade OTA design deals a wide output voltage swing OTA by reducing its 1/f noise and offset. Similarly, according to studies and simulations, on the functional behavior of the three types of current mirrors, the cascade mirror current deals a large dynamic which allows obtaining a better output dynamic compared to other types; Wilson and improves Wilson mirrors current.

V. CONCLUSION

Folded Cascode Bulk Driven OTA is a high potable and robust system, very insensitive in integrated continuous time filters, low voltage and high frequency applications, and interface sensors. In this project, we successfully designed a classic folded casocde OTA. The transistor channel widths and lengths are optimized to get high gain bandwidth and high gain with low power consumption; a high gain of 74.6dB and gain bandwidth of 0.655MHz with a load capacitor of 2pF. Also, we successfully designed a Folded Casocde Bulk Driven OTA. The gain of OTA is increased to 76dB with unity gain bandwidth of 0.736 MHz and power consumption of 24.974µW in saturation region, with a compensation load capacitor of 2Pf. With a single 2V power supply, the input common mode range is about 0.420V to 1.593V and the output voltage swing is of the order of 0.191V to 1.96V. The OTA biased in a Folded Cascode structure with bulk driven configuration improves the PSRR characteristic, a PSRR of about 70.12dB. Also in this application, the output voltage swing can be improved by bulk driven technique.

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