FPGA Controlled Simplified H-Bridge Multilevel Inverter

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Abstract—the multilevel inverter is recently applied in many industrial applications such as ac power supplies, static var compensators, drive system, etc. One of the significant advantages of multilevel configurations is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel inverter starts from three levels. As the number of level reach infinity, the output THD approaches zero. This work reports a multilevel inverter using an H-Bridge output stage with a bidirectional auxiliary switch. This Simplified H-bridge multilevel inverter produces a significant reduction of power devices and capacitor required to implement a multilevel output.

Index Terms—bidirectional auxiliary switches, field programmable gate array, h-bridge, multilevel inverter

I. INTRODUCTION

The different topologies presented in the literature as a multilevel inverter show a number of characteristics in common. The main disadvantage associated with the multilevel inverter configurations is their circuit complexity [1] requiring a high number of power switches. When we are entering the simplified H-Bridge multilevel inverter, power devices will be reduction and circuit complexity also reduction so circuit losses also reducing.

Even taking into account the technological tendency to lower the prize at which multilevel inverter can compete with standard configurations. As contribution to solve this twin Problem (cumbersome power stage and complex firing control circuit) this work proposes a new converter topology, presented [2] as a block diagram in Fig. 1(a). This topology includes an H-Bridge stage with an auxiliary

bidirectional switch, drastically reducing the power circuit complexity, and a modulator and firing control circuit developed using a field programmable gate array (FPGA). These two Concepts used in the design of the seven level bridge converters [3] presented below. The new converter topology used in the power stage offers an important improvement in term of lower component count and reduced layout complexity, when compared with the five level converters presented in the literature [4], [5]. The simplified H-bridge multilevel inverter achieves a reduction in the number of main switch required and uses no more diodes and capacitors that the second best topology, the asymmetric cascade configurations [6]. In the modulator circuit, the FPGA can perform all required modulation functions providing another important reduction in cost and circuit complexity [7].
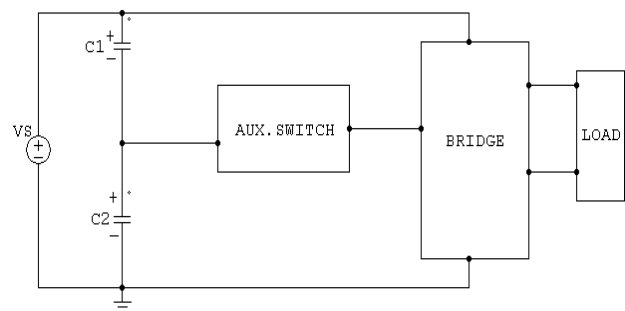

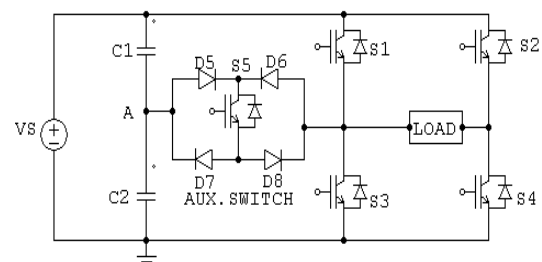Figure 1(a). Block diagram of simplified h-bridge multilevel inverter

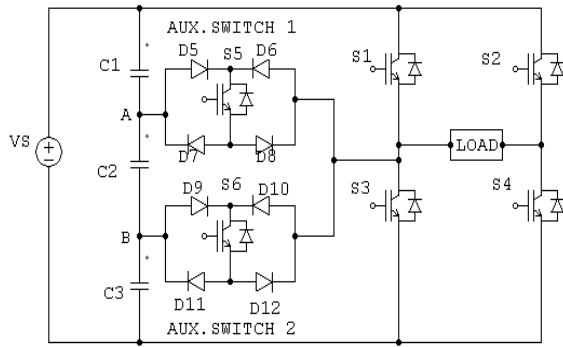Figure 1(b). Simplified h-bridge five level inverter power stages

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Figure 1(c). Simplified h-bridge seven level inverter power stage

TABLE I. COMPARISON BETWEEN FOUR DIFFERENT MULTILEVEL LEVEL INVERTERS

Multilevel inverter type	H-Bridge auxiliary switch	Diode clamped	Flying capacitor	Cascaded type
Main controlled switches	4	12	12	12
Auxiliary controlled switches	2	0	0	0
Diodes	12	28	12	12
Capacitor	3	8	10	2

II. POWER STAGE

A. Circuit Configuration

Fig. 1(a) shows that block diagram of simplified H-bridge multilevel inverter and Fig. 1(b) shows that five level simplified H-bridge multilevel inverter. Fig. 1(c) shows that a simplified seven level H- bridge inverter. The H-bridge is formed by four main power devices, S_1 to S_4. For seven level output voltage [8] two auxiliary switches, four main switches and three capacitors requires.

B. Stage Advantages

To prove the reduction in component numbers achieved by this simplified H-bridge multilevel inverter configuration, Table I present the number of component required to implement [9] a seven level inverter using simplified H- bridge multilevel inverter and three previously defined ones: the two that considered as the standard multi level stages [10], the diode clamped and the capacitor clamped configuration, and a new and highly improved multi level stage, the symmetric cascade configuration [11]

1) Main power switches

The new topology achieves a around 40% reduction in the number of main switches required, using only six controlled power switches instead of twelve required in any of the other three configurations [12]. The auxiliary switch voltage and current rating are lower than the once required by the main controlled switches.

2) Auxiliary devices (diodes and capacitors)

The new configurations reduce the number of diodes and capacitors, when compared with diode clamped configurations. The new configurations reduce the number

of capacitors [13], when compared with the capacitor clamped configurations. The new configurations use no more diodes or capacitors that the second best topology in the table, the asymmetric cascade configurations.

Additionally, since three capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation [14], [15] avoiding a problem that can limit operating range in some other multi level configurations.

C. Power Stage Operation

The required seven voltage output level (Vs, 2Vs/3, Vs/3, 0, -Vs/3, -2Vs/3, -Vs) are generated as follows:

1) Maximum positive output level (Vs): S1 is ON, connecting the load positive terminal to Vs and S4 is on, connecting the load negative terminal to ground. All other control switches are OFF. The voltage applied to load terminal is Vs as in Table II

2) Positive output level (2Vs/3): The auxiliary switch S_5 is ON Connecting to the load positive terminal, through diodes D_5 and D_8, and S_4 is ON, connecting the load negative terminal to ground. All other control switches are OFF, the voltage applied to load terminal is 2Vs/3.

3) Positive output level (Vs/3): The auxiliary switch S_6 is ON, connecting the load positive terminal, through diodes D_9 and D_{12} and S_4 is ON, connecting the load negative terminal to ground. All other control switches are OFF; the voltage applied to the load terminal is Vs/3.

4) Zero output level: The two main switches S_3 and S_4 are ON, short circuiting the load. All other control switches are OFF; the voltage applied to the load terminal is zero.

5) Negative output level (-Vs/3): The auxiliary switch S_6 is ON, connecting the load positive terminal, through diodes D6 and D7 and S_2 is ON, connecting the load negative terminal to ground. All other control switches are OFF, the voltage applied to load terminal is -Vs/3.

6) Negative output level (-2Vs/3): The auxiliary switch S_5 is ON, connecting the load positive terminal, through diodes D_{10}, D_{11} and S_2 is ON, connecting the load negative terminal to ground. All other control switches are OFF, the voltage applied to load terminal is -2Vs/3.

7) Maximum negative output level (-Vs): S2 is ON, connecting the load negative terminal and S3 is ON, connecting the load positive terminal to ground. All other control switches are OFF, load voltage applied to the load terminal is -Vs.

TABLE II. SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

S_1	S_2	S_3	S_4	S_5	S_6	V_{RL}
On	off	off	On	off	off	V_S
Off	off	off	On	on	off	$2V_S/3$
Off	off	off	On	off	on	$V_S/3$
Off	off	on	On	off	off	0
Off	on	off	Off	off	on	$-V_S/3$
Off	on	off	Off	on	off	$-2V_S/3$
Off	on	on	Off	off	off	$-V_S$

III. SIMULATED RESULTS

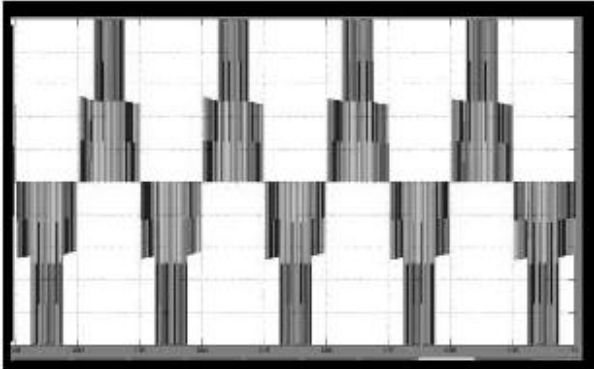The simplified H-bridge seven level inverter was simulated in MATLAB.

Figure 2(a). Simulated simplified h-bridge five level inverter output voltage (V_{DC}: 100V, sample frequency is 1000Hz, the fundamental frequency is 50Hz)
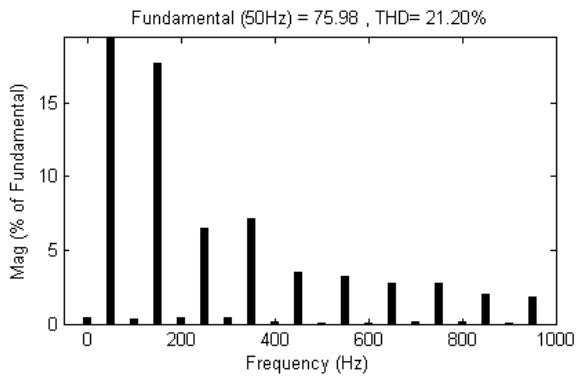

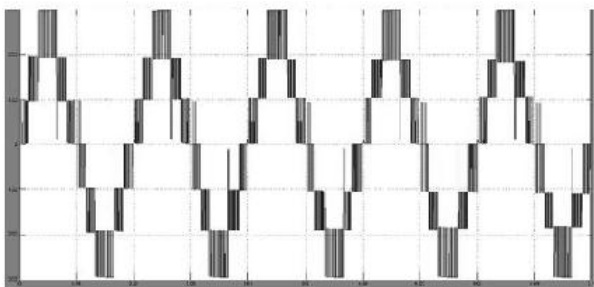Figure 2(b). THD result for simplified h-bridge five level inverter

Figure 2(c). Simulated simplified h-bridge seven level Inverter output voltage (V_{DC}: 300V, sample frequency is 1000Hz, the fundamental frequency is 50Hz)
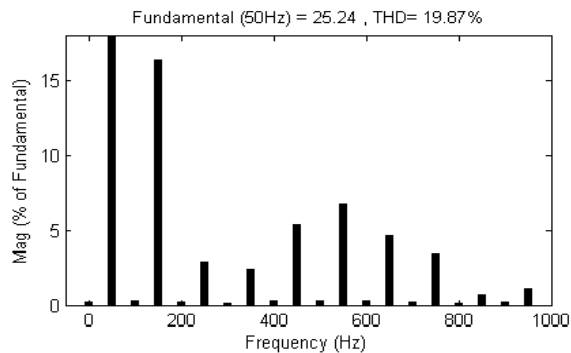

Figure 2(d). THD result for simplified h-bridge seven level inverter

Fig. 2(a) shows that simulated output waveform for five level simplified H-bridge inverter. The sample frequency was 1000Hz amd modulation index was 0.8. It is clearly visible that the simulated output is very close to ideal output defined for five level inverter. Fundamental frequency si 50 Hz. It can be seen that the pulse duration is variable depending on the modulator previous state. The five voltage levels in the Figureure are Vs=200V, Vs/2=100V, 0V, -Vs/2=-100V, -Vs=-200V. Fig. 2(b) shows that total harmonic distortion, the percentage of THD analysis in conventional five level inverter is 21.20%.

Fig. 2(c) shows that simulated seven level output voltage. The sample frequency is 1000Hz and modulation index is 0.8. It is clearly visible that the simulated ouput is very close to ideal output defined for seven level inverter. Fundamental frequency si 50Hz. It can be seen that the pulse duration is variable depending on the modulator previous state. The seven voltage levels in the Figureure are Vs=300V, 2Vs/3=200V, Vs/3=100V, 0V, -Vs/3=-100V, -2Vs/3=-200V, Vs=-300V. Fig. 2(d) shows that total harmonic distortion, the percentage of THD analysis in Proposed seven level inverter is 19.87%.

IV. HARDWARE CIRCUIT DESIGN

Experimental validation of the simplified H-bridge seven level inverter is going to achieve by using the configurations. Fig. 3(a) shows the simplified h-bridge Seven level inverter with RL load. Total harmonic distortion analysis is proposed seven level inverter with RL load is shown in Fig. 3(b)

Three main blocks are going to present: the modulator block, the driver circuit and the seven level inverter power stages shows in Fig. 3(c).
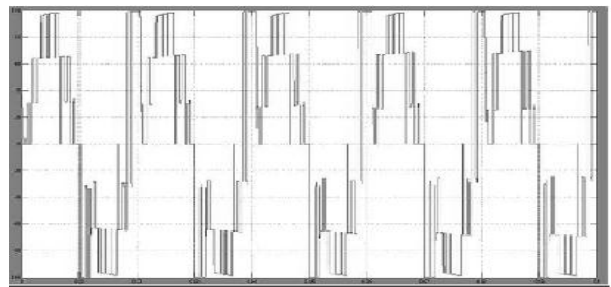

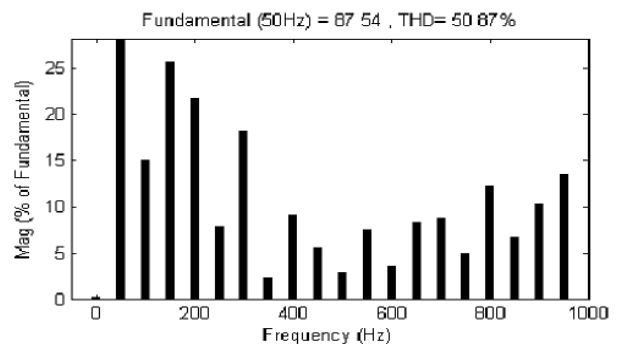Figure 3(a). Simulated simplified h-bridge seven level inverter with RL load

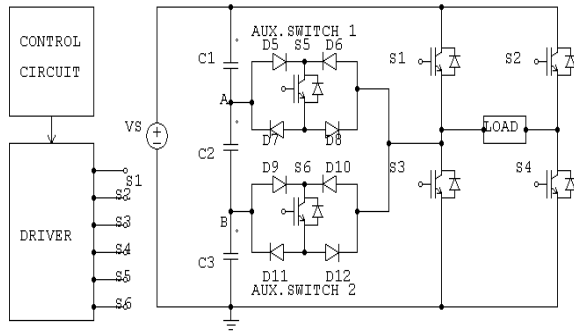Figure 3(b). THD result for simplified h-bridge seven level with RL load

Figure 3(c). Simplified h-bridge seven level hardware circuit diagram

A. Control Circuit

In the seven level inverter controls circuit generates the control signal for all the power components in the power stage. In this implementation, going to use a FPGA programmable circuit (sparton 3). All programs are going to done verilog hardware description language.

B. Interface Circuit

The interface circuit going to provide the required isolation and power gain between the modulator seven output and power devices gate.

C. Power Stage

The power stage going to assemble by using IGBT H-bridge with auxiliary switch module. The auxiliary is containing diodes and IGBT.

V. CONCLUSION

A cost effective simplified H-bridge seven level inverter has been developed and simulated using MATLAB. A performance comparison of the proposed simplified seven level inverter with a conventional simplified H-bridge five level inverter is also made in terms of total Harmonic distortion (THD) response. The multi level inverter is number of level will be increasing THD approaches to zero.
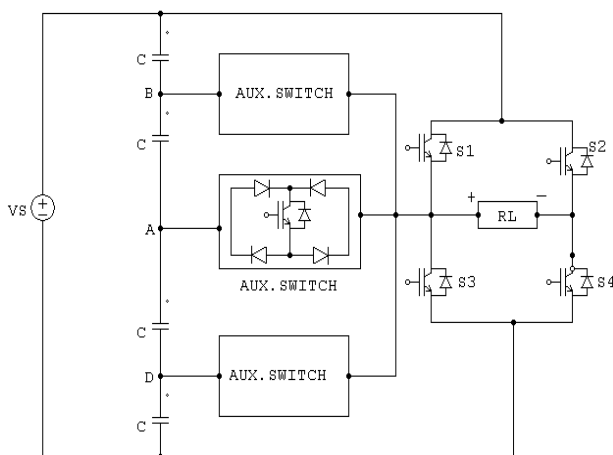

Figure 4. Generalized multilevel inverter configurations using the simplified h-bridge

A further development of the simplified H-bridge multilevel inverter able to be applied to any number of

voltage levels with in the power switches maximum voltage, is now under consideration. As shown in Fig. 4. The inverter power stage under study will consist of an H-bridge n-level capacitor voltage divider.

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