Equalization Chargers Using Parallel- or Series-Parallel-Resonant Inverter for Series-Connected Supercapacitors

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***Abstract*—A equalization charger using parallel-or series-parallel-resonant inverter for series-connected supercapacitors is proposed in this paper, according to low voltage characteristic of supercapacitor. This topology reduces a large number switches and only has resonant structure including some diodes and a single transformer. In addition, because of the characteristic of parallel resonant inverter, the equalization charging current can be limited in the numerical value. So the topology can work steadily without feedback control. The control circuit is greatly simplified. The simulation results from a 200W universal input prototype are given to verify the effectiveness of the analysis and the merits and demerits of this topology also are introduced.**

***Index Terms*—supercapacitor (SCs), resonant inverter, equalization charger**

I. INTRODUCTION

With the rapid development of the rail transportation today, how to reduce the subway's energy loss and operating costs is especially important. The research on metro regenerative braking energy recycling is of great significance to the development of rail transportation, the energy conservation as well as the protection of environment. In metro regenerative braking energy recycling systems, supercapacitors (SCs) are widely used to store the regenerative braking energy. However, the voltage equalization of SCs in series is a key technical problem which limits the application of SC storage systems. The equalizers of SCs become research hotspots. A SC voltage equalization charger device used in DC metro traction power grid is studied, and a novel voltage equalization charger circuit is proposed which is promised to achieve a high equalization precision. The equalization device also has other auxiliary functions to guarantee the security and reliability of SCs.

Alongside, a variety of equalization techniques have been proposed to mitigate the voltage unbalance of series-connected Lic and Scs [1]-[4]. But the conventional topology exist too much transformers and switches. So the equalization charger needs a large scale and high weight [5]. The least but not the least, it is rather expensive comparing to this novel topology.

II. OPERATION ANAYSIS OF EQALIZATION CHARGER

Fig. 1 is the main circuit of equalization charger. First, the circuit has two parts. Fig. 2 is resonant inverter and voltage multiplier.

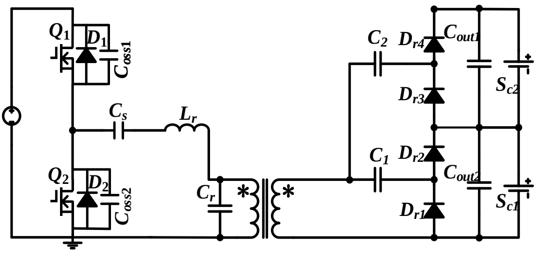
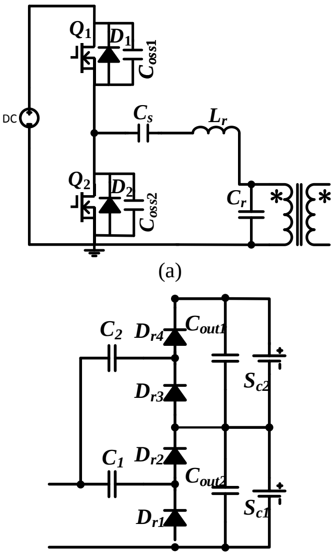


Figure 1. Main circuit of equalization charger



(a)

(b)

Figure 2. (a) Resonant inverter (b) voltage multiplier

In resonant inverter circuit, a DC source gives the energy to resonance unit. The resonance unit consists of two capacitors C_s C_r and single inductance L_r. Cs plays an effect as not only resonance unit but also a blocking capacitor. So the C_s need to design much larger than C_p. This issue will also be discussed in the following article. Two switches work at a very high frequency because when the characteristic impendence of resonant inverter is rather smaller, L_r C_p can be designed at very low value.

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Also the equalization current can be designed at high value.

In voltage multiplier circuit, the equalization current from primary side of transformer deliver to transformer secondary side. On account of current flow direction, we can be divided into two types. Firstly, the current inflows into diodes which have the odd-numbered subscript. Secondly, the current inflows into diodes which have even-numbered subscript. These two situations are the same considering the effect on mitigate the Scs. C_1 and C_2 have an effect on clamping voltage. C_{out} is filter capacitor and it is leaved out when analysis the multiplier.

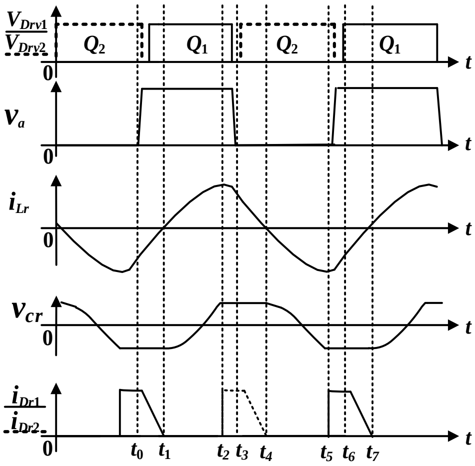
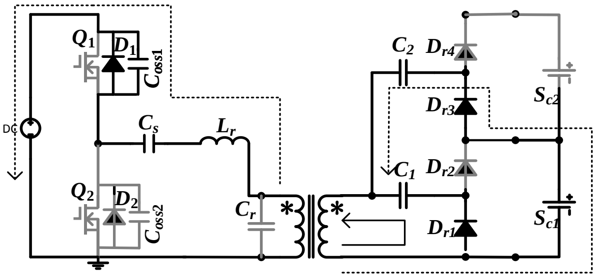
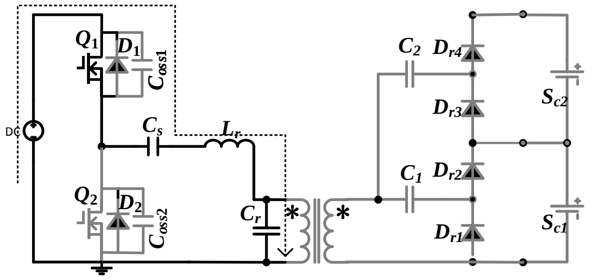


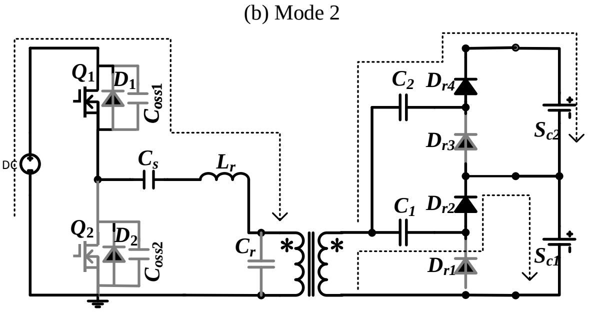
Figure 3. Key operation waveforms under voltage-balanced condition



(a) Mode 1



(b) Mode 2



(c) Mode 3

Figure 4. Current flow direction

Waveforms in Fig. 3 are illustrated assuming the components are ideal and C_{out} is large enough. Fig. 4 illustrates current condition in every state.

Time t_0-t_1: Current condition are expressed in Fig. 4(a). The current inflow into fly-wheel diode while V_{cp} is clamped to $-nV_i/2$ and i_{Dr1} i_{Dr3} have the current that from the primary transformer. L_r and C_s happen resonance. Because before i_{Lr} reaches to zero, the driving signal of Q_1 is emerged. So the Q_1 can turn on at zero Voltage (ZVS).

Time t_1-t_2: When i_{Lr} reaches to zero, transformer quit to the circuit. So L_r C_s C_r resonant. All the diodes in secondary transformer have no currents. The multiplier does not work. These situations similar with parallel-series resonant. In order to achieve the high equalization charger current, we need to make $i_{Lr\text{-}max}$ larger. So in this state, L_r C_s C_r need to design quite small.

Time t_2-t_3: When V_{cr} increases to $nV_i/2$, V_{cr} is clamped at this value. C_r quit resonance. Voltage multiplier works. The diodes with even-numbered have the current. So the equalization charger current is sum of every diode current. In other words, the whole equalization charger current can be divided into several Scs.

Time t_3-t_4: When the driving signal of Q_1 is off, anti-parallel diode D_2 can freewheel. So Q_2 is ready for ZVS. The waveforms are similar with the first state. Current situation in t_3-t_6 is symmetrical to situation in t_0-t_3.

III. ANALYSISING AND MODELLING FOR VOLTAGE MUTIPLIER

In this section, voltage analysis is showed in this part of article. We can ignoring the C_{out} because comparing to Sc, C_{out} is extremely small.

As showing in Fig. 3 and Fig. 4, the resonant inverter provide to the current only when the V_{cp} is constant neither $nV_i/2$ or $-nV_i/2$. The voltage multiplier only works in these situations so the circuit in Fig. 4(b) is neglected. It is reasonable to analysis Fig. 4(a) and Fig. 4(c).

For clarity, only two supercapacitors discusses in the model. The model also has two states. First the situation while current flow into odd-numbered diodes, on the contrary, the situation while current flow into even-numbered diodes.

According to KVL law, from Fig. 5(a) the secondary voltage of transformer which is input voltage for voltage multiplier can be expressed in following equation.

$$\begin{aligned} V_{S-E} &= V_m - V_{Cm-E} + V_D + I_{Cm}(\mathrm{r}_m + \mathrm{r}_D) \\ V_{S-E} &= V_m + V_n - V_{Cn-E} + V_D + I_{Cn}(\mathrm{r}_n + \mathrm{r}_D) \end{aligned} \tag{1}$$

where V_i is the voltage of supercapacitor, $V_{Ci\text{-}E}$ is voltage of C_1, V_D is voltage of diode, I_{ci} is current of diode in conduction angle. r_i and r_D are resistance of S_C and diode.

Also According to KVL law, from Fig. 5(b) the secondary voltage of transformer which is input voltage for voltage multiplier can be expressed in following equation.

$$\begin{aligned} V_{S-O} &= V_{Cm-O} + V_D + I_{Cm}(\mathrm{r}_m + \mathrm{r}_D) \\ V_{S-O} &= -V_m + V_{Cn-O} + V_D + I_{Cn}(\mathrm{r}_n + \mathrm{r}_D) \end{aligned} \tag{2}$$

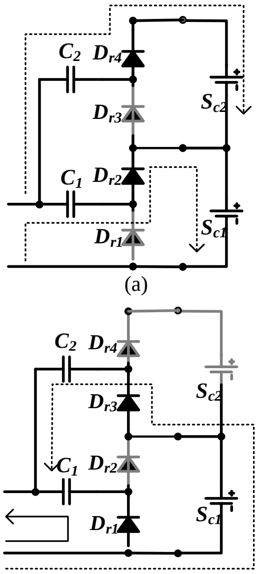


Figure 5. (a) Even-Numbered diodes are on (b) odd-numbered diodes are on

In practical, the outer capacitor flows larger current when the input voltage is larger. So it is necessary to use outer capacitors to reduce current of S_C.

Because two states are symmetrical, the input voltages of voltage multiplier are the same.

$$V_{S-E} = V_{S-O} = V_S \tag{3}$$

According to (1), (2):

$$\begin{aligned}\Delta V_{Ci} &= V_{Ci-O} - V_{Ci-E} \\ &= 2V_S - V_i - 2V_D - \frac{2\pi}{\theta} I_{Ci}(r_i + r_D)\end{aligned} \tag{4}$$

In general, the variation of capacitor can be expressed in following equation.

$$\Delta V = \frac{It}{C} = \frac{I}{Cf} = IR_{eq} \tag{5}$$

Finally Substitution (5) into (4):

$$2V_S = V_i + 2V_D + \frac{I_{Ci}}{2} R_{eq-i} \tag{6}$$

where R_{eq-i} is equivalent resistance of voltage multiplier:

$$R_{eq-i} = 2\{\frac{1}{C_i f} + \frac{2\pi}{\theta}(r_i + r_D)\} \tag{7}$$

$$V_{c1} = -(V_1/2) \tag{8}$$

$$V_{c2} = -(V_2/2+V_1) \tag{9}$$

So the voltage multiplier can be modeled as the following equivalent circuit.

The input voltage of multiplier doubles as $2V_S$, while the current halved as $I_{VM}/2$. $I_{VM}/2$ equals to sum of every Sc equalization charger current. $I_{VM}/2$ automatically distributes more current into the Sc which has lower voltage than the other SCs. In conclusion, the voltage multiplier can equal SCs' voltage automatically, without having voltage detection module. The voltage precision of equalization charger depends on R_{eq-I} (7). R_{eq-i} includes the equivalent resistance of C_i, Sc and diode. If the values of three factors C_1 r_1 and r_D are all the same as the value of another three factors, the voltage of the S_{c1} and S_{c2} will be identical. In other words, the effect of the equalization is excellent.

IV. DESGIN GUIDE

In this section, a design guide will be discussed. A equalization charger using parallel resonant inverter is designed to charge 8 supercapacitors. These 8 supercapacitors have different initial voltages. These voltages are 1.1V, 1.2V, 1.3V, 1.4V, 1.5V, 1.6V, 1.7V, 1.8V. The maximum power is 200W when the input voltage dc source is 100V. Q1 and Q2 work at the frequency of 195kHz. A voltage multiplier consist of C_i (C_i=100uF, r_i=100mΩ) and diodes (V_D=0.38, r_D=20mΩ).

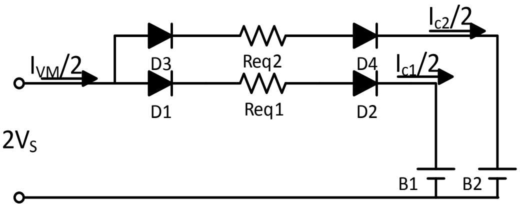


Figure 6. Equivalent of voltage multiplier

According to Fig. 6, I_{VM} is the sum of $I_{ci}/2$ which is the equalization charger current toward supercapacitor. Under a voltage-balanced condition:

$$\frac{I_{VM}}{2} = \frac{I_{c1}}{2} + \ldots + \frac{I_{c8}}{2} = \frac{200[\mathrm{W}]}{100[\mathrm{V}]} = 2[\mathrm{A}] \tag{10}$$

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{11}$$

Then L_r is designed to be 25uH while C_r is 30n, C_s is designed to be 1u and it is much larger than C_r.

V. SIMULATION RESULT

Simulate in Saber. The parameters of the prototype are as follows:

1) Input voltage: $v_{in} = 100V$;
2) Equalization charger current: $I_{eq} = 2A$;
3) Equalization charger power: $P_{eq} = 200W$;
4) Switching frequency of the converter: $195kHz$

The parameters of the PRI stage are as follows:

1) Magnetizing inductance: $L_r = 22uH$;
2) Resonance capacitor: $C_r = 30nF$
3) Blocking capacitor: $C_s = 1uF$
4) Duty ratio: $n = 4$;
5) Supercapacitor: $S_c = 200F$

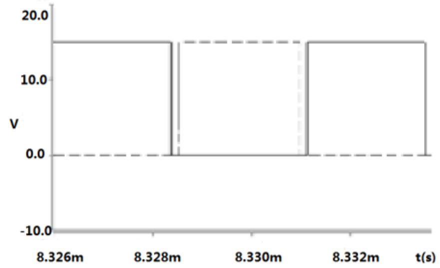
Fig. 7 shows the waveforms of constant duty cycle, the input voltage of resonance unit, current of L_r, the voltage of C_p, the voltage of C_s, the current of i_{VM} and even-numbered and odd-numbered Diode under voltage-balanced condition.

In Fig. 7(a), Duty cycle is 49.7% in order to prevent short circuit of Q_1 and Q_2.

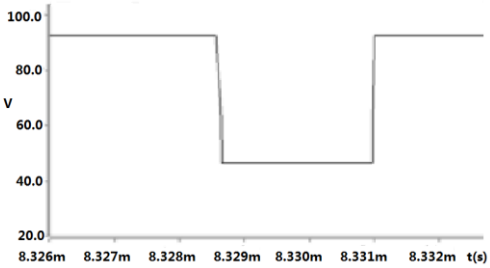
In Fig. 7(d), it can be seen that when the voltage of C_p is clamped to-$nV_i/2$ and +nVi/2, the voltage multiplier works. Energy from PRI distributes to the S_{Cs} to achieve the purpose of equalization charging.

In Fig. 7(e), it can be seen that C_s plays a role of not only the resonance unit component but also blocking capacitor.

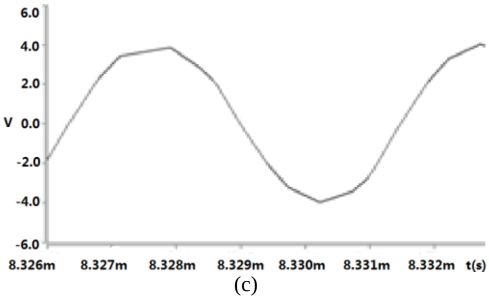
In Fig. 7(f), i_{VM} in the duty is different from the next duty because the S_{cs} is charging that means the changes on the voltages of S_{cs} influence i_{VM}.



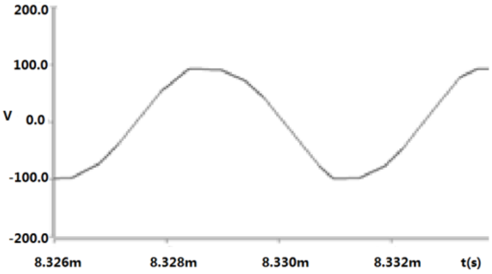
(a)



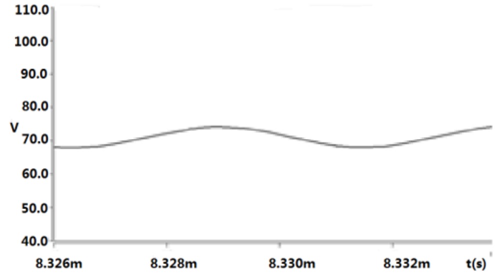
(b)



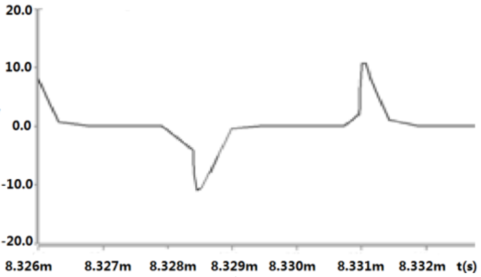
(c)



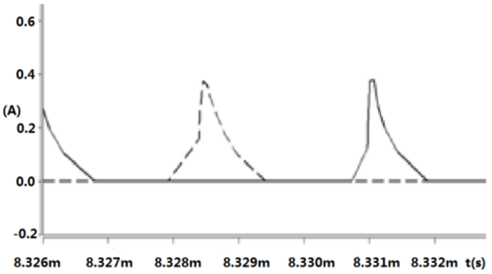
(d)



(e)

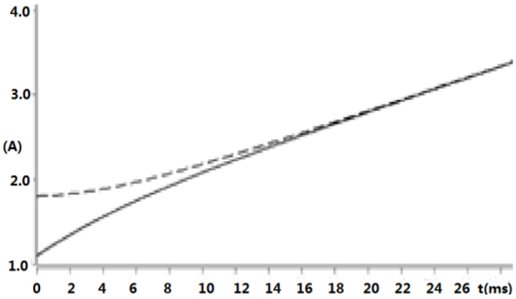


(f)

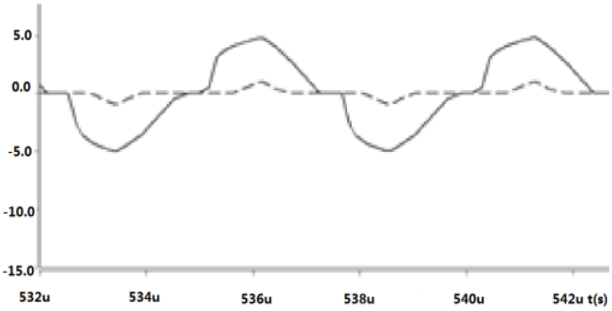


(g)

Figure 7. Simulation waveforms (a) constant duty cycle (b) the input voltage of resonance unit (c) current of L_r, (d) the voltage of C_p (e) the voltage of C_s (f) the current of i_{VM} (g) current of even-numbered (dotted line) and odd-numbered Diode (solid line)



(a)



(b)

Figure 8. Equlization of Sci (a) the voltage of Sc1 and Sc8 (b) the current of even-numbered and odd-numbered Diode

Fig. 8(a) shows the waveform of voltage of Sc1 and Sc8 and the current of even-numbered and odd-numbered Diode.

Because of large capacitor of Sc, the simulation time is extremely long. So in this situation use 10mF value instead of 200F.

It can be seen from this waveform that the voltage of Sc1 and Sc8 from unbalanced situation to balanced situation. The result is excellent using this topology.

In Fig. 8(b), it can be seen from this waveform that the voltage multiplier can automatically distribute more current into the Sc which have the lower voltage value.

VI. CONCLUSIONS

The equalization charger using parallel resonance and voltage multiplier has the advantage of topology simple and efficient, widely used in small and medium power applications while the volume of passive components constraint its further improve of the power density. A 200-W prototype of the proposed equalizer for 8 supercapacitors connected in series was built. The voltage of SCs initially different and imbalance eventually eliminates, then become the same voltage level.

ACKNOWLEDGMENT

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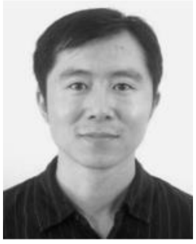

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