Design of Reliability Improvement in HV p-Channel LDMOS DUTs by a 0.25μm 60-V BCD Process

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***Abstract*—Different drain-side layout patterns for the 0.25μm 60-V high voltage p-channel Lateral-Diffused MOS device (pLDMOS) devices are investigated in this paper. For the anti-ESD capability evaluation, a drain-side "*pnp*" arranged-type for a pLDMOS-embedded-SCR structure is used to study this layout type's effect. Here, the layout types of P^+ region will be treated as some Continuous-Extended (CE) type into the drain-side manners and some Discrete-Distributed (DD) areas into the drain-side architectures, respectively. After all, from Transmission-Line Pulse (TLP) experimental data, it can be found that the DD-type layout manners in the drain-side have a better anti-ESD capability than that of the CE-type, and the secondary breakdown current (I_{t2}) values can be achieved above 7A (so good their are). On the other hand, the holding voltage (V_h) for the latch-up consideration of the CE-type shows an escalating trend, so it will be with higher anti-electrical-over-stress (EOS) capability.**

***Index Terms*—Electrical-Over-Stress (EOS), Electrostatic Discharge (ESD), embedded-SCR, holding voltage (V_h), p-channel-lateral-diffused MOS (pLDMOS), secondary breakdown current (I_{t2}), Transmission-Line Pulse (TLP), trigger voltage (V_{t1})**

I. Introduction

High-Voltage (HV) Lateral-Diffused Metal-Oxide-Semiconductor (LDMOS) devices are the dominant technology used in many applications nowadays, such as communication modules, power electronics components, power management circuits, automotive electronics, LCD drivers [1]-[7], its importance is increased in the HV purposes. Due to its high operating voltage, it needs to have a good reliability. Usually, hoping these devices has good reliability capabilities in the anti-ESD and/or Latch-Up (LU) immunity.

Usually, n-channel Lateral-Diffused MOS device (nLDMOS) device cells have a large cell area, therefore we hope it can be a anti-ESD protection component for its low on-resistance behavior, but it has several obvious shortcomings, including the Vt1 is too high and the device in a multi-finger structure can't completely turned-on, then it will result in per unit length the ESD capacity is too low. On the other hand, a conventional SCR is also used in HV applications due to have a very strong ESD capacity per unit length, but it also has some disadvantages, including the Vh is too low. Then, there are some studies brightening an idea to combine these two components [8]-[15]. An ESD protection circuit in the power port, the nLDMOS device is easily prone to the latch-up happening, so using a pLDMOS will have some advantages; however the pLDMOS has a higher Vh value than an nLDMOS, and its anti-ESD efficiency is lower than an nLDMOS. In this paper, an N+ implants in the drain-side of a pLDMOS to form a pLDMOS with an embedded SCR structure, so that these two elements can be corporate their characteristics to achieve a high anti-ESD and a high anti-LU abilities.

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II. HV Test Devices and Design Methods

A. pLDMOS-Embedded-SCR ("pnp"-P^+ CE Type in the Drain-Side)

Here, the experimental tested devices of pLDMOS and pLDMOS-SCR were fabricated by a TSMC 0.25-μm 60-V BCD process. The channel length (L) is kept to be 2-μm, channel width of each finger (W_f) is 100-μm, finger numbers M=6, and the total channel width (W_{tot}) is kept a constancy, 600-μm. Fig. 1 and Fig. 2 are the cross-section and schematic layout of a pLDMOS-SCR conventional stripe-type, respectively. From this cross-section illustration, a pLDMOS is divided into three zones in the drain-side, and then the N^+ doses implanted into the center region to form a parasitic SCR structure, which called the pLDMOS-SCR "*pnp*"-type structure. From Fig. 1~Fig. 2, a reference DUT is defined as with adding an original stripe type SCR structure of the pLDMOS device which was not modulated in the drain-side. In the first part, the layout type of these P^+ regions from the original stripe type was changed to the P^+ region continuous extended toward the middle region of the N^+ diffusion region by some fixed spacing intervals. Then, the P^+ diffusion area of a pLDMOS will be increased, which is used to verify whether its anti-ESD ability of a pLDMOS will increase or not?

The experimental groups of part-1 are shown in Table I, where there are five different planning parameters. The interval between two adjacent extended P^+ region are kept two contact spacing and the segment length of every P^+

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extension area into the middle N^+ zone are kept to be 3, 11, 24, 63, 128 contact spacing. Therefore, the P^+ to N^+ area ratios of these samples is not same. Meanwhile, this part will be compared with the reference DUT (none-modulated pLDMOS-SCR ("*pnp*") stripe type); we hope to find an optimum ratio value for the best anti-ESD ability. These high-voltage pLDMOS-SCR ("*pnp*") DUTs with a P^+ continuously extended type in the drain-side are listed in Table I and a schematic layout of (CE 3_2co) device is shown in Fig. 3.

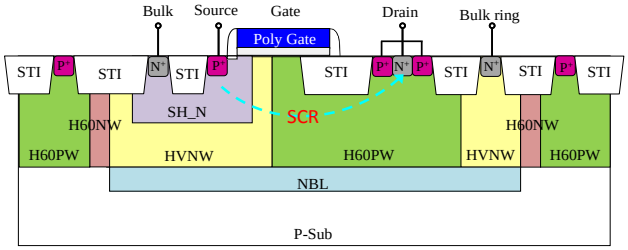

Figure 1. Cross-Section diagram of an HV pLDMOS-SCR ("*pnp*" conventional stripe-type).

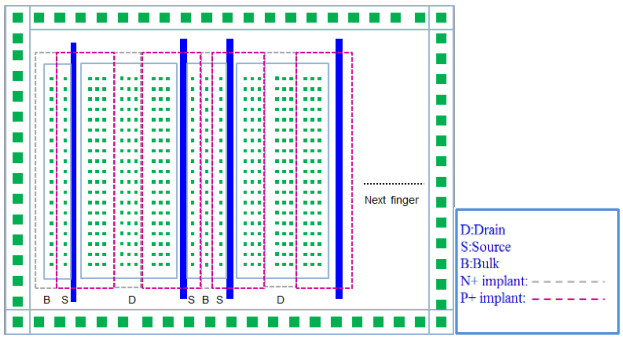

Figure 2. Schematic layout of an HV pLDMOS-SCR ("*pnp*" conventional stripe-type).

TABLE I. DEVICE LISTS OF PLDMOS-SCR ("*PNP*") DUTS WITH A P^+ CE-TYPE

Types	Cell name
1	pLD_pnp_CE 3_2co
2	pLD_pnp_CE 11_2co
3	pLD_pnp_CE 24_2co
4	pLD_pnp_CE 63_2co
5	pLD_pnp_CE 128_2co

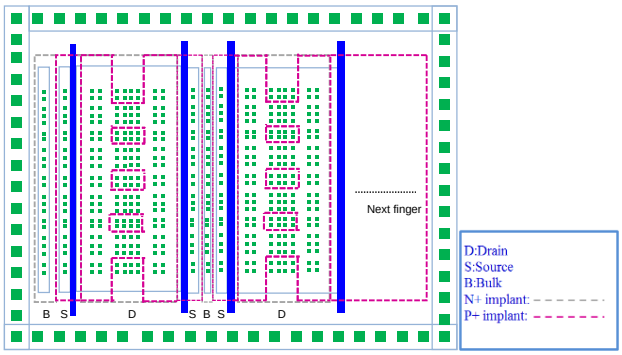

Figure 3. Schematic layout of an HV pLDMOS-SCR ("*pnp*") with a CE-type (CE 3_2co-type).

B. pLDMOS-Embedded-SCR ("pnp"-P^+ DD Type in the Drain-Side)

In the previous section, the HV pLDMOS-SCR ("*pnp*") with a drain-side P^+ continuous extended type makes the drain-side P^+ diffusion area increasing, which is used check more the drain-side P^+ diffusion area with regard to the pLDMOS-SCR whether positive to the anti-ESD capacity or not? In this section, the P^+ diffusion area will be reduced in the drain-side by the P^+ discrete distributed type, which is acted to increase the parasitic SCR area. A schematic layout of (DD 3_2co) high-voltage pLDMOS-SCR ("*pnp*") DUT with a P^+ discrete distributed type in the drain-side is shown in Fig. 4.

Similarly, the experimental groups of part-2 are shown in Table II, where there are five different planning parameters. The interval between two adjacent discrete P^+ region are kept two contact spacing and the segment length of every P^+ discrete area in the drain-side are kept to be 3, 11, 24, 63, 128 contact spacing. Therefore, the P^+ to N^+ area ratios of these samples is not same. Meanwhile, this part will be compared with the reference DUT (none-modulated pLDMOS-SCR ("*pnp*") stripe type); we hope to find an optimum ratio value for the best anti-ESD ability.

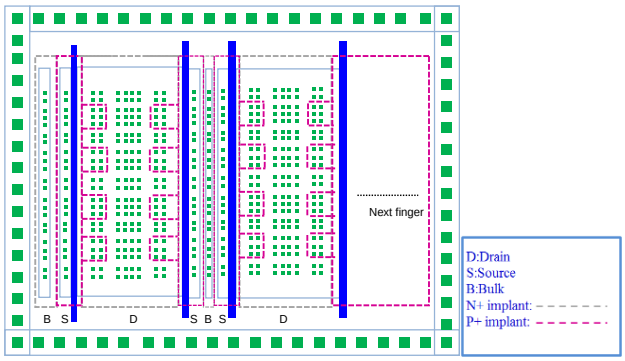

Figure 4. Schematic layout of a pLDMOS-SCR ("*pnp*") with a P^+ DD-type (DE3_2co).

TABLE II. DEVICE LISTS OF PLDMOS-SCR ("*PNP*") DUTS WITH A P^+ DD-TYPE

Types	Cell name
6	pLD_pnp_ DD 3_2co
7	pLD_pnp_ DD 11_2co
8	pLD_pnp_ DD 24_2co
9	pLD_pnp_ DD 63_2co
10	pLD_pnp_ DD 128_2co

III. TESTING EQUIPEMENT

A Transmission-Line-Pulse (TLP) testing system will be used to measure the high-current snapback key parameters of these ten kinds of pLDMOS–embedded SCR DUTs. A TLP tester can offer a continuous step-high pulse to a Device-Under-Testing (DUT), and shortly rising/falling time of the continuous square wave can also simulate the transient noise of an ESD incident. Then, it is behaved as a short square wave with a 100-ns pulse

width and less 10-ns rising/falling times to evaluate the device snapback I-V response.

IV. Testing Results and Discussion

A. pLDMOS-Embedded-SCR ("pnp"-P^+ CE Type in the Drain-Side)

The snapback I-V curves of HV pLDMOS-SCR ("*pnp*") with a drain-side P^+ continuously extended type are shown in Fig. 5. It can be found that the reference group which does not modulate the SCR structure and with the I_{t2} value is averaged about 6.84A, however the I_{t2} value of five continuously modulated groups are falling between 0.7~0.9A. The V_{t1}, V_h, and I_{t2} distributions are shown in Fig. 6~Fig. 7 and Table III. And, the breakdown voltage (V_{BK}) distribution by using a Keithley 2410 is also shown in Table III (under the V_g=V_s=VDD bias condition).

Here, the P^+ continuously extended type in drain-side makes the P^+ area expansion. In the same meaning, when one does expand the drain-side area of a pLDMOS which will weaken the contribution of the parasitic SCR. Therefore, the testing results of I_{t2} value of these continuously extended are all within the range of 0.7~0.9A. As the proportion of N^+/P^+ (the proportion of this parasitic SCR) lower, the capability of anti-ESD is significantly decreased. But, the V_h values of this type arrangement are good for the LU immunity (improvement more than 10.5% as compared with the reference DUT).

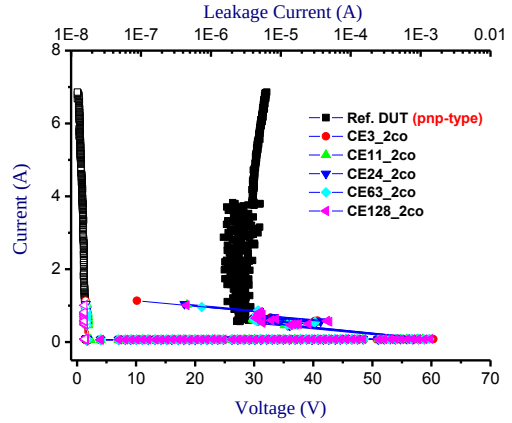

Figure 5. Snapback I-V curves & leakage currents of pLDMOS-SCR ("*pnp*" type) P^+ drain-side CE-types in the drain side.

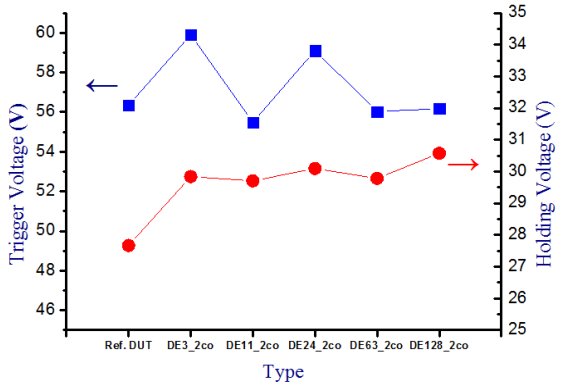

Figure 6. Relationship diagrams of V_{t1} & V_h values values of pLDMOS-SCR ("*pnp*" type) P^+ drain-side CE-types in the drain side.

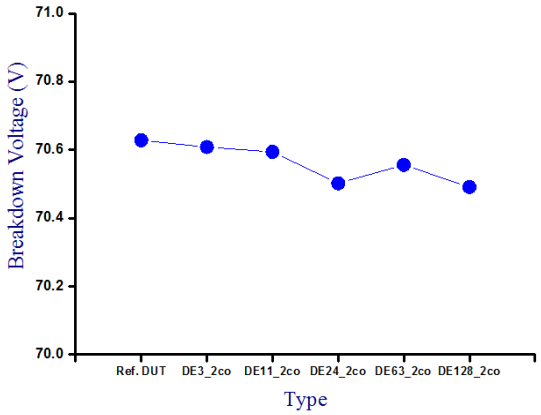

Figure 7. Relationship diagrams of breakdown-voltage values of pLDMOS-SCR ("*pnp*" type) P^+ drain-side CE-types in the drain side.

TABLE III. Snapback Key Parameters of pLDMOS-SCR ("*pnp*" Type) DUTs

pLDMOS+SCR ("*pnp*"-type)		V_{t1} (V)	V_h (V)	I_{t2}(A) (mean ±σ)	V_{BK} (V)
Ref. DUT	pLDMOS_pnp	56.345	27.670	> 7	70.628
CE-types	CE 3_2co	59.903	29.841	0.91 ±0.13	70.608
	CE 11_2co	55.483	29.707	0.78 ±0.09	70.594
	CE 24_2co	59.099	30.096	0.80 ±0.08	70.502
	CE 63_2co	56.027	29.783	0.76 ±0.16	70.556
	CE 128_2co	56.166	30.574	0.74 ±0.12	70.491
DD-types	DD 3_2co	41.735	6.655	> 7	58.322
	DD 11_2co	43.793	8.089	> 7	58.461
	DD 24_2co	42.391	8.088	> 7	58.017
	DD 63_2co	45.130	8.074	> 7	58.162
	DD 128_2co	42.715	8.189	> 7	58.188

B. pLDMOS-Embedded-SCR ("pnp"-P^+ DD Type in the Drain-Side)

The snapback I-V curves of HV pLDMOS-SCR ("*pnp*") with a drain-side P^+ discrete distributed type are shown in Fig. 8. It can be found that the I_{t2} values are all larger than 7A (due to the electric power limitation of this TLP measurement system, a measurement will be stopped when the internal current of DUTs is more than 7A). Meanwhile, the V_{t1}, V_h and I_{t2} distributions are shown in Table III. And, the breakdown voltage (V_{BK}) distribution by using a Keithley 2410 is also shown in Fig. 9~Fig. 10 and Table III (under the V_g=V_s=VDD bias condition).

Then, the P^+ discrete distributed type in drain-side makes the P^+ area shrink. In the same meaning, when one does shrink the drain-side area of a pLDMOS which will strengthen the contribution of the parasitic SCR. Therefore, the testing results of I_{t2} value of these discrete distributed DUTs are all above 7A. As the proportion of N^+/P^+ (the proportion of this parasitic SCR) higher, the capability of anti-ESD can be kept significantly good. But, the V_{t1} and V_h values of this type arrangement are decreased as compared with the reference DUT.

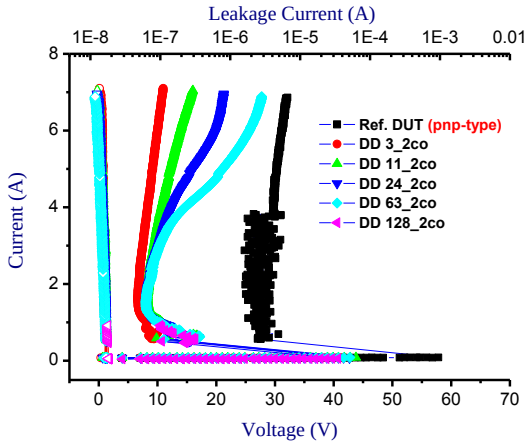

Figure 8. Snapback I-V curves & leakage currents of pLDMOS-SCR ("*pnp*" type) P^+ type drain-side DD-type in the drain side.

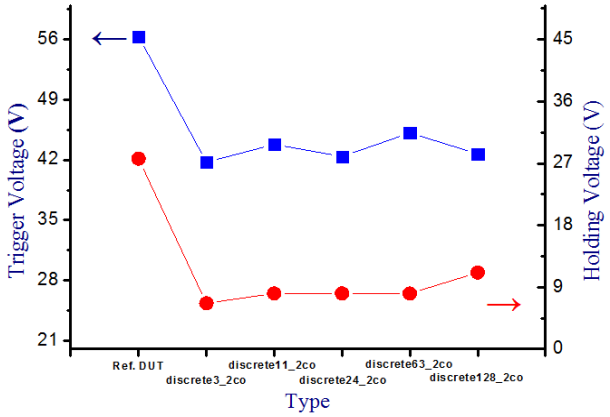

Figure 9. Relationship diagrams of V_{t1} & V_h values values of pLDMOS-SCR ("*pnp*" type) P^+ drain-side DD-types in the drain side.

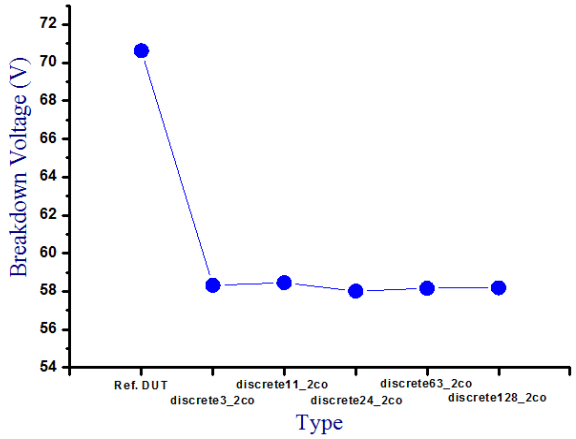

Figure 10. Relationship diagram of breakdown-voltage values of pLDMOS-SCR ("*pnp*" type) P^+ type drain-side DD-types in the drain side.

V. Conclusion

An implementation of the embedded-SCR in drain-side corporate with CE- and DD-types pLDMOS has been demonstrated in this paper. From this work, it can be found that the n^+ implanted location and percentage of a pLDMOS with embedded SCRs in the drain-side will have a strong impact on the anti-ESD robustness. Through a systematic design and analysis of experiment DUTs, we can find that the layout type of DD of p^+ region in the drain-side have a better capability of anti-ESD than the CE-type, it's I_{t2} value can be reached over 7 A. However, the holding voltage (V_h) of CE-type has higher value and this type arrangement is good for the LU immunity (improvement more than 10.5% as compared with the reference DUT). Therefore, the layout type of p^+ CE-type in the drain-side can use to reduce the possibility of LU happening.

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