A Minimum Manhattan Distance Retrieving Circuit Using Neuron CMOS Inverters

Yujiro Harada¹, Kuniaki Fujimoto¹, Kei Eguchi², Masaaki Fukuhara³, and Masahiro Yoshida³
³Graduate school of Industrial Engineering, Tokai University, Kumamoto, Japan
²Department of Information Electronics, Fukuoka Institute of Technology, Fukuoka, Japan
¹Department of Embedded Engineering, Tokai University, Tokyo, Japan
Email: 4bijm002@mail.tokai-u.jp, eguti@fit.ac.jp, {fujimoto, fukuhara, yoshida}@tokai.ac.jp

Abstract—According to the development of information technologies, a high-speed similar data retrieval system is becoming important to retrieve similar data from mass data in database for character recognition, fingerprint recognition, data compression, color image recognition, and so on. However, the conventional similar data retrieval system implemented by software or hardware using conventional memory is slow, because a computer must compare the called data sequentially. For this reason, in order to retrieve similar data, an associative memory has been studied in recent years. In this paper, by utilizing a neuron CMOS inverter, we propose a novel minimum Manhattan distance retrieving circuit as an important functional block of the associative memory. The proposed circuit is less affected by the influence of the initial charge and the variation of threshold voltage. The effectiveness of the proposed circuit is demonstrated by the Simulation Program with Integrated Circuit Emphasis (SPICE) simulations.

Index Terms—Manhattan distance, associative memory, neuron CMOS inverter, time domain

I. INTRODUCTION

According to the development of information technologies, a high-speed similar data retrieval system is becoming important to retrieve similar data from mass data in a database. For example, the similar data retrieval system is utilized for character recognition, fingerprint recognition, data compression, color image recognition, and so on. For this reason, the improvement in speed performance of the similar data retrieval system is strongly recommended. In the measurement of similarity between stored data and input data, the Hamming distance or the Manhattan distance is commonly used [1]. For example, the Hamming distance is used for the recognition such as character, fingerprint, and so on. On the other hand, the Manhattan distance is used for data compression and color image recognition. However, the similar data retrieval system implemented by software is slow, because a computer must compare the called data sequentially. Also, basic process is the same as in the case of software implementation even when it is implemented with hardware using the conventional memory. In these methods, the retrieval time increases in proportion to the increase of data volume. For this reason, in order to retrieve similar data, an associative memory has been studied in recent years [2]-[6]. However, the conventional methods are of no practical use. Unlike the conventional retrieval system, humans can instantly retrieve for the data showing features which are most similar to the inputs among data which have been already stored in the brain.

By utilizing a neuron CMOS inverter which has similar characteristics to a brain neuron [7], we propose a minimum Manhattan distance retrieving circuit as an important functional block of the associative memory. Due to the influence of the initial charge and the variation of threshold voltage in neuron MOS transistors, a malfunction is occurred in conventional circuits using neuron MOS transistors [8]-[10]. In the proposed circuit, the voltage of the floating gate of neuron CMOS inverters is equal to its threshold voltage by connecting the output to the floating gate of neuron CMOS inverters before retrieving process. Owing to this operation, the influences of the initial charge and the variation of threshold voltage can be eliminated. The proposed circuit also achieves high retrieving speed by using fully parallel processing. Furthermore, the proposed circuit can retrieve not only the completely matched data but also the most similar data. To confirm the validity of the proposed circuit, Simulation Program with Integrated Circuit Emphasis (SPICE) simulations are performed.

II. CIRCUIT CONFIGURATION OF THE DATA COINCIDENCE DETECTOR

First, we describe a data coincidence detector using a neuron CMOS inverter. In the proposed minimum Manhattan distance retrieving circuit, the data coincidence detector is one of the most important building blocks. The Manhattan distance between \((A_1, \ldots, A_M)\) and \((B_1, \ldots, B_M)\) and \((B_1, \ldots, B_M)\) is defined as follows:

\[
D_{Manh} = \sum_{j=1}^{M} |A_j - B_j|
\]  

In (1), \(A_j\) and \(B_j\) \((j = 1, 2, \ldots, M)\) are binary data with \(N\)-bits \((N = 1, 2, \ldots)\) and \(M\)-elements \((M = 1, 2, \ldots)\).

Fig. 1 shows the circuit configuration of the data coincidence detector using a neuron CMOS inverter,
where the input data and the reference data are expressed as $(A_1, \ldots, A_i, \ldots, A_M)$ and $(B_1, \ldots, B_j, \ldots, B_M)$, respectively. In Fig. 1, $V_{dd}$ is the supply voltage, $F$ is the control voltage to start the retrieving for the matching data, $G$ is the control voltage for the most similar data retrieving, $SW_1$ is the switch to set the floating gate voltage $V_F$ of the neuron CMOS inverter $\nu$CMOS to the threshold voltage $V_{TH}$ and $SW_2$ is the switch to enable the retrieving for the matching data. In the neuron CMOS inverter $\nu$CMOS, the capacitances $C_{0,i}$, $C_{i,j}$ $(i = 1, 2, \ldots, N)$ and $C_H$ between the floating gate and the input terminal of $\nu$CMOS are designed to satisfy the following conditions:

$$C_{0,i} = C$$

(2)

$$C_{i,j} = 2^{-1}C$$

(3)

and

$$C_H = C$$

(4)

In this case, the output of $\nu$CMOS inverter, the $\nu$CMOS and $\nu$CMOS are designed to satisfy the following conditions: First, the control voltage $F$ is set to a low level, $G$ is set to a high level, the switch $SW_1$ is turned “ON,” and the $SW_2$ is connected to the lower side. In this case, the floating gate voltage $V_F$ of $\nu$CMOS is expressed as:

$$V_F = V_{TH}$$

(7)

here, all the outputs of NAND become a high level and the output $OUT$ becomes a low level, because $F$ is at a low voltage level.

Next, the $SW_2$ is connected to the upper side after the $SW_1$ is turned “OFF”. Here, we consider about the floating gate voltage $V_F$ of $\nu$CMOS. When the voltage of the input terminal that has the capacitance $C_i$ between the input terminal and the floating gate is changed by $AV$, the amount of change in the voltage $V_F$, $AV_F$, is expressed as:

$$AV_F = \frac{C_i}{C_T} AV$$

(8)

In (8), $C_T$ is the total of the capacitance between the input terminal and the floating gate of $\nu$CMOS and the capacitance $C_F$ between the floating gate and the substrate. The total capacitance $C_T$ is expressed as:

$$C_T = \sum_{j=1}^{M} \left( C_{0,i} + \sum_{i=1}^{N} C_{i,j} \right) + C_H + C_F$$

(9)

When the $SW_2$ is connected to the upper side, the voltage of the lowest input terminal $V_{dd}$ of $\nu$CMOS changes from $V_{TH}$ to $V_{dd}$. Therefore, from (4), (7) and (8), the floating gate voltage $V_F$ is obtained as:

$$V_F = V_{TH} + \frac{C}{C_T} (V_{dd} - V_{TH})$$

(10)

In this case, the output of $\nu$CMOS becomes a low level, because $V_F$ exceeds the threshold voltage $V_{TH}$ as shown in (10).

Next, the control voltage $F$ is set to a high level. When the $i$-th element $e_{i,j}$ of the $j$-th element $E_{i,j}$ or borrow, are at a high level, the output $V_{ij}$ of NAND or $V_{aj}$ become 0V from the supply voltage $V_{dd}$. In this case, we define the floating gate voltage $V_F$ as $V_{F'}$. From (2), (3), (8), and (10), the voltage $V_{F'}$ is expressed as:

$$V_{F'} = V_{TH} + \frac{C}{C_T} (V_{dd} - V_{TH}) - \sum_{j=1}^{M} \left( \frac{C}{C_T} (V_{dd} - V_{0,i,j}) + \sum_{i=1}^{N} 2^{-1}C (V_{dd} - V_{i,j}) \right)$$

(11)

Then, (11) is rewritten as:

$$V_{F'} = V_{TH} + \frac{C}{C_T} (V_{dd} - V_{TH}) - \sum_{j=1}^{M} |A_i - B_j| \frac{C}{C_T} V_{dd}$$

$$= V_{TH} + \frac{C}{C_T} (V_{dd} - V_{TH}) - D_{mean} \frac{C}{C_T} V_{dd}$$

(12)

As (12) shows, $V_{F'}$ is lower than the threshold voltage $V_{TH}$. Therefore, the output of $\nu$CMOS becomes a high level and the output $OUT$ remains a low level. When the input data $(A_1, \ldots, A_i, \ldots, A_M)$ is fully equal to the reference data $(B_1, \ldots, B_j, \ldots, B_M)$, all $E_j$ becomes 0V. The
voltage of the floating gate, $V_F$, does not change from (10), because all the outputs of NAND remain a high level and the output of vCMOS also remains a low level. Therefore, the output $OUT$ becomes a high level. As explained above, the proposed circuit can detect the coincidence between $(A_1, ..., A_j, ..., A_m)$ and $(B_1, ..., B_j, ..., B_m)$. When the control voltage $V_G$ exceeds the threshold voltage $V_{TH}$, the output of the multi-input OR becomes a high level. The data coincidence detector used in the proposed circuit converts the Manhattan distance into a time. If one of $OUT_i$ becomes a high level, the output of the multi-input OR becomes a high level. The rising of the all floating gate voltage is stopped, because $M_3$ becomes “OFF”. Therefore, the output $OUT_i$ which is the place of the reference data with the smallest Manhattan distance becomes a high level first. If there are some reference data with the smallest Manhattan distance, the data coincidence detection can be performed stably by setting the off time of the transistor $M_3$ to $\Delta T_i$.

As (12) shows, the floating gate voltage $V_F$ decreases in proportion to the Manhattan distance $D_{Manh}$ when the input data $(A_1, ..., A_j, ..., A_m)$ is not equal to the reference data $(B_1, ..., B_j, ..., B_m)$. When the control voltage $V_G$ is set to a low level, the pMOS transistor $M_3$ is turned “ON.” Then the constant current flows from the drain of $M_3$ to the floating gate of vCMOS. The floating gate voltage $V_F$ begins to rise linearly from $V_F'$. When $V_F$ exceeds the threshold voltage $V_{TH}$, the output of the neuron CMOS inverter becomes a low level, and the output $OUT$ becomes a high level. If the constant current that flows through $M_3$ is $I$, the time $T$ taken from the output $OUT$ becomes a high level to the control voltage $V_G$ becomes a low level is expressed as:

$$T = \frac{C_L (V_{TH} - V_{F'})}{I}$$  \hspace{1cm} (13)

By substituting (12) into (13), the time $T$ is expressed as:

$$T = \frac{C_L (V_{TH} - V_{TH}) - \frac{C}{C_L} (V_{DD} - V_{TH}) + D_{Manh} \frac{C}{C_L} V_{DD}}{I}$$

$$= D_{Manh} \frac{C}{I} V_{DD} - \frac{C}{I} (V_{DD} - V_{TH})$$  \hspace{1cm} (13)

As we can see from (14), the time $T$ is invariant to the parasitic capacitance and the initial charge. When the difference of the Manhattan distance is 1, the time lag $\Delta T$ is expressed as:

$$\Delta T = \frac{C}{I} V_{DD}$$  \hspace{1cm} (13)

From (15), the change of the threshold voltage $V_{TH}$ doesn’t affect the time lag for the difference of the Manhattan distance.

### III. CIRCUIT CONFIGURATION OF THE MINIMUM MANHATTAN DISTANCE RETRIEving CIRCUIT

Fig. 2 shows the circuit configuration of the proposed minimum Manhattan distance retrieving circuit. The proposed circuit is constituted by arraying $L (=2, 3, ...)$ data coincidence detectors when the number of words is $L$. The control voltage $V_G$ of the data coincidence detector is connected to the output of the multi-input OR. In Fig. 2, $H$ is the control voltage to retrieve the most similar data. The data retrieval is started when the $H$ becomes a low level.

The operation principle of the proposed circuit will be described. The operation of the proposed circuit can be divided into three cases: 1. If the reference data $B_k = (B_{1,k}, ..., B_{j,k}, ..., B_{m,k})$ ($k = 1, 2, ..., L$) completely matches the input data $A=(A_1, ..., A_j, ..., A_m)$ and the control voltage $V_F$ is at a high level, the output of the data coincidence detector, $OUT_i$, becomes a high level. 2. If the reference data $B_k$ does not completely match the input data $A$, all the output $OUT_i$ remain a low level. 3. If the reference data $B_k$ does not match the input data $A$ at all, the control voltage $H$, the pMOS transistor $M_3$ becomes “ON.” Therefore, the constant current begins to flow, and the floating gate voltage starts to rise. The data coincidence detector used in the proposed circuit converts the Manhattan distance into a time. If one of $OUT_i$ becomes a high level, the output of the multi-input OR becomes a high level. The rising of the all floating gate voltage is stopped, because $M_3$ becomes “OFF”. Therefore, the output $OUT_i$ which is the place of the reference data with the smallest Manhattan distance becomes a high level first. If there are some reference data with the smallest Manhattan distance, the data coincidence detection can be performed stably by setting the off time of the transistor $M_3$ to $\Delta T_i$.

By above-mentioned operations, the proposed circuit can find out the matching data from the input data when the control voltage $V_F$ is set to a high level. Furthermore, the proposed circuit can find out the reference data which is the most similar to the input data when the control voltage $H$ is set to a low level.

IV. SIMULATION

As an example of the proposed minimum Manhattan distance retrieving circuit, we performed the HSPICE simulations concerning the proposed circuit with 4-bits, 2-elements, and 8-words. In these simulations, we assumed a ROHM 0.18\textmu m CMOS process as a transistor model. The conditions of the SPICE simulations are as follows: \( V_{DD} \) is 1.8V and the threshold voltage of the floating gate of neuron CMOS inverters, \( V_{TH} \), is 0.9V.

Fig. 3 shows the simulation results when the reference data with Manhattan distance 0-15 is inputted. In this figure, \( t_1 \) denotes the point when the control voltage \( F \) is set to a low level, SW\(_1\) is turned “ON” and SW\(_2\) is connected to the lower side, \( t_2 \) denotes the point when SW\(_1\) is turned “OFF” and SW\(_2\) is connected to the upper side, and \( t_3 \) denotes the point when the control voltage \( F \) is set to a high level. As Fig. 3 shows, the floating gate voltage \( V_F \) is equal to the threshold voltage \( V_{TH} \) at the point \( t_1 \). At the point \( t_2 \), \( V_F \) exceeds \( V_{TH} \). And the floating gate voltage \( V_F \) decreases in proportion to the Manhattan distance at the point \( t_1 \). Fig. 4 shows the floating gate voltage \( V_F \) as a function of the Manhattan distance. In this figure, the floating gate voltage \( V_F \) satisfies (12) and is expressed as a linear function of the Manhattan distance.

Fig. 5 shows the simulation results when the reference data with the minimum Manhattan distance 1-16 is inputted. Fig. 6 shows the retrieval time as a function of the Manhattan distance, where the ordinate represents the time when \( V_F \) reaches \( V_{TH} \). As Fig. 5 and Fig. 6 show, the retrieval time increases linearly in proportion to the Manhattan distance. In this simulation, the retrieval time is 32.3ns when the Manhattan distance is 16.
Fig. 7 shows the simulated output waveform, where the relationships of I/O data were set as shown in Table I. As Table I shows, the input data \( A \) completely matches the reference data \( B \). In Fig. 7, the output \( \text{OUT}_2 \) and \( \text{OUT}_3 \) are a high level after the control voltage \( H \) becomes a low level. Therefore, we can confirm that the proposed circuit is able to find out the most similar data.

V. CONCLUSION

In this paper, we proposed a novel minimum Manhattan distance retrieving circuit using neuron CMOS inverters. By converting the Manhattan distance to the time, the proposed circuit can retrieve for the data with the minimum Manhattan distance using a fully parallel operation. Unlike conventional circuits, the proposed circuit is less affected by the initial charge of the floating gate and the variation of threshold voltage. The validity of the proposed circuit was confirmed through SPICE simulations.

In a future study, we will apply the proposed circuit to associative memories and confirm the operation by experiments using an integrated circuit.

**REFERENCES**


Yujirō Harada is a graduate student at the Graduate School of Industrial Engineering, Tokai University, Kumamoto, Japan. He received The 4th Unique Self-IC-Fabrication Contest in Hibikino Award for excellence. His research interests include digital circuits and integrated circuits.
Kuniaki Fujimoto received the B.E., the M.E., and the D.E. degrees from Tokai University, Japan, in 1987, 1989, and 2009. He is currently a professor of Tokai University, Kumamoto, Japan. He is received The 1st Unique Self-IC-Fabrication Contest in Hibikino Award for excellence, The 2nd Unique Self-IC-Fabrication Contest in Hibikino Highest Award and Award for excellence, The 4th Unique Self-IC-Fabrication Contest in Hibikino Award for excellence, and KKU-IENC2014 Outstanding Paper Award. His research interests include pulse circuit and digital circuit.

Kei Eguchi received the B.E., the M.E., and the D.E. degrees from Kumamoto University, Kumamoto, Japan, in 1994, 1996, and 1999. He is currently a professor of Fukuoka Institute of Technology, Fukuoka, Japan. He is an associate editor of ICIC express letters, an associate editor-in-chief of IJIES, an editorial board of engineering & technology of IIE, a senior member of IEEJ of Japan and APCBEEs. He received ICIAE2015 Best Presentation Award, ICPEE2014 Excellent Oral Presentation Award, iCABSE2014 Excellent Paper Award, KKU-IENC2014 Outstanding Paper Award, ICEEN2014 Excellent Paper Award, JTL-AEME2013 Best Paper Award, ICTEEP2013 Best Session Paper Award, 2010 Takayanagi Research Encouragement Prize, 2010 Paper award of the Japan Society of Technology Education, ICICIC2009 Best Paper Award, ICINIS2009 Outstanding Contribution Award, and IEEE MWSCAS 2004 Best 10 Paper. His research interests include switching converters and integrated circuits.

Masaaki Fukuhara received the B.E., the M.E. and the D.E. degrees from Tokai University, Kanagawa, Japan, in 2002, 2004 and 2007 respectively. He is currently an assistant professor at the Department of Embedded Technology, Tokai University, Tokyo, Japan. His research interests include neuron MOS transistor and the application to CAM LSI's.

Masahiro Yoshida received the B.E., the M.E. and the D.E. degrees from Tokai University, Japan, in 1976, 1978, and 1990 respectively. He is currently a professor at the Department of Embedded Technology, Tokai University, Tokyo, Japan. His research interests include low power CMOS’s LSI, CAM’s LSI and charge-pump circuits.