A Low Noise Figure Single-to-Differential Low Noise Amplifier for Wideband Application

Ro-Min Weng, Li-Wei Chen, and Ren-Yuan Huang
Department of Electrical Engineering, National Dong Hwa University, 97401 Hualien, Taiwan
Email: romin@mail.ndhu.edu.tw

Abstract—A wideband Single-to-Differential Low-Noise Amplifier (STDLNA) is proposed in this paper. An input network and inverters are implemented to achieve input resistance matching of 50ohm. A common-source amplifier and a common-gate amplifier are employed to generate a pair of differential signals. An Agilent momentum electromagnetic simulation tool is used to demonstrate the design concept. With 0.18um CMOS process parameters, the presented STDLNA provides a noise figure of 3.37-3.7dB. The maximum power gains S21 and S31 within the wideband are 13.44 dB and 13.47 dB, respectively. The input and output reflection coefficients are both below -10dB. The linearity IIP3 at 4GHz is -8dBm. The maximum gain and phase imbalance of the differential output ports are 0.3dB and 2.97 degree, respectively. The core circuit excluded output buffers consumes 19.53mW at 1.3V supply voltage. The chip size including pads is 1.2935mm*1.088mm.

Index Terms—LNA, single to differential, active balun

I. INTRODUCTION

The availability of wideband wireless systems has attracted much attention due to their high data transmission rate [1]. Wireless receivers are essential for systems to receive incoming radio-frequency signals. Among front-end circuits in receivers, Low Noise Amplifiers (LNAs) are applied for input signal amplification. A Single-to-Differential Low Noise Amplifier (STDLNA) which combines an LNA with an output balance-to-unbalance (balun) circuit is popular and can be connected directly to the input ports of mixers. The differential outputs are required to have the gain amplitude difference of 0dB and the phase difference of 180 degree. Normally, a traditional passive balun using LC networks or transformers often occupies large chip area. Therefore, an active balun with small chip size and low cost is a better choice. A single transistor could be regarded as an active balun for the phase difference between drain and source is 180 degree [2], [3]. A fully differential amplifier with a single input port was presented [4]. Also, a series feedback path with inductive source degeneration was applied to common source topology [5]. An active balun was designed Common-Source (CS) and Common-Gate (CG) topology [6], [7]. Compared to a CS stage, an inverter has a lower noise figure at the same biasing current. The output buffer is used to increase the gain.

In Section II, a novel STDLNA is proposed and analyzed. The chip implementation and EM simulation results of the designed STDLNA are given in Section III. Finally, conclusion remarks are made in Section IV.

II. PROPOSED SINGLE-TO-DIFFERENTIAL LNA

Fig. 1 shows the schematic of the proposed wideband STDLNA employing CS-CG topology. There are three stages including an input impedance matching stage, a single-to-differential amplifier stage and an output driver stage.

The first stage employs a push-pull inverter and matching components. The input matching done by M2, M3, R4, L1, L2, and C1 is able to match an antenna impedance of 50.

The second stage employs CS (M1) and CG (M4) amplifiers which generate a phase difference of 180 degree with the same amplitude. A pair of phase differential signals is therefore obtained at the output ports of CS (M1) and CG (M4) amplifiers. The single-to-differential core components are M1, M6, R2, R5, and L5. The maximum gain is determined by the second stage. Inductor L4 is added to extend the circuit bandwidth for wideband design.

The third stage using differential amplifiers (M5, M6), L6 and L7, acts as output buffers. RF output signals can be improved by the output driver stage. The passive components, R8, R9, C5, and C6, are parts of the output matching network at both ends.
A. Input Impedance Matching Stage

Fig. 2 shows the schematic of the push-pull inverter in the first stage. The push-pull inverter can provide gain based on the common source configurations, M1 and M4. Compared to a common-source amplifier under the same biasing current condition, the push-pull inverter has achieved both low noise figure and high transconductance. The transconductance of the push-pull inverter can be achieved both low noise figure and high transconductance.

where \( g_{m1}, K_m, \) and \( W_n \) are device parameters of \( M_2, g_{mp}, K_p, \) and \( W_p \) are device parameters of \( M_1 \). \( \xi \) is the efficiency factor of the push-pull inverter. It can be seen that the efficiency is larger than one for fixed values of \( g_{m1} / I_D \) and \( W_n \). When \( W_p = W_n K_m / K_p \), the efficiency factor is equivalent to 2 which means that \( g_{m1} \) of the push-pull inverter is larger than that of a common-source amplifier [8]-[11].

The simplified model of the push-pull inverter can be viewed as a feedback resistor. Hence, the gain and the input impedance are expressed as follows:

\[
A_i = \frac{V_{out}}{V_{in}} = 1 - (g_{m1} + g_{mp}) R_s \quad Z_m = \frac{v_{in}}{I_{in}} = \frac{1}{g_{m1} + g_{mp}}
\]

where \( L_1, L_2 \) and \( C_1 \) need to be adjusted accordingly so as to provide the imaginary part resonance of the input impedance over the full operation band.

B. Single-to-Differential Stage

The second stage of STDLNA is implemented by using a CS-CG configuration. Fig. 3(a) shows a single common source amplifier (M1) as in Fig. 1. The output port of the push-pull inverter is connected to the gate terminal of \( M_1 \) as the input port and the drain terminal as the output of the second stage. The common source configuration has input and output characteristics of a differential phase. The small signal equivalent circuit is shown in Fig. 3(b). The gain of \( M_1 \) can be expressed as follows:

\[
A_i = \frac{V_{out}}{V_{in}} = -g_m \times (R_D / r_s) = g_m \times (R_D / r_s)
\]

As depicted in Fig. 3(c), the common gate amplifier (M4) has the source terminal as the input port and the drain terminal as the output port. The common gate configuration has input and output characteristics of the same phase. The small signal equivalent circuit is shown in Fig. 3(d). The gain of \( M_4 \) can be expressed as follows:

\[
A_i = \frac{V_{out}}{V_{in}} = -g_m \times v_{gs} \times R_D = g_m \times R_D
\]

From (3), (4), CS and CG are proved to have the output signals with phase difference of 180 degree. Therefore, such configuration can be used as a single-to-differential stage.

C. Output Buffer and Output Impedance Matching

Fig. 4 shows the buffer stage, \( M_5 \) and \( M_6 \) for the output signals from the single-to-differential stage. The output impedance matching can obtain higher gain and better isolation between output and input port. On the other hand, the feedback resistors, \( R_6 \) and \( R_7 \), are able to improve the linearity of STDLNA efficiently. The output matching network employs passive components. Traditionally, using source follower as output buffers needs two current paths for output matching which will result in more power consumption [12], [13]. Therefore, the use of passive components (\( C_5, C_6, R_8, \) and \( R_9 \)) for output impedance matching is a good choice for low power design.
III. EM SIMULATION RESULTS

The proposed single-to-differential low noise amplifier is simulated and fabricated with tsmc CMOS 0.18m process parameters with 1.3V supply voltage. The component values of the STDLNA are listed in Table I. The proposed STDLNA is operated within 3.1-to-5GHz of lower band in ultra-wideband systems. A chip area of 1.29x1.09mm² including I/O pads is occupied. The proposed STDLNA was simulated under a typical-typical corner by Agilent Momentum simulation tool. Both prelayout simulation and EM simulation results are provided.

As depicted in Fig. 5, the maximum power gains of S21 and S31 are 13.44dB and 13.47dB, respectively. The input and output reflection coefficients, S11, S22, and S33, are all less than -10dB as show in Fig. 6(a) and Fig. 6(b). As shown in Fig. 7, the minimum noise figures NF2 and NF3 are 3.46dB and 3.37dB, respectively. The input-referred third-order intercept point (IIP3) is -8dB as shown in Fig. 8.

<table>
<thead>
<tr>
<th>TABLE I. TYPE SIZES FOR CAMERA-READY PAPERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
</tr>
<tr>
<td>M2</td>
</tr>
<tr>
<td>M3</td>
</tr>
<tr>
<td>M4</td>
</tr>
<tr>
<td>M5</td>
</tr>
<tr>
<td>M6</td>
</tr>
<tr>
<td>M7</td>
</tr>
<tr>
<td>L1</td>
</tr>
<tr>
<td>L2</td>
</tr>
<tr>
<td>L3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE II. PERFORMANCE COMPARISON OF VARIOUS SINGLE-TO-DIFFERENTIAL LOW NOISE AMPLIFIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref.</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>This work</td>
</tr>
<tr>
<td>[8] 2012</td>
</tr>
<tr>
<td>[11] 2014</td>
</tr>
<tr>
<td>[14] 2015</td>
</tr>
</tbody>
</table>
As shown in Fig. 9, the EM simulation results show that the proposed STDLNA obtains the gain imbalance and the phase imbalance of ±0.3dB and ±2.97°, respectively. The total power consumption is 19.53mW.

Figure 9. Gain and phase imbalance of STDLNA.

Figure 10. Chip layout of the proposed STDLNA.

The performances of the proposed wideband STDLNA compared with other LNAs are summarized in Table II. The figure of merit is defined as:

\[
FOM = 10 \times \log \frac{Gain(dB) \times Freq(GHz)}{NF(dB) \times P_{dc}(mW)}
\]  

(5)

IV. CONCLUSION

A single-to-differential low-noise amplifier circuit is presented for wideband system applications. The STDLNA employs a push-pull inverter based on the common-source and common-gate topology as an input stage to lower the noise figure. The EM simulation results demonstrated that the noise figure performance as well as the gain and phase imbalances can be improved by the three-stage STDLNA design. Achieved double-ended output gain and minimum noise figure respectively 13.4dB and 3.37dB.

ACKNOWLEDGMENT

The authors wish to thank the Chip Implementation Center (CIC) of the NARL, Taiwan, for supporting the TSMC CMOS process, the chip implementation, and the further measurement. This work was supported by Ministry of Science and Technology, Taiwan, under the Grants NSC102-2221-E-259-033 and MOST103-2221-E-259-045.

REFERENCES


Ren-Yuan Huang received the B.S. degree in electrical engineering from National Ilan University, Ilan, Taiwan, in 2010, the M.S. degree in electrical engineering from National Dong Hwa University, Hualien, Taiwan, in 2013. He is now working toward the Ph.D. degree in electrical engineering from National Dong Hwa University, Hualien, Taiwan. His research interests include analog and RF circuits.