Abstract—A highly linear, low voltage, low power, Low Noise Amplifier (LNA) using a novel nonlinearity cancellation technique is presented in this paper. Parallel Inductor (PI) matching is used to improve LNA gain by 3dB at the desired frequency. The linear LNA was designed and simulated in a TSMC 0.18μm CMOS process at 5GHz frequency. By employing the proposed technique, the IIP, is improved by 12dB in contrast to the conventional folded cascode LNA, reaching -1dBm without having any significant effect on the other LNA parameters such as gain, NF and also power consumption. The proposed LNA also improves without paying attention to the NF parameter.

The cascode structure is extensively used in the LNA design; however, it is not suitable for low voltage applications due to its stacking configuration. Since, with the NMOS stacking architecture of the common-source and common gate transistors, relatively large bias voltage is required for transistor biasing, and the performance degrades significantly as the supply voltage decreases. For low-voltage applications, a folded topology is one of the popular structures. As shown in Fig. 1(a), a folded cascode topology, instead of a stacking cascode topology, is adopted to reduce the supply voltage.

Although source inductive degeneration is one of the popular methods for input impedance matching, it leads to reducing the LNA gain. Therefore, more power should be consumed to compensate the missing gain. In order to increase the power gain, a new input impedance matching called Parallel Inductor (PI) was presented in details by the author in [1]. The source inductor has been removed and the parasitic gate resistance can be converted to 50Ω by a simple LC matching circuit network.

Considering Fig. 1(a), the input impedance of the LNA can be expressed as [1]:

\[ Z_{in} = \left(\frac{\omega L_p}{\omega R_p}\right)^2 + j(\omega L_p - 1/(\omega C_s)) \]

where \( R_p = 1/(R_{out}(\omega C_g)^2) \) and \( C_g \) and \( R_{out} \) are gate source capacitance and parasitic input resistance of MOSFET, respectively. In addition, \( L_p \) is the inductance which is seen by \( C_s \) when looking towards the LNA. Therefore, when the input of the LNA is matched, one obtains \( (\omega L_p)^2/R_p=50 \) and \( \omega C_p=1/(\omega C_s) \), which yields:

\[ C_s = C_p \sqrt{\frac{R_{out}}{50}} \]

\[ L_p = \frac{1}{\omega^2 C_p (1 + \sqrt{\frac{R_{out}}{50}})} \]

Index Terms—First Low Noise Amplifier (LNA), folded cascade, high linear, low power, low voltage, current reuse

I. INTRODUCTION

The increasing demands upon portable wireless devices have motivated the development of CMOS Radio Frequency Integrated Circuits (RFIC). These devices require low power dissipation to maximize battery lifetime. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at low supply voltage with a small battery or environment energy, thus the power and supply voltage constringtion is a crucial issue for these designs [1].

On the other hand, due to the possible large interference signals at the output of a Low-Noise Amplifier (LNA), the LNA has to provide high linearity to prevent the intermodulation tones created by the interference signal from corrupting the carrier signal. This linearity improvement should not be at the cost of gain or Noise Figure (NF). This requires the use of linearization techniques implemented with minimal current overhead. In order to improve the linearity of LNAs, several linearization techniques have been proposed recently [2]. In [3], [4], the linearity factor was improved without paying attention to the NF parameter. In [5], linearity was dramatically enhanced, but the presented topology requires a high supply voltage and consumes more power. In this paper, a new implementation of the linearization technique which is recommended for low voltage and low power LNAs is proposed while gain and NF are maintained approximately constant.

II. CIRCUIT DESCRIPTION

The cascode structure is extensively used in the LNA due to its stacking configuration. Since, with the NMOS stacking architecture of the common-source and common gate transistors, relatively large bias voltage is required for transistor biasing, and the performance degrades significantly as the supply voltage decreases. For low-voltage applications, a folded topology is one of the popular structures. As shown in Fig. 1(a), a folded cascode topology, instead of a stacking cascode topology, is adopted to reduce the supply voltage.

Although source inductive degeneration is one of the popular methods for input impedance matching, it leads to reducing the LNA gain. Therefore, more power should be consumed to compensate the missing gain. In order to increase the power gain, a new input impedance matching technique called Parallel Inductor (PI) was presented in details by the author in [1]. The source inductor has been removed and the parasitic gate resistance can be converted to 50Ω by a simple LC matching circuit network.

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\[ C_s = C_p \sqrt{\frac{R_{out}}{50}} \]

\[ L_p = \frac{1}{\omega^2 C_p (1 + \sqrt{\frac{R_{out}}{50}})} \]
Moreover, the effective transconductance of transistor M1 can be calculated as [1]:

\[ G_{e1} = \frac{i_{m1}}{v_{gs}} = \frac{\omega}{50\alpha} \sqrt{\frac{50}{R_{ss}}} \]  

where \( \omega \) is the angular frequency, \( \alpha \) is the transconductance, and \( R_{ss} \) is the source resistance.

Furthermore, as demonstrated in [1], the PI matching technique results in enhancing the LNA gain by 3dB at the desired frequency band while it consumes no extra power.

The schematic of a low voltage low power folded cascode LNA based on the PI matching network is shown in Fig. 1(a). This LNA is designed for 5GHz applications with a low supply voltage. The folding of the common-gate transistor helps extend the cut-off frequency of the common-source transistor. In addition, the parasitic capacitances at the drain node of the common-source transistor (M1) can be easily eliminated by the resonance with the inductance at the supply pin \( L_p \). The elimination or the reduction of this parasitic capacitance helps suppress the noise contribution of the common-gate transistor at the output. A simple L-C network using an on-chip inductor of \( L_0 \) and an on-chip capacitor of \( C_o \) is used to match the output of the LNA.

The drain current of the MOSFETs can be expressed using Taylor series expansion [6]:

\[ i_{ds}(v_{gs}) = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + g_{m4}v_{gs}^4 + g_{m5}v_{gs}^5 \]

where, \( g_{m1} \) is the nth-order drain conductance nonlinearity coefficient, \( g_{m2} \) is the nth-order drain conductance nonlinearity coefficient, and \( V_{gs} \) is the gate-to-source voltage, and \( V_{ds} \) is the drain-to-source voltage. We neglect the cross modulation coefficients (\( g_{md1} \)), which are very low in a typical MOSFET, and the drain conductance nonlinearity coefficient (\( g_{dd} \)), which has a minor effect on IIP3 calculation for simplicity [2], [7]. Consequently, the simplified small signal output current of the proposed LNA, which includes the difference between \( i_{ds1} \) and \( i_{ds2} \), can be written as follows:

\[ i_{out} = (g_{m2} + g_{m3})V_{gs} + (g_{m4} - g_{m5})V_{gs}^2 + (g_{m4} + g_{m5})V_{gs}^3 \]

where \( g_{m2} \) and \( g_{m3} \) show the nth-order drain conductance nonlinearity coefficient of transistor x and y, respectively.

According to (6), it can be shown that the amplifier’s total trans-conductance increases; the IM2 term decreases, as \( g_{m2} \) and \( g_{m3} \) have the same sign; and the IM3 term decreases, because \( g_{m4} \) and \( g_{m5} \) could have different signs. By properly choosing the circuit parameters such as the transistors’ aspect ratio and the biasing voltage, \( V_b \), the optimum criteria could be achieved, where \( g_{m2} = g_{m3} \) and \( g_{m4} = g_{m5} \), and therefore:

\[ i_{sw} = (g_{m2} + g_{m3})V_{gs} \]

As can be clearly seen from (7), the output current of the proposed LNA is proportional with the first order transconductance of the transistors M2 and M3. Furthermore, the second and third order transconductance nonlinearity coefficients of the transistors M2 and M3 are cancelled.

The elimination of the IM3 components generated by the main amplifier causing high linear characteristic of conventional folded cascode. Therefore, the output current is obtained from the difference between the drain currents of M2 and M3. The aspect ratio, the bias voltage, and the value of L2 associated with the auxiliary transistor are chosen to tune the magnitude and phase of M3 3rd order intermodulation component, IM3, cancelling the IM3 components generated by the main amplifier causing high linear characteristic of conventional folded cascode. C1 and C2 are the coupling capacitors that are both chosen as 5pF to get low impedance at 5GHz. Since the auxiliary transistor (M3) is added in the second stage of the amplifier, it has a negligible effect on the amplifier’s noise figure. Moreover, it does not also dissipate any extra power because of the bias current reusing via M3.

One of the important parameters that should be considered in the design of the LNA is linearity. The linearity of a low voltage low power LNA is generally degraded by other design limitations, thus linearity improvement techniques should be applied to enhance the linearity. The main source of nonlinearity of origin in a MOS transistor is the nonlinear transconductance \( g_{mX} \) which converts the linear input voltage to nonlinear output drain current. As can be seen from Fig. 1(b), a feed forward structure by adding an NMOS transistor (M3) and inductor L2 is utilized in contrast to the conventional folded cascode. Therefore, the output current is obtained from the difference between the drain currents of M2 and M3.

**Figure 1.** (a) Conventional folded cascode LNA with PI input matching, (b) proposed folded cascode LNA

and the gate bias voltage of M3. The second and the third orders nonlinear coefficients of MOSFET can be controlled by Vgs. At first, both the second- and the third-order nonlinear currents of M2 are calculated. Since the main transistor, M2, is biased in strong inversion region, its third-order nonlinear coefficient, $g_{m3}$, has positive as well as negative values; therefore, in order to cancel the nonlinearity trend, the lowest value of the third-order nonlinear coefficient of the PMOS transistor must be cancelled by the highest value of the third-order nonlinear coefficient of the NMOS transistor M3; in this case, M3 operates in weak inversion region. Meanwhile, despite the fact that the variation of $g_{m3}+g_{m2}$ is sensitive to $V_{gs}$, that cannot be the main concern since proper bias voltage for transistors have been chosen to satisfy in this condition. The most significant nonlinearity effects of transistors results from the third order nonlinear coefficient, thus it is necessary to confirm its cancelation. As can be clearly seen from Fig. 2(a), there is a boundary around Vgs of 0.5V where the third-order nonlinear coefficients in the PMOS and the NMOS devices have the same amplitude but different signs. As a consequence, $g_{m3}$ of the transistors can be easily compensated. Furthermore, whilst the second order nonlinear coefficient of the PMOS transistor is negative, the coefficients positive for the NMOS transistor. Accordingly, the second order nonlinear coefficient of the transistors can be simultaneously cancelled by choosing a specific bias voltage and also determining the size of M3. As shown in Fig. 2(b), considering the bias voltage of 0.5V for M3, the second order nonlinearity coefficient becomes zero. In this case, the best performance of linearity can be achieved. Meanwhile, since the second order nonlinear coefficient does not play crucial role in the linearity as much as the third order nonlinear coefficient [2]; therefore, there is no concern about its variation. Moreover, to determine the best size for M3, the IIP3 is swept versus the number of finger for M3. As shown in Fig. 3, choosing the number of fingers as 18 for M3 results in achieving the highest value of IIP3. In this case, the width of M3 is considered to be 8μm.

Finally, it is worth mentioning that unconditional stability refers to the situation where the amplifier remains stable throughout the entire domain of the Smith Chart at the selected frequency and the bias conditions. The conditions can be expressed in terms of the stability or Rollett factor K [8]:

$$K = \frac{1 + |\Delta| - |S_{11}| - |S_{22}|}{2|S_{12}|} > 1$$

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$. If the input and the output are matched well to the source and the load impedances, the values of $S_{11}$ and $S_{22}$ are approximated to zero. From (8), $1+|\Delta|$ is obviously more than 1. If the input and output do not match sufficiently, decreasing reverse isolation ($S_{12}$) will enhance the stability factor. Since $S_{12}$ is in the denominator of (8) and it plays crucial role. In this work, input and output are matched sufficiently and their values are -9dB and -12dB at desired frequency, respectively. Since the contribution of forward power gain is much less than the reverse isolation in stability; therefore, decreasing $S_{12}$ results in enhancing stability factor. In this case, $S_{12}$ is -25dB whereas $S_{22}$ is 12.35dB.

III. SIMULATION RESULTS AND DISCUSSION

The proposed LNA has been simulated by Advanced Design System (ADS) simulator using 0.18μm CMOS process BSIM3 model parameters. In this circuit, passive elements such as Cs and $L_p$ are chosen to satisfy input impedance matching. Having allocated a specific power budget for the LNA, the total current can be calculated, and since M1 plays a crucial role in having a high gain as well as a low noise figure, it has more current compared to that of M2. Considering the amount of current of M1, the size of M1 can be easily determined, and also the values of the parasitic capacitance and the gate resistance of M1 are known. Next, based on (2) and (3), Cs and $L_p$ can be calculated. Furthermore, to determine the value of $L_p$, it is worth mentioning that it should be resonated by total parasitic capacitance at drain of M1, such as drain to gate capacitance of M1, and also gate to source capacitance of M2 at the desired frequency. Moreover, the LNA output should be matched to 50Ω impedance; therefore, a simple LC network is chosen for this purpose.

Figure 2. (a) Third order nonlinear coefficient. (b) Second order nonlinear coefficient

Figure 3. IIP3 versus number of finger of transistor M3
The folded cascode structures used in the design of these circuits are studied, with the width of the transistors M₁ and M₂ equal to 80μm and 160μm, respectively. To reduce the gate resistance, the multi-finger configuration is employed to implement these devices, in which the width and the length of each finger are 8μm and 0.18μm, respectively. Considering the schematic of the proposed LNA (Fig. 1(b)), \( |V_{gs}| \) for M₁ and M₂ are equal to \( V_{dd} (0.6V) \) and since \( V_{th} \) is almost 0.52V in 180nm CMOS, M₁ and M₂ can be easily turned on, whereas \( |V_{gs}| \) for M₃ is equal to \( V_b \) and it is chosen smaller than \( V_{th} \) which results in not operating in saturation region. Since the [Vds] for M₁ is Vdd; therefore, M₁ can be obviously operated in strong inversion region. Additionally, although M₂ and M₃ are stacked, the paths of gate to source voltage for biasing of these transistors are separated from each other and the only dependence is \( |V_{ds2}|+V_{ds3}=V_{dd} \). Furthermore, the worst condition for keeping M₂ in saturation region is to satisfy the following equation;

\[
|V_{ds2}|>|V_{gs2}|-V_{th} \quad \text{or} \quad V_{dd}-V_{th}.
\]

Since the \( V_{dd} \) is 0.6V and \( V_{th} \) in 0.18um CMOS is almost 0.52V, by increasing size of M₂, its \( V_{dd} \) can be decreased, considering at least 100mV for \( V_{ds2} \), M₂ would be in saturation region and in this case, \( |V_{ds3}| \) is 500mV and since \( V_{gs3} \) has been chosen less than \( V_{th} \) consequently M₃ operate in weak inversion region. The size of M₂ and M₃ are properly chosen to. Therefore, M₁ set \( |V_{ds2}|=V_{ds3}=300mV \) and in all corner cases would maintain their regions and M₂ operate in strong inversion region, whereas M₃ acts in weak inversion region. M₁ plays an important role in this design as it is required to operate in strong inversion region to achieve high gain as well as maintain low noise performance. As discussed in the paper, in order to improve the linearity, M₃ should be biased in weak inversion region, and by choosing its gate voltage lower than \( V_{th} \) there should be no other concerns about it. The LNA operates with a 0.6V power supply and consumes 1.28mW of DC power. Fig. 4 shows the IIP₃ of the LNA before and after linearization. The IM₃ of the LNA was simulated by two input tones with 10MHz offset. It can be verified that the value of IIP₃ is improved by more than 12dB reaching -1dBm. The simulated S₂₁ and NF performances of the LNAs are plotted in Fig. 5 and Fig. 6, respectively. Fig. 7 depicts the simulation results of S11 and S22 for the proposed LNA. Fig. 8 shows the K factor in the desired frequency whose value is more than 4 which guarantees the stability of the circuit. At 5GHz, the linear LNA has Noise Figure (NF) of 3.5dB, voltage gain of 12.25dB, input return loss of -12dB, and the output return loss of -9dB. The return loss, S₁₂, is less than -25dB over the bandwidth. By taking consideration into the account, the circuit parameters of proposed folded cascode LNA are tabulated in Table I.

To evaluate the performance of an ultra low voltage LNAs, different Figures of Merit (FOMs) are commonly used in the literature such as follow [9]:

\[
FOM = \frac{\text{gain}(abs).\text{IIP₃}(mw)}{(\text{NF} - 1)(abs).\text{power}(mw)} \quad (9)
\]
A new linearization technique was presented in this paper which is recommended for low voltage LNAs. Due to the reusing of DC current, the proposed method does not consume extra power. According to simulation results, the proposed technique improves IIP3 more than 12dB without any significant effect on the other parameters such as NF, voltage gain and power dissipation. The gain and NF of the proposed LNA are 12.25dB and 3.5dB, respectively. Employing the folded cascode configuration, the fully integrated LNA can operate with small supply voltage of 0.6V while consuming only 1.28mW of power. The simulation results show that the proposed LNA is suitable for ultra low power and ultra low voltage applications.

**TABLE II. COMPARISON RESULTS WITH OTHER PUBLISHED PAPERS, IN F0=5GHz**

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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech (μm)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.4</td>
<td>1.5</td>
</tr>
<tr>
<td>Power(mW)</td>
<td>1.28</td>
<td>1.3</td>
<td>1.3</td>
<td>0.9</td>
<td>0.8</td>
<td>1.68</td>
<td>1.03</td>
<td>12</td>
</tr>
<tr>
<td>NF(dB)</td>
<td>3.5</td>
<td>3.5</td>
<td>3.2</td>
<td>4</td>
<td>4.5</td>
<td>3.7</td>
<td>4.1</td>
<td>3.5</td>
</tr>
<tr>
<td>S₁₁(dB)</td>
<td>12.25</td>
<td>12.7</td>
<td>15</td>
<td>9.5</td>
<td>9.2</td>
<td>11.2</td>
<td>10.23</td>
<td>14.1</td>
</tr>
<tr>
<td>S₂₂(dB)</td>
<td>-12</td>
<td>-9</td>
<td>-8</td>
<td>-15</td>
<td>-15</td>
<td>-18</td>
<td>-17.9</td>
<td>-17</td>
</tr>
<tr>
<td>S₃₃(dB)</td>
<td>-9</td>
<td>-13</td>
<td>-12</td>
<td>-20</td>
<td>-21</td>
<td>-21</td>
<td>-10.6</td>
<td>-17</td>
</tr>
<tr>
<td>FOM</td>
<td>1.42</td>
<td>0.093</td>
<td>0.067</td>
<td>0.042</td>
<td>0.036</td>
<td>0.043</td>
<td>0.063</td>
<td>0.033</td>
</tr>
<tr>
<td>IIP₃(dBm)</td>
<td>-1</td>
<td>-13</td>
<td>-15.9</td>
<td>-16</td>
<td>-16</td>
<td>-17.5</td>
<td>-15</td>
<td>-17.1</td>
</tr>
<tr>
<td>Body biasing</td>
<td>Not used</td>
<td>Not used</td>
<td>Not used</td>
<td>Not used</td>
<td>Not used</td>
<td>Used</td>
<td>Used</td>
<td>Used</td>
</tr>
<tr>
<td>S/M*</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>M</td>
<td>S</td>
<td>M</td>
<td>S</td>
</tr>
</tbody>
</table>

*Simulation/Measurement Results

**IV. CONCLUSION**

It is unfair to compare the simulation results with the experimental results. However, in this work our simulation results have been compared with the simulation results reported in the cited works, and also their measurement results have been added too. Table II represents the summary of the simulation results and comparison with other published papers. The results prove that the proposed technique for linearization of the folded cascode LNA is very efficient because, NF, gain and also power dissipation that are the most important parameters of LNAs have the same value compared to the conventional folded cascode.

**REFERENCES**


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