Nano Scale Low Power Amplifier Using Cascode and Cascade Nutrilization in 45nm CMOS

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Abstract—A low voltage power amplifier mastered by nanoscale CMOS technology has been designed for communication technology and simulated using cadence tool. Basically working of amplifier comprises of boosting up the input to produce a larger version at the output of the devices. An input signal is basically small i.e. a few millivolts to a few microvolt. The main factors concerning small signal amplifier are normally linearity of amplification and magnitude of the output signal, since the value of voltage and current are small in a small-signal amplifier, the amount of power-bearing capacity and efficiency factor are not of much consideration. An amplifier produces greater amount of voltage at the output terminal with reference to the input signal. Large-signal amplifiers, on the side basically offer enough power to the output terminal of power handling device, ranging from few watts to some nano watt. An important function of a large-signal amplifier is the power efficiency of circuit i.e. the maximum amount of power bearing capacity of the circuit, and the impedance of the output device. It is a small dimensional circuit due to the use of nanoscale technology topologies. Basically the circuit has been designed by using feed-back mechanism of two stage amplifier, first is the differential amplifier which helps in differently amplifying the signal between its two inputs and the other is the common drain amplifier that helps in producing low power to this power amplifier. The circuit has been designed using 45nm technology. The main objective of the circuit is to produce circuit as minimize as possible in nanoscale or nanometres to produce circuit parameters best suited for latest miniature technology.

Index Terms—VLSI devices, nanoscale technology, CMOS technology, cascade amplifier, cascode amplifier, slew rate

I. INTRODUCTION

With the advent of technology new electronic devices with precise parameters and increased future output are designed. The technology lays more emphasis on physical parameters of the devices to reduce the size of device as much as possible. For achieving these objectives we rely on VLSI technology plays a vital role & it has been regarded as the future of electronic devices. For decreasing the physical parameters of devices, nano-technology is used especially for communication devices today. This technology deals with reduction of the dimensions in the smallest size in nano-meters or less, creating miniature circuits or devices which are standard dimension tools that are used to manufacture devices and simple structure. Theoretically 1 nanometre is equal to a billion of a meter ($e^{-10}m$). This technology includes all of nano-technology except molecular manufacturing that uses nano-scale to build devices structures, and system in a molecular level [1]. Nano-scale technology was so designed to build devices called nano-electronic devices that include carbon, nano-wires, nano-tubes molecular electronic devices, single-electron devices, resonant tunnelling diodes and QCA such as Field-Effect Transistors (FETs), diodes and molecular and mechanical switches. The experimental of nano-scale devices can prove non-volatile devices which maintain the states in a few molecules [2]. This technology is the latest one to fabricate integrated circuits. The dimension of device has been applied consistently with many generations of technology are in the nanometre scale that are suitable to design smaller devices [3]. The CMOS technology prefers high frequency operation and high integration [4].

A. Power Amplifier

The power amplifier seems to be leading the output voltage power with respect to the input supply given. The two stage power amplifier was designed in this current technology and results are noted below.

CMOS power amplifier is a type of power amplifier designed by using CMOS transistors connected together and get the output gain of amplifier [5]. The basic circuit of CMOS power amplifier is displayed in Fig. 1.

![Figure 1. Schematics of CMOS power amplifier](image-url)

In the above figure $V_{in}$ is the applied voltage to the power amplifier having $R_B$, $R_C$, & $R_E$ being the base, collector and emitter resistance to the transistor $Q_1$. 
B. Differential Amplifier

The power amplifier seems to be leading to configurations which take advantage of a common source type output stage in order to achieve higher load current capability along with a higher output swing as mentioned in reference. Differential amplifier is used to amplify the difference between signals at its two inputs port. It consists of two nMOS Transistor one current and voltage source and two resistance circuits. It is very easy to design a specific gain because the input impedance of amplifier is very high [6]. Basic structure of the differential amplifier is depicted in Fig. 2. Where \( Q_1, Q_2 \) are two transistors having \( V_{\text{out}} \) as the output voltage and \( R_1 \& R_2 \) are the resistance.

\[
I_{D1} = \frac{K_n}{2} (V_C - V_X - V_{T1})^2 \quad (1)
\]
\[
I_{D2} = \frac{K_n}{2} (V_C - V_X - V_{T2})^2 \quad (2)
\]

Small signal analysis of the circuit yields of the differential gain of this circuit is:

\[
\frac{\partial (V_{\text{out}})}{\partial (V_C - V_X)} = - R \cdot g_m \quad (3)
\]
\[
g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{k_n T \frac{I_D}{R}} \quad (4)
\]

The differential output of the amplifier can be raised sufficiently by using active loads instead of resistors and by using cascode configuration, i.e., an intermediary common gate stage between the common-source transistors and the load transistors. Finally, the differential output of the cascode stage must be converted into single-ended output, by using a level-shifter and buffer stage.

C. Common Drain Amplifier

The schematics of the common drain amplifier has been shown in the Fig. 3. It consist of a voltage source, current source a transistor and voltage out. Common drain amplifier or source-follower amplifier uses a field-effect transistor. The input signal is ejected between gate port and drain. While the output is held between source and drain port [8].

\[
\begin{align*}
V_{\text{in}} & \quad V_{\text{out}} \\
R_1 & \quad R_2
\end{align*}
\]

D. Cascade and Cascode Amplifier

The circuit mainly comprises of two stages of power amplifier circuits Cascade amplifier and Cascade amplifier. Cascade amplifier is a differential two stage amplifier consisting of transistor and conductor amplifier. The basic circuit of cascade is often designed from two transistors as shown in figure below. The structure of cascade amplifier is inter-connected between one acting as common emitter or common source and other as common base or common gate. It comprises of series of amplifier stage interconnected one another amplifier stage in which the output of one amplifier stage is connected to the input of other amplifier stage [10]. It offers low output gain whereas it requires low supply voltage, Cascade amplifier circuit is given in Fig. 4 below.

\[
\begin{align*}
V_{\text{in}} & \quad V_{\text{out}} \\
R_1 & \quad R_2
\end{align*}
\]
Basic circuit is designed from two transistors, one of which acts as a common emitter or common source while the other behaves as a common base or common gate [12], [13]. It proves high output gain and high input impedance but requires low power, two transistors and high supply voltage [14].

II. PROPOSED CIRCUIT

The proposed circuit of the power amplifier is presented in the Fig. 6. It comprises of feedback mechanism. The output of one amplifier is connected to the input of the second amplifier. The circuit is so designed to have basic size as small as possible by connecting various nano-scale based devices. It is basically an arrangement in which output of cascode amplifier is produced connected to the input of cascode amplifier i.e. the overall circuit is followed up by a feedback mechanism.

The circuit comprises of five RF CMOS transistor i.e. 3 NMOS and 2 PMOS transistor namely Modn1, Modn2, Modn3, Modp1, Modp2, load resistor (R), inductor (L), input voltage (Vin), input bias (I), drain voltage (ad) and source voltage (Vs). All the input values to the parameters used in the circuit has been defined by the means of table as under. The dimensions of all the transistors given are taken to be equal in length but the weight of the output transistor Modn3 is taken to be double then that of other transistor, as it has to take the load of the output produce. One Inductor and one Resistor are also used to act as an impedance circuit of respective dimensions. The circuit has been simulated using cadence tool and has a major objective to acquire smaller dimension and power consumption, for this purpose 45 nano meter technology has been used.

Fig. 7 depicted the layout design of the proposed power amplifier in which different connecting layers has been shown side-wise.

TABLE I. DIMENSIONS

<table>
<thead>
<tr>
<th>S. no.</th>
<th>Elements</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modp1,Modp2</td>
<td>0.4um and 5um by length and weight respectively</td>
</tr>
<tr>
<td>2</td>
<td>Modn1,Modn2</td>
<td>0.4um and 5um by length and weight respectively</td>
</tr>
<tr>
<td>3</td>
<td>Modn3</td>
<td>0.4um and 10um by length and weight respectively</td>
</tr>
<tr>
<td>4</td>
<td>Inductor</td>
<td>1uH</td>
</tr>
<tr>
<td>5</td>
<td>Resistor</td>
<td>100 ohms</td>
</tr>
</tbody>
</table>

The simulation values of the circuit parameters taken very precisely has been shown in the Table II.

All the parameters are calculated with great precision using 45nm technology to carry out the simulation process and output has been noted at each point. From the produced result it is concluded that the total power of this amplifier is in micro-watt ranges which is achieved
by having lower delays and targeted performance and feedback mechanism.

Similarly, efficiency of amplifier represents the amount of ac power delivered from the dc source. Efficiency of the amplifier can be calculated as:

\[
\% \eta = \frac{P_o}{P_i} + 100 \% \tag{9}
\]

Slew Rate (SR) is the maximum possible rate of change of the operational amplifier output voltage.

\[
SR = \frac{dv_o}{dt} \text{max} \frac{V}{\mu s} \tag{10}
\]

\[
SR = \frac{l_{\text{max}}}{C} \tag{11}
\]

In a similar manner, the amplifier gain & Common Mode Rejection Ratio (CMRR) of the amplifier can be calculated as:

\[
A_d = \frac{v_o}{v_{id}} = g_m \left( R_D \| r_0 \right) \tag{12}
\]

where, \(A_d\) = differential gain, \(v_o\) = output voltage, \(v_{id}\) = differential input, \(g_m\) = transconductance, \(R_D\) = drain resistance, and \(r_0\) = output resistance.

Common mode gain:

\[
A_{cm1} = A_{cm2} = \frac{v_{o1}}{v_{cm}} = \frac{v_{o2}}{v_{cm}} = - \frac{R_D}{g_m + 2R_{ss}} = - \frac{R_D}{2R_{ss}} \tag{13}
\]

where: \(A_{cm1} = A_{cm2} = \text{common mode gain}\) and \(R_{ss} = \text{source resistance}:

\[
\text{CMRR} = \frac{\text{Differential mode gain}}{\text{Common mode gain}} = \frac{A_d}{A_{cm}} = g_m R_{ss} \tag{14}
\]

IV. CONCLUSION

Power amplifier has been generally used in the electronic circuit for boosting up or strengthening the applied signal, this has been done to obtain high variation in the signal applied. The power amplifier based on 45nm technology has been designed and simulated in this paper, the amplifier output response is compared with the 180nm technology response, and all the result produced is noted down precisely to obtain high accuracy and circuit precision. The simulation results are observed at 1.56GHZ frequency i.e. is the input frequency of the circuit, which is defined as the communication frequency range that is more often used in communicating devices and in technologies. The output voltage obtained is 2.90V at 1.56GHZ frequency. The output power of this amplifier is noted to be 436us at 1.56GHz frequency.

The output response as compare to the 180nm is shown in the Fig. 8 and it has been observed that the leakages are very high in this case.

AC power delivered to the load \(R_C\) may be:

Output power:

\[
P_o = V_{CE} (\text{rms}) I_C (\text{rms}) \tag{6}
\]

\[
P_o = I_C^2 (\text{rms}) R_C \tag{7}
\]

\[
P_o = \frac{V_C^2 (\text{rms})}{R_C} \tag{8}
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\]
reducing the circuit efficiency has also reduced effectively.

Figure 9. Output response of power amplifier simulated at 45nm technology

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[7] Differential Transistor Amplifier, the Creative Commons Attribution License, Version 1.0, Stanford, California 94305, USA.


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