

# Two Phase, Three Legs Inverter with Z-Source Input Impedance

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**Abstract**—This paper is talking about two phase inverter, three legs with Z-source input impedance. At first showing two phase inverter two legs and its operation modes using Sine Pulse Width Modulation SPWM. After that connection of two phase inverter circuit with three legs, and switches operation modes using (SPWM). In section four, Z-source input impedance, method of introducing Z-source input impedance onto two phase inverter, two legs, and onto two phase inverter circuit, with three legs. The method of how to get shoot-through states and use them to raise the voltage output of the inverter. Finally simulation results.

**Index Terms**—z-source, shoot- through, SPWM, transistor, switches

## I. INTRODUCTION

The two phase inverter is used to drive the two phase induction motors that was supplied in past from four wires networks of two phases source. In the industrial and residential applications, that is very cost to use three phase induction machines because of high cost of their power electronic circuits. Today, two phase drives are developed and produced in low cost [1]. One of these new drives is two phase inverter with  $(90^\circ)$  between each phase with three legs and two legs circuit and Z-source property investment to raise the voltage output of the inverter. Selection of switches for example (transistors, mosfet's, IGBT) that will derive the inverter circuit is very important, and selection of modulation type, for example (SPWM) or space vector pulse width modulation (SVPWM) is very important for the building the inverter circuit that will be used for driving, because it will specify the output shape of inverter and its value.

## II. TWO PHASE, TWO LEGS INVERTER

The circuit of two phase inverter, two leg is same as single phase inverter (full bridge) circuit. It consists of four switches (S) and the input source ( $V_{in}$ ) as shown in Fig. 1, but, the difference is the choosing of switching operating sequence for each leg. For assuming the switch ( $S_1$ ) is on with time period ( $\pi$ ) from the full period ( $2\pi$ ) and ( $S_3$ ) delays than ( $S_1$ ) by  $(\pi/2)$  as shown in Fig. 2. The switches conduction periods of ( $S_2$ ) and ( $S_4$ ) is reverse to that of ( $S_1$ ) and ( $S_3$ ) respectively. There are Four modes of operation of the circuit as expressed in Fig. 3a-Fig. 3d. In

mode (1) for period  $(0-\pi/2)$ , ( $S_1$ ) and ( $S_3$ ) will be at (1,0) state respectively and ( $S_1$ ) will operate with ( $S_4$ ) at the same time [2]. The two phases will be in parallel to each source,  $(+V_{dc})$  will supply the first phase but  $(-V_{dc})$  is supplied to the second phase, equivalent circuit of mode (1) is shown in Fig. 3a.

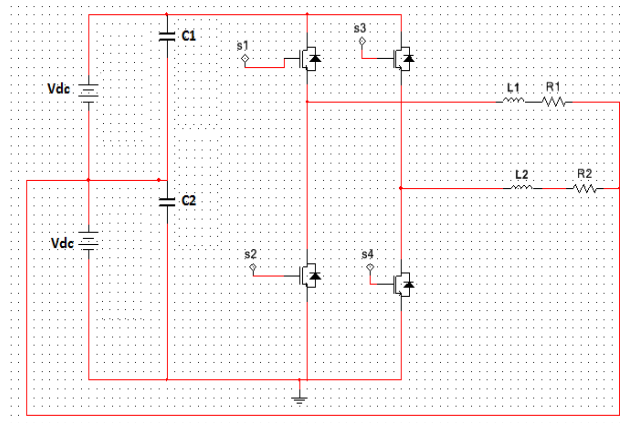


Figure 1. Two phase inverter circuit with two legs.

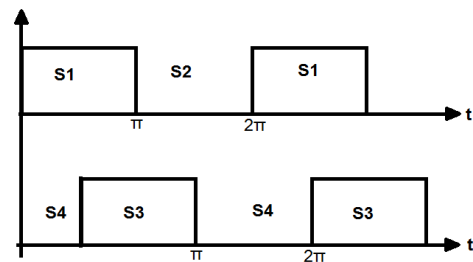


Figure 2. Switching sequence of two phase inverter.

In mode (2) for period  $(\pi/2-\pi)$ , ( $S_1, S_3$ ) will be on (1,1), this means that the terminals of each load of the two phase will be in parallel Connected to the up of input voltage ( $V_{in}$ ), this leads to that the output voltage of phase one ( $PH_{(1)}$ ) equal to the output voltage of phase two ( $PH_{(2)}$ ), ( $V_{PH(1)} = V_{PH(2)} = +V_{dc}$ ), equivalent circuit of mode (2) is shown in Fig. 3b. In mode (3) for period  $(\pi-\pi/2)$ , ( $S_1$ ) and ( $S_3$ ) will be at (0,1) state respectively and the terminals of phase one ( $PH_{(1)}$ ) will be connected to the lower source with reverse polarity and phase two ( $PH_{(2)}$ ) will remain connected to the up of source, ( $V_{PH(1)} = -V_{dc}$ ,  $V_{PH(2)} = +V_{dc}$ ), equivalent circuit of mode (3) is shown in Fig. 3c. The last mode is mode (4), ( $S_1$ ) and ( $S_3$ ) will be off (0,0), this mean ( $V_{PH(1)} = V_{PH(2)} = -V_{dc}$ ) [2]. The equivalent circuit of mode (4) is shown in Fig. 3d, and the

all operation modes of switches and related output voltages of each phase is illustrated in Table I.

TABLE I. MODES OF OPERATION

S1	S3	VPH(1)	VPH(2)	Mode
1	0	+Vdc	- Vdc	1
1	1	+Vdc	+Vdc	2
0	1	- Vdc	+Vdc	3
0	0	- Vdc	-Vdc	4

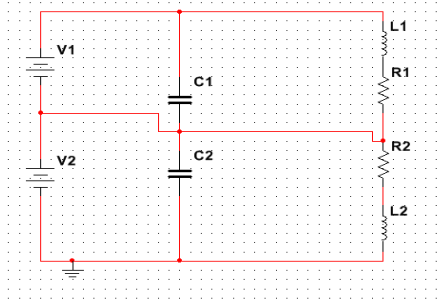


Figure 3a. Two phase, two legs inverter circuit at mode (1).

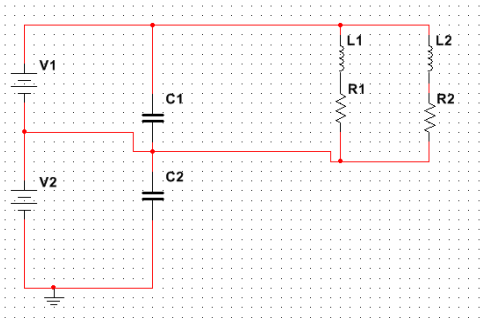


Figure 3b. Two phase, two legs inverter circuit at mode (2).

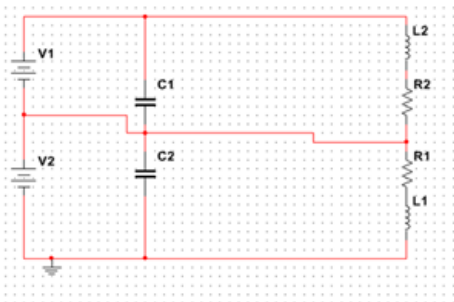


Figure 3c. Two phase, two legs inverter circuit at mode (3).

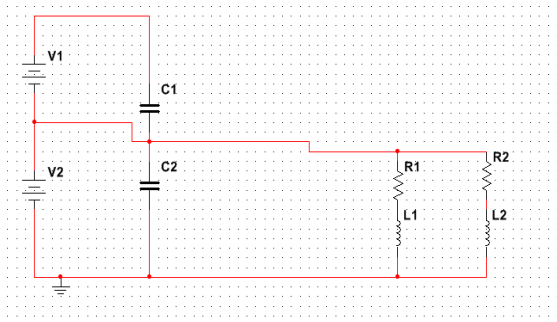


Figure 3d. Two phase, two legs inverter at mode (4).

The period of each mode that illustrated above in Fig. 2, is  $(\pi/2)$ . For the Two phase two legs inverter circuit that illustrated in Fig. 1, the values were  $(V_1=V_2=100\text{v})$ , and  $(C_1=C_2=10\mu\text{F})$ . The two phases load circuit is assumed it is composed from  $(R_1=R_2=3.58\Omega)$ ,  $(L_1=L_2= 0.1\text{mH})$ . The inductive load had chosen to express the behavior of the switches and freewheeling diodes same as in three phase inverter. By using (SPWM), when the two phase control signals are much greater than the carrier signal, the output of the circuit (voltages and currents) was not effected by modulation index (m), [2]. The output of the circuit at this case is as shown in Fig. 4a and Fig. 4b.

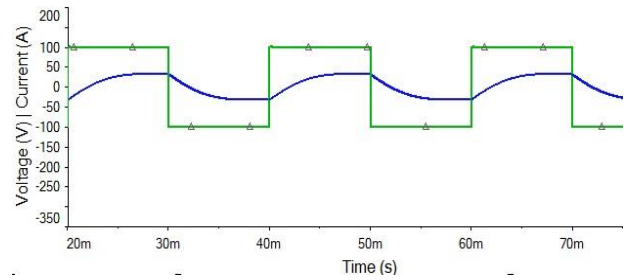


Figure 4a. Output (current and voltage) of phase one.

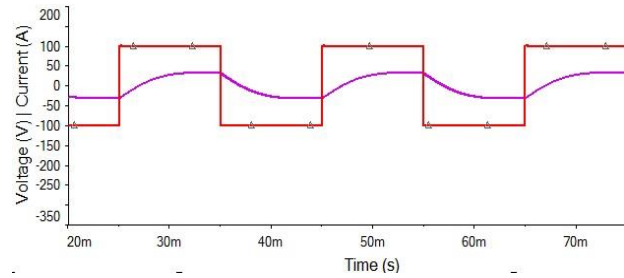


Figure 4b. Output (current and voltage) of phase two.

From above we can notice that the output voltage of each phase with respect to time is " $V_{PH(1)} = 4v_{dc}/\pi \sin\omega t + 4v_{dc}/3\pi \sin 3\omega t + 4v_{dc}/5\pi \sin 5\omega t + 4v_{dc}/7\pi \sin 7\omega t + \dots$ ",  $(V_{dc}=100\text{v})$ . About the phase one  $(PH_{(1)})$  from  $(0-\pi)$  current will flow at  $(D_1, S_1)$  and for the period from  $(\pi-2\pi)$  the current will flow in  $(D_2$  and  $S_2)$ . For the phase two  $(PH_{(2)})$  from  $(\pi/2-3\pi/2)$  current will flow at  $(D_3, S_3)$  and for the period from  $(3\pi/2-5\pi/2)$  the current will flow in  $(D_4$  and  $S_4)$ , this is true when there is no modulation and for any modulation index. For modulation index  $(m=0.5)$ , the output voltage of each phase after filter is half of the fundamental component " $(V_{PH(\text{peak})} = 50\text{v})$ " as expressed in Fig. 5. For modulation index  $(m=1)$  the output voltage of each phase after filter is " $(V_{PH(\text{peak})} = 100\text{v})$ " as expressed in Fig. 6.

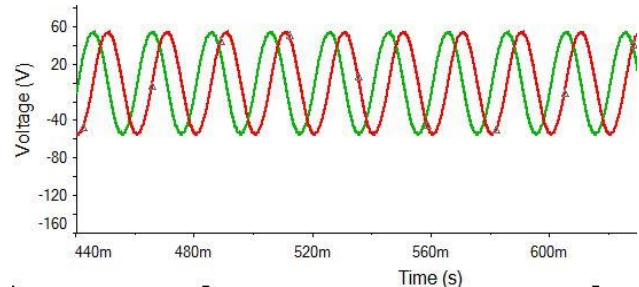
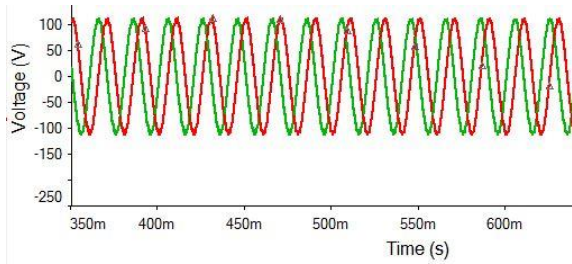


Figure 5. Output of two phase inverter at modulation index  $(m=0.5)$ .


 Figure 6. Output of two phase inverter at modulation index ( $m=1$ ).

### III. TWO PHASE INVERTER CIRCUIT BY ADDING THIRD LEG

In this circuit third leg had added to the previous circuit, this leg represents the neutral leg. For the third leg the control signal is zero voltage was compared with the carrier signal. In this case the control signals for switches ( $S_1$ ) and ( $S_3$ ) and ( $S_5$ ) are as follows:

$$V_{C(S1)} = V_m \sin \omega t$$

$$V_{C(S3)} = V_m \sin(\omega t - 90^\circ)$$

$$V_{C(S5)} = \text{Zero volts.}$$

The circuit of Two phase inverter by adding third leg is shown in Fig. 7. The control signal that compared with carrier signals for ( $S_1$ ,  $S_3$ ,  $S_5$ ) before and after modulation as shown in Fig. 8a-Fig. 8d. In mention the switching pulse voltages of the ( $V_{C(S2)}$ ,  $V_{C(S4)}$ ,  $V_{C(S6)}$ ) are the inverse of the switching pulse voltages of ( $V_{C(S1)}$ ,  $V_{C(S3)}$ ,  $V_{C(S5)}$ ).

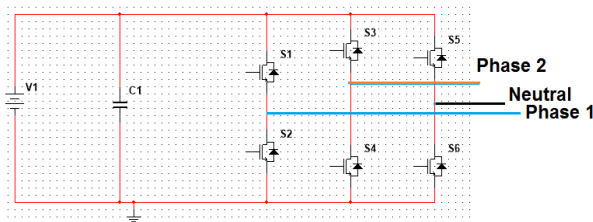


Figure 7. Two phase inverter circuit with third leg.

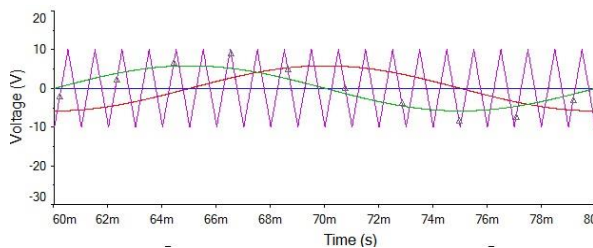
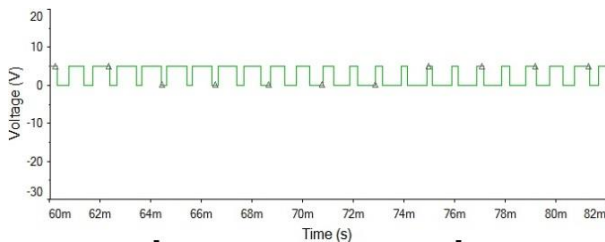
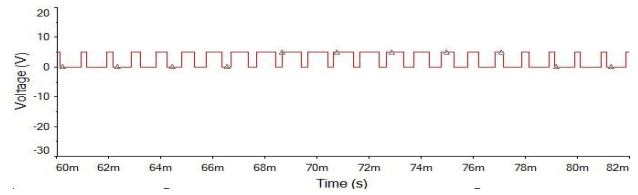
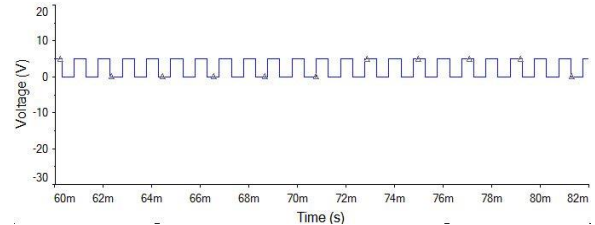


Figure 8a. Control signals and carrier signal two phase, three legs inverter.


 Figure 8b.  $V_{C(S1)}$  after modulation.

 Figure 8c.  $V_{C(S3)}$  after modulation.

 Figure 8d.  $V_{C(S5)}$  after modulation.

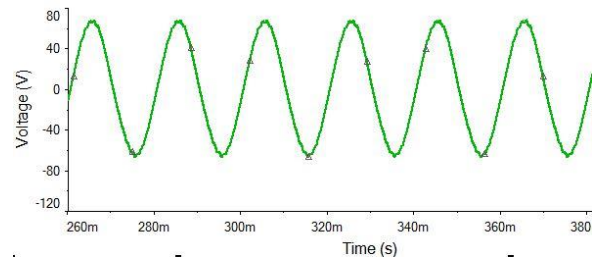
From watching the output voltage for the two phases three legs inverter, it is found eight modes of the output voltage, as shown in the following Table II. Resistive load is used in this circuit, because it is simple in analysis of Z-source components. For the simulation of this circuit input voltage was ( $V_{in}=200\text{V}$ ) and the resistances of the two phase load were equal ( $R_1=R_2=20\Omega$ ), modulation index ( $m=0.6$ ), and carrier frequency = 1kHz.

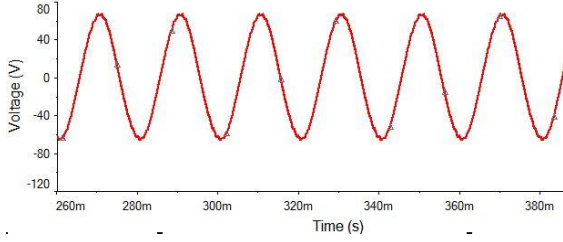
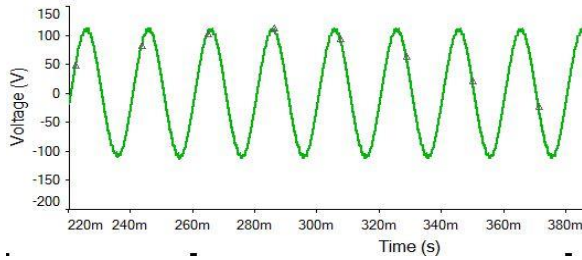
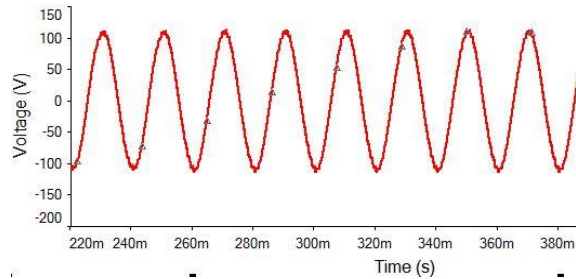
$$V_{ac(peak)} = M * \frac{V_{in}}{2} \quad (1)$$

The output of the circuit of the fundamental component after low pass filter found from equation (a), and was equal to (60V), and for modulation index ( $M=1$ ) was equal to (100V) as shown in Fig. 9a and Fig. 9b and Fig. 10a and Fig. 10b.

TABLE II. MODES OF OPERATION

$S_1$	$S_3$	$S_5$	$V_{PH(1)}$	$V_{PH(2)}$	Mode
0	0	0	0	0	1
1	0	0	$V_{in}$	0	2
1	1	0	$V_{in}$	$V_{in}$	3
0	1	0	0	$V_{in}$	4
0	1	1	$-V_{in}$	0	5
0	0	1	$-V_{in}$	$-V_{in}$	6
1	0	1	0	$-V_{in}$	7
1	1	1	0	0	8


 Figure 9a. Output voltage of phase one at modulation index ( $m=0.6$ ), before and after low pass filter.


 Figure 9b. Output voltage of phase two at modulation index ( $M=0.6$ ), before and after low pass filter.

 Figure 10a. Output voltage of phase one at modulation index ( $m=1$ ), before and after low pass filter.

 Figure 10b. Output voltage of phase two at modulation index ( $m=1$ ), before and after low pass filter.

#### IV. Z-SOURCE INPUT IMPEDANCE

The limitation of (VSI) Voltage source inverter is that the ac output voltage cannot be more than the dc bus voltage. Similarly for (CSI) Current source inverter, the output ac voltage has to be greater than the original dc voltage that feeds the dc inductor, dc voltage produced is always smaller than the ac input voltage. That means the VSI is a buck inverter whereas CSI is a boost inverter. On the other hand in case of these two inverters, the upper and lower devices of each phase leg cannot be turn on simultaneously either by purpose or by EMI noise. If a shoot-through state occurs then these inverters get damaged. There we need to provide dead time in between upper and lower gate pulses for each leg. To avoid these limitations of VSI & CSI, Z-source inverter is introduced [3], [4]. Z-source inverter is much reliable buck-boost capable inverter with impedance network. Z-source inverter is a very recently used inverter. Generally in traditional inverter there are various conventional (PWM) techniques like Sine triangle (PWM), Space Vector (SVPWM) techniques. Likewise in Z-source inverter there are various types of conventional (PWM) techniques used to control Z-source inverter. These techniques are Simple Boost Control (SBC), Maximum Boost Control (MBC), Maximum Boost Control with third harmonic injection. The equivalent circuit of Z-source impedance is as shown

in Fig. 11, the parameters of the z-source circuit in Fig. 11 are symmetrical that's mean ( $V_{C1}=V_{C2}$ ,  $C_1=C_2$ ,  $V_{L1}=V_{L2}$ ,  $L_1=L_2$ ). In two phase, two legs inverter it is very difficult introduce Z-source input impedance onto it, because when the circuit transforms from mode (1) Fig. 12a to mode (2) Fig. 12b the circuit will be suffer from unbalance state. In mode (1) there is no problem in operation in the output voltage of Z-source as shown in Fig. 12a, But in mode (2) the capacitors of Z-source will not charge equally, and the result of this, there is un equality in voltage magnitudes of phase one and phase two Fig. 12b. Because of this reason introducing Z-source input impedance onto two phase inverter three legs is more practical, and more useful. States of imbalances state cannot be seen because of the presence of neutral third leg in the inverter circuit.

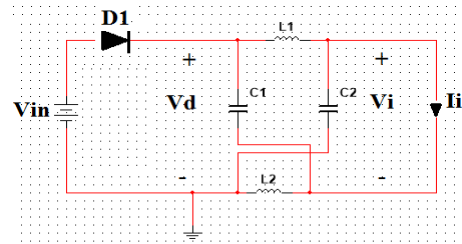


Figure 11. Z-source input impedance circuit.

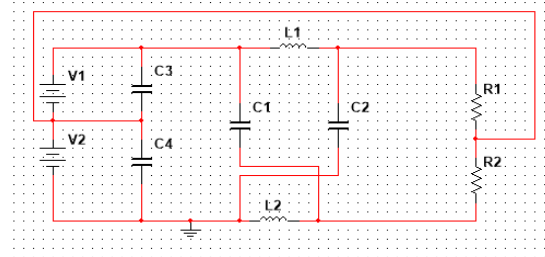


Figure 12a. Two phase two legs inverter at mode (1) in the presence of z-source input impedance circuit.

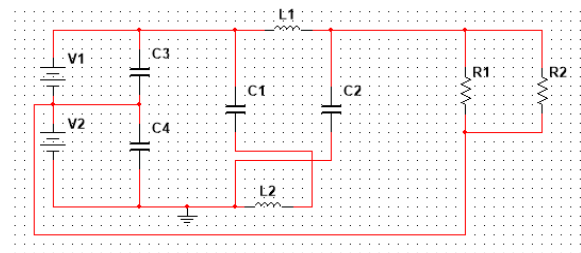


Figure 12b. Two phase, two legs inverter at mode (2) in the presence of z-source input impedance circuit.

When the z-source circuit at shoot through zero state for interval of ( $T_0$ ) that is mean ( $S_1$ ) and ( $S_2$ ) or ( $S_3$ ) and ( $S_4$ ) or ( $S_5$ ) and ( $S_6$ ) are on in the same time. In this case ( $C_1$ ) will be in parallel with ( $L_1$ ) and ( $C_2$ ) will be in parallel with ( $L_2$ ) and  $V_{L1}=V_{C1}$  and  $V_{L2}=V_{C2}=V_C$  and  $V_d=2V_C$ , therefore ( $V_d$ ) will be more than ( $V_{in}$ ) and ( $D_1$ ) will be off, " $V_i = \text{zero volts}$ " [5], [6]. The second state the Z-source circuit will be at any non-shoot through states for an interval of ( $T_1$ ) from the switching cycle ( $T$ ). In this case " $V_L=V_{in}-V_C \dots (1)$ ", " $V_d=V_{in} \dots (2)$ " Fig. 11, that is mean ( $D_1$ ) will be ON, in this case:

$$V_i = V_c - V_L = 2V_c - V_{in} \quad (3)$$



and “ $T=T_1+T_0$ ”. The average voltage of the inductors for the full period (T) should be zero in steady state as shown in “(2)”:

$$V_L = V_{L(average)} = \frac{T_0 \cdot V_c + T_1 \cdot (V_{in} - V_c)}{T} = \text{zero} \quad (4)$$

That is mean:

$$\frac{V_c}{V_{in}} = \frac{T_1}{T_1 - T_0} \quad (5)$$

Similarly the average (D.C) link voltage across the inverter bridge can be found as follows:

$$V_i = V_{i(average)} = \frac{T_0 \cdot 0 + T_1 \cdot (2V_c - V_{in})}{T} = \frac{T_1}{T_1 - T_0} \cdot V_{in} = V_c \quad (6)$$

Similarly the peak (D.C) link voltage across the inverter bridge can be found as follows:

$$V_{i(peak)} = V_c - V_L = 2V_c - V_{in} = 2V_{in} \cdot \frac{T_1}{T_1 - T_0} - V_{in} = V_{in} \cdot \frac{T_1 + T_0}{T_1 - T_0} = V_{in} \cdot \frac{T}{T_1 - T_0} = B \cdot V_{in} \quad (7)$$

$$B = \frac{\frac{T}{T_1 - T_0}}{\frac{T}{T_1 - T_0} - \frac{T_0}{T_1 - T_0}} = \frac{1}{1 - \frac{T_0}{T_1}} \geq 1 \quad (8)$$

(B) is the boost factor from the shoot-through zero state. The output peak phase voltage ( $V_{ac(peak)}$ ) of the inverter can be expressed as:

$$V_{ac(peak)} = m \cdot \frac{V_{i(peak)}}{2} \quad (9)$$

where (m) is the modulation index. Using “(7)” and “(9)”, can be further expressed as:

$$V_{ac(peak)} = m \cdot B \cdot \frac{V_{in}}{2} \quad (10)$$

For the traditional V-source(PWM) inverter “ $V_{ac(peak)} = m \cdot \frac{V_{in}}{2}$ ”, “equation (10)” shows that the output voltage can be stepped up and down by choosing the appropriate buck-boost factor  $B_B$ .

$$B_B = m \cdot B = (0 \sim \text{infinity}) \quad (11)$$

From “(1)” and “(5)” and “(8)”:

$$V_{c1} = V_{c2} = V_c = \frac{\frac{T}{T_1 - T_0} \cdot T_0}{\frac{T}{T_1 - T_0} - \frac{T_0}{T_1 - T_0}} \cdot V_{in} = \frac{1 - \frac{T_0}{T_1}}{1 - \frac{T_0}{T_1}} \cdot V_{in} \quad (12)$$

For finding the values of inductances (L) and capacitance (C) for Z-source circuit for the two phase three legs inverter, there will be an assumption for the load and output voltage of the inverter [7]. The input (D.C) voltage is “ $V_{in}=200\text{v}$ ”, and the assumption for the peak output voltage is “ $V_{ac(peak)}=350\text{v}$ ” for each phase, assume the load is purely resistive load ( $20\Omega$ ), this leads to the peak output current will be “ $I_m=17.5\text{A}$ ”, and modulation frequency “( $F_s=1000\text{Hz}$ )”:

$$T = \frac{1}{F_s} = \frac{1}{1000} = 10^{-3} \quad (13)$$

$$B_B = \frac{2V_{ac(peak)}}{V_{in}} = 2 \cdot \frac{350}{200} = 3.5 \quad (14)$$

$$\frac{T_0}{T} = D_o = \frac{2V_{ac(peak)} - V_{in}}{4V_{ac(peak)} - V_{in}} = \frac{2 \cdot 350 - 200}{4 \cdot 350 - 200} = 0.4166 \quad (15)$$

$$m = 1 - D_o = 1 - 0.4166 = 0.583333 \quad (16)$$

$$V_{i(peak)} = 2V_c - V_{in} = \frac{2V_{ac(peak)}}{1 - D_o} = \frac{2 \cdot 350}{1 - 0.4166} = 1200\text{V} \quad (17)$$

$$I_o = 2V_{ac(peak)} \cdot \frac{I_m}{[2V_{i(peak)} \cdot (1 - D_o)]} = 2 \cdot 350 \cdot \frac{17.5}{[2 \cdot 1200 \cdot (1 - 0.4166)]} = 8.75\text{A} \quad (18)$$

The symbol ( $I_o$ ) represents the Z-source output current. The value of Z-source impedances can be found from (19) as:

$$C = I_o \cdot D_o \cdot \frac{T}{2K_C \cdot V_{in}} = 8.75 \cdot 10^{-3} \cdot \frac{0.41666}{2 \cdot 0.5 \cdot 200} = 182\mu\text{F} \quad (19)$$

$$L = V_{in} \cdot D_o \cdot \frac{T}{2K_L \cdot I_o} = 200 \cdot 0.41666 \cdot \frac{10^{-3}}{2 \cdot 0.1 \cdot 8.75} = 47\text{mH} \quad (20)$$

The final two phase, three legs inverter circuit that these values above were applied to it is as shown in Fig. 13.

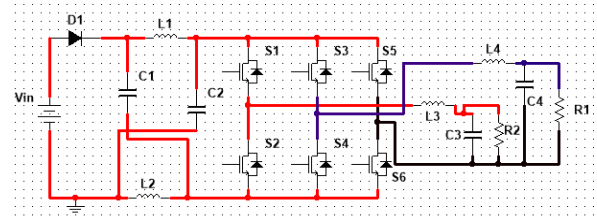


Figure 13. Two phase, three legs inverter with Z-source input impedance circuit.

## V. SIMULATION RESULTS

The last two phase, three legs inverter circuit used with modulation index ( $m=0.583333$ ), depending on the analysis of Z- source components, the resistive load was ( $R=20\Omega$ ), and input voltage ( $V_{in}=200\text{v}$ ). In this circuit the method used for obtaining shoot-through state is simple boost shoot through control (SBC) [8]-[10]. The block diagram for this control method is as shown in Fig. 14. For the traditional circuit, the maximum output voltage for each phase at this modulation index must be “ $V_{ac(peak)}=58.333\text{v}$ ”, as in Section (3) “(1)”. In this simulation the peak voltage for each phase appeared as “ $V_{ac(peak)} = 62\text{v}$ ” as in Fig. 15. Now with using shoot-through zero-state with Z- source circuit as in Fig. 13, with the value of ( $D_o$ ) that obtained from “(15)”, the peak output (A.C) voltage as in “(10)”, will be; “ $V_{ac(peak)}=6 \cdot 0.58333 \cdot 62=372 \text{ v/PH}$ ”. The output voltage obtained from the simulation program is in Fig. 16.

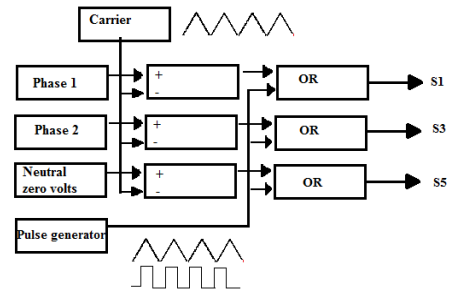


Figure 14. Block diagram of introducing shoot-through onto the two phase, three legs inverter.

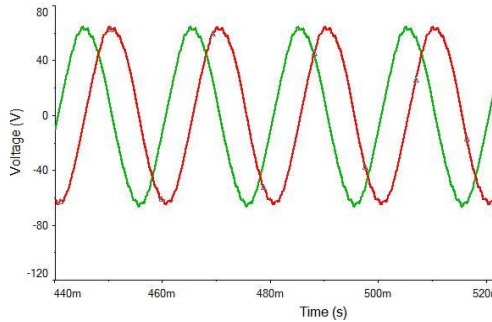


Figure 15. Output voltage of the traditional two phase, three legs inverter without Z-source, at modulation index ( $m=0.58333$ ).

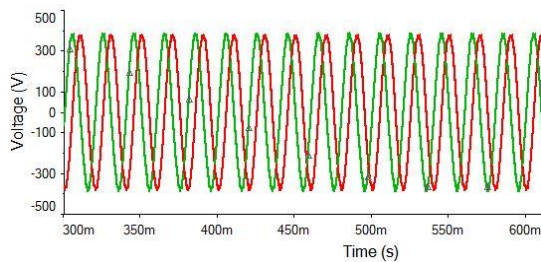


Figure 16. Output voltage of the two phase, three legs inverter after applying shoot-through states, at modulation index ( $m=0.58333$ ).

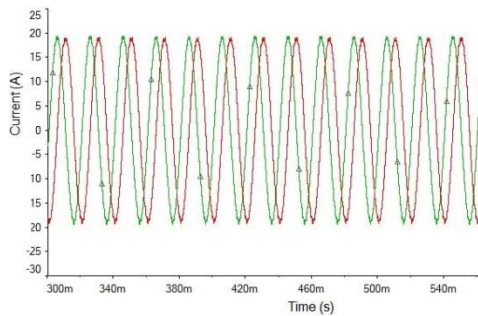


Figure 17. Current waveforms of the two phase, three legs inverter after applying shoot-through states, at modulation index ( $m=0.58333$ ).

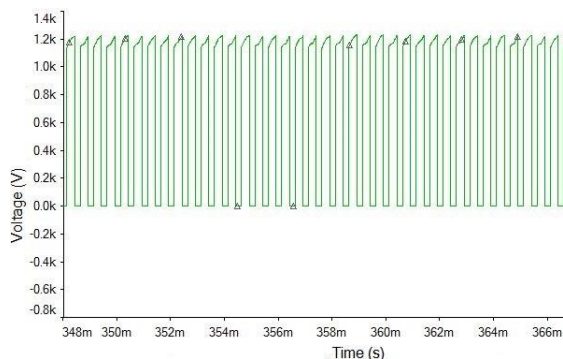


Figure 18. Voltage wave form of ( $V_i$ ) at ( $T_o$ ) and ( $T_i$ ), at modulation index ( $m=0.58333$ ).

The output current of the two phases is as in Fig. 17. The shape of ( $V_i$ ) will be zero at ( $T_o$ ) and at ( $T_i$ ), will be ( $V_i=1400-200=1200v$ ). With initial value at ( $T_o$ ) and increase to maximum final value at ( $T_i$ ). This increasing is the charging of capacitors at shoot-through states, the shape of ( $V_i$ ) is as shown in Fig. 18. The voltage shape of position ( $V_d$ ) will be (200V) at no shot-through state ( $T_i$ ) with forward bias of ( $D_i$ ). When switches of any leg

operate at same time in ( $T_o$ ), every capacitor will be in parallel with every inductor and discharges its charges in the inductor, so the value of ( $V_d$ ) will equal value of ( $2V_c=2*700V=1400V$ ), the shape of the voltage ( $V_d$ ), is as shown in Fig. 19.

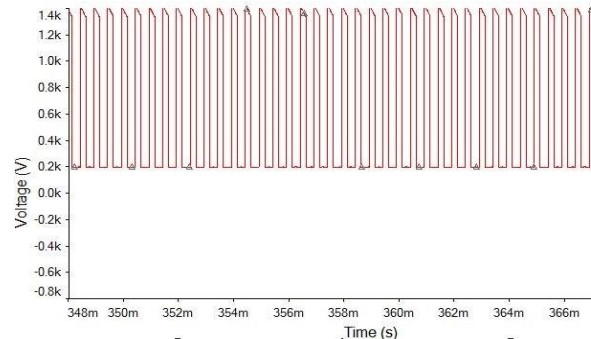


Figure 19. Voltage wave form of ( $V_d$ ), at ( $T_o$ ) and ( $T_i$ ), at modulation index ( $m=0.58333$ ).

## VI. CONCLUSION

This article focused on simple (SPWM) method for two legs, three legs, Z- source, two phase inverter. It depended on the third leg to remain the symmetry of behavior of Z-source components and to divide the input voltage, the zero sequence modulation was made for zero control voltage and compared it with carrier signal. And after that we applied it with Z-source circuit to boost the voltage to the desired value. Before that analysis (LC) components of Z-source is done to obtain good results close to the true values. The two phase inverter is very important because it used to supply two phase induction machines, that have low cost compared with three phase machines and their power electronics drive circuits. The simulation results that was obtained may be contain small errors, but it rationally acceptable. These errors may be because the behavior of components filters, diodes, inductances, switches, or because the simulation technique used in program .Simulation program was Ni-multism 2014 (64-bit). Finally we hope we did the best for this work.

## ACKNOWLEDGMENT

For this work, we present thank for God firstly, and our families, and for everyone in the academic staff that erg us and prepare all conditions to do this work.

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