

ESD with Line Length in TFT-LCD Circuits

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Abstract—In the circuit of semiconductor, ESD usually occurred between two lines which are closed to each other. To study the how to improve the anti-ESD of current design, the test lines for both first gate and last gate are compared. The two test lines go cross over another line but they are different length. The products were exposed to the same rich-static environment to test their anti-ESD ability. Result shows that the longer the line is, the more possibilities of the ESD is, especially when the length difference exceeds 14%. The result would direct the design of the micro circuit by dividing long line into several short-line of semiconductor, which would reduce the probability of ESD.

Index Terms—ESD, test line, microelectronics, TFT-LCD, peripheral circuit

I. INTRODUCTION

As we know, ESD (Electro-Static Discharge) is the most common defect in semiconductor field which has a big effect to the product yield and causes enormous economic loss. The control of electrostatic discharge is an important aspect in the manufacturing, assembling and repairing of devices that employ electronics. Electrostatic discharges can damage an electronic component at any stage of its production or application if not controlled. What is more, manufacture procedure also involve repair, rework, sorting, shipping, labour cost and time consumption. The economic effect is not just a simply diode damage but huge procedure error which cause million dollar cost. Many measures have been taken to avoid ESD. Those methods can be divided into reducing electrostatic charge generation, outlet charge and neutralizing charges. Many actions have been taken to avoid ESD such as optimizing design [1]-[7], removing charges to ground, improve our environment [8]-[12], optimizing design, set ionizer bar, applying low resistance material, decreasing line resistance. Among those methods, design improving is a high cost-efficiency approach. In this paper the design factors which influence ESD are studied.

II. BACKGROUND

Liquid Crystal Display (LCD) is widely used in TV, computer monitor, notepad, pad, mobile, etc. Majority of those LCD are Thin-Film Transistor LCD (TFT-LCD). In the display area of display there are thousands of lines, for instance, a VGA display consists of 640 date lines and

480 gate lines, while XGA consists of 1027 date lines and 768 gate lines. Those lines drive vertically (date line) and horizontally (gate line) to form pixel units. Those gate lines all begin at one side of the panel, lies with equal interval and parallel direction, and reach at the other side of panel, then all the gate lines changes direction, go through the lead area and toward Integrate Circuit (IC) bonding area (three trapezoid unit at Fig. 1). Finally those gate lines concentrate together at the IC bonding area. The data lines go with the same pattern and concentrate at the data IC bonding area.

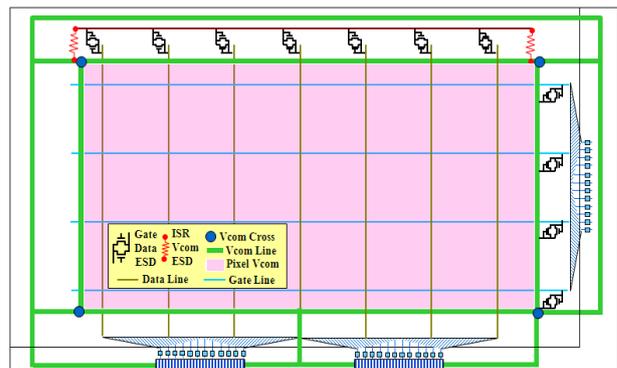


Figure 1. TFT-LCD panel outline

Except those lines in display area there are also many different functional lines lie in the peripheral area of display, especially locate between the IC area and the display area. Those functional lines can supply panel with various pulse and voltage. Those functions lines assistant gates line and data line to supply pixel with different voltage, and those pixel units work independently to form a picture (Fig. 2). When gate line/data line encounter with other functional lines, one must go across over to the other to avoid electronically short, so an insulator layer is inserted between two metal layer to prevent their short.

Although many actions are taken to prevent ESD, ESD still frequently happened between two insulated lines. With outer electric charge accumulating, the voltage between two lines rises higher. When the voltage exceeds the breakdown voltage, ESD occurs.

During mass production, it was found ESD is more easily to occur at some certain fixed cross area. The fixed position maybe related with contact point with equipment, or special design unit which is different with other area of normal area. This paper is to find out how line length influences the ESD possibility by comparing test lines.

Most test lines originated from the edge area of display and extend to a pad where research can be made.

III. EXPERIMENT

A. Selecting Proper Product

To study the influence of length of line on ESD, the lines to be compared should be the same material, same thickness, same surrounding circuit but with different length. A couple of twin lines meets the above requirements and is selected to be compared. Each of the twin lines is composed of one gate line connecting to one test line. The gate lines offer horizontal signal to drive the panel when displaying different pictures. Taking 7 inch panel for example, which is widely used in pad, mini portable notepad, or small screen fixed on the backseat of a car. Its resolution is 1024×600, which means there are 600 horizontal lines. The 600 gate lines are named G1, G2...G600 respectively. The G1 to G600 are with the same material, same length, same width (Fig. 2), original from one side of panel, go through the panel and reach at the other side of panel, then gather together at the IC bonding area. While unlike G2~G599, G1 and G600 are connected with their corresponding test lines (red lines in Fig. 2) at the end of IC bonding area. The test lines start from G1 or G600 at the IC bonding area, go through the similar route and finally end as the test pad at a spacious area. The test line is an extend tail from normal G1 or G600 gate line, and the function is only for research or monitor purpose. G1 and G600 are all in identical except their connected corresponding test line length. What is more, because the test line for G1 and G600 are original from different site, thus makes their different length. It can be concluded from Fig. 1 that G1 from the gate line 1. By exactly calculating, G600 is 30mm longer than G1 line. Considering the total line length, the longer line is 14% longer than the shorter line, as shown in Fig. 2.

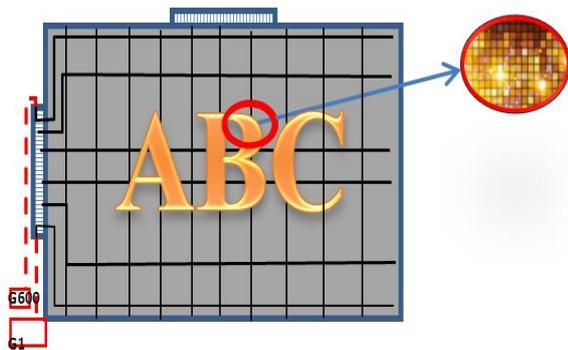


Figure 2. Test lines distribution on 7 inch panel

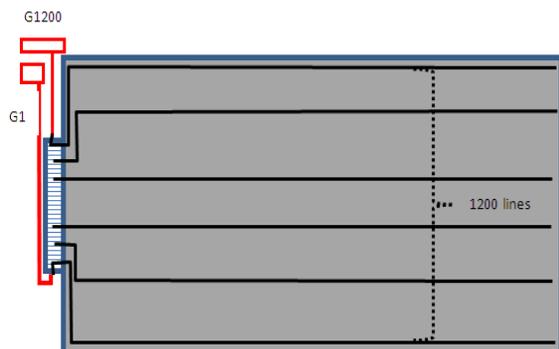


Figure 3. Test lines distribution on 8 inch panel

To further confirm the result, another product: 8 inch was taken into experiment. Its resolution is 1024×1200. The product also has two gate test lines, one is G1 and the other is G1200, G1 and G1200 are also connected to G1 and G1200 respectively. They are similar designed except length. Unlike G1 is shorter than G600 in 7 inch, G1 is longer than G1200 in 8 inch (Fig. 3). And G1 is 11% longer than G1200 in length.

B. Experimental Step

Step 1: The first step is to prepare enough samples. The manufactured procedure can be divided as array process and cell process. Array process is to form the necessary lines and cell process is to add liquid and colour filter to make it displayable. Array process is a standard TFT-LCD process, mainly composed of thin-film, photo, etch and strip. The first metal layer is 260nm thickness Al then with 80nm thickness Mo. The line CD is 3.5um. The second metal layer is Mo with thickness of 220nm, and its CD is 4um. To form the whole TFT structure, other layers are required to form the necessary pattern. The other layers consist of pixel ITO, common ITO, active layer, gate insulator layer and PVX layer. After the last pattern is formed, the array process finished.

There is an electronic test after array process, where all electronic defects including short or open can be detected. Make sure that no ESD occurred after array test. Then the substrate can flow to the next step.

Cell process begins with PI coating, and then followed by rubbing. Rubbing is a high risk process for ESD, because the glass substrates are rubbing by a highly rotating cloth wrapped around a rubbing rolling, as figured in Fig. 4. The cloth is made from cotton or nylon, which is easy to generate static electricity when contacting with TFT substrate. After rubbing process the TFT substrate is dropped with enough liquid crystal and covered with a colour filter substrate. The last process is to scribe the substrate into proper size. For instance, a big substrate can be scribed into 56 pcs 8 inch panel (7 rows and 8 columns), or 72 pcs 7 inch panel (12 rows and 6 columns). After those procedures two split samples are prepared. Split 1 is 16000 pcs of 7 inch products and split 2 is 8000 pcs of 8inch products. During the main process, the two test lines are evenly exposed under potential ESD risk procedures like delivering, deionization, manual clean, etc.

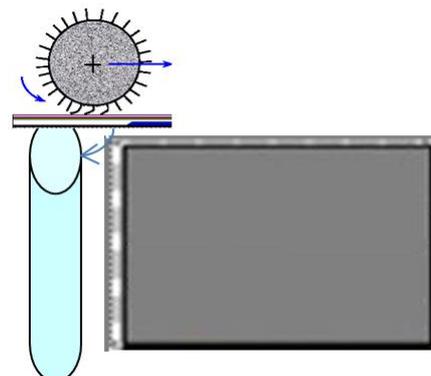


Figure 4. Rubbing process

Step 2: Check ESD. ESD in test line will lower the voltage on Gate line, resulting in a line defect in the screen. So ESD can be easily checked by visual test on light-on status. What is more, only grey patterns are applied to ensure that G1 and G600 are driven by the same voltage and pulse.

IV. RESULT AND DISCUSSION

The results are shown as below, all the 16000 pcs of 7 inch products were tested electronically one by one, and total 352 pcs products that have a line defect were detected, as shown in Fig. 5.

Observing the ESD location under the microscope, it can be found that the line defects is cause by ESD in the cross area. All ESD occurred at Site1 or Site 2 where G1 and G600 go cross with another line, as shown in Fig. 6. What is more, it can also be obviously summarized from the microscope images that all the ESD occur at site 2 while no ESD occur at site 1. In other word, all ESD

occur on the G600 while no ESD occur on G1. As shown in Fig. 7, small black dot can be observed obviously on the cross line of G600.

The result of 8 inch keeps accordance with result of 7 inch. As shown in Fig. 8, ESD overwhelmingly happened on the G1200 line. Both occur on the longer test line in the two splits.

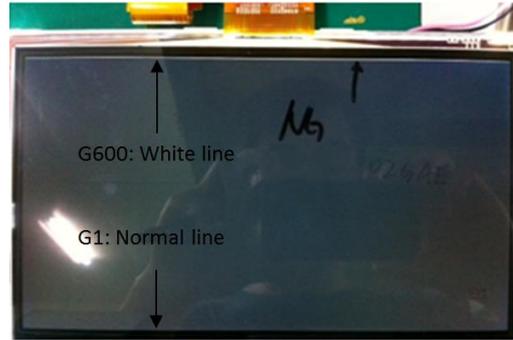


Figure 5. G600 line defect

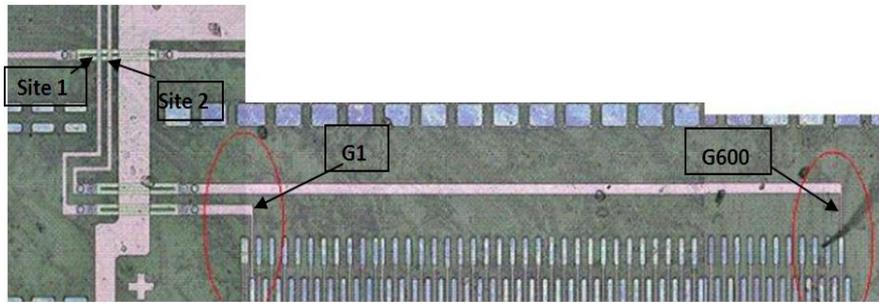


Figure 6. G1 & G600 around the IC bonding region

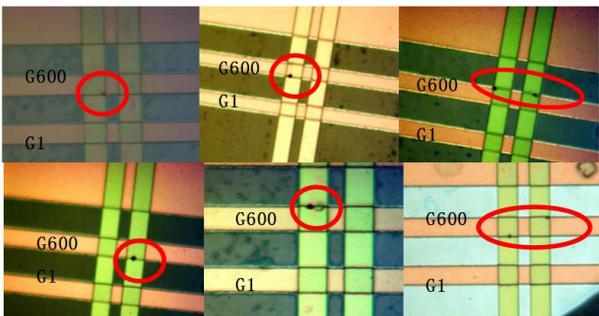


Figure 7. Microscope image of 7 inch

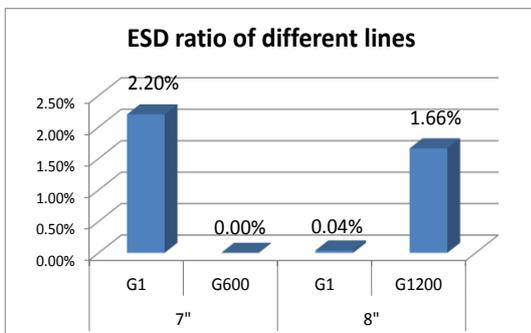


Figure 8. ESD ratio of different test lines

To confirm if the black dot is ESD, we analyzed the defect samples by FIB (Focused Ion beam) equipment (Equipment serial: FEI NOVA 200). As shown in Fig. 9.

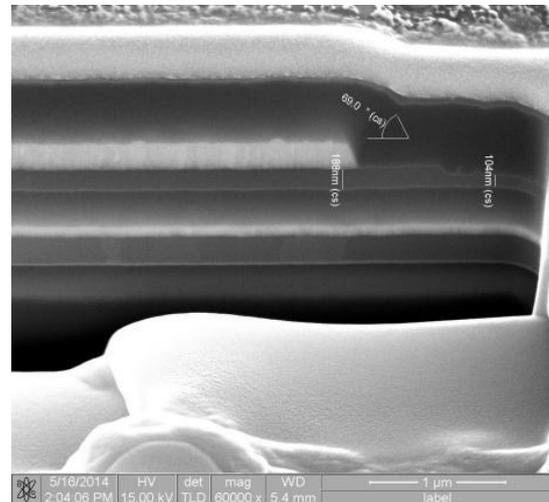


Figure 9. Cross section of normal area

The first mental layer (gate layer) is isolated from the second mental layer (data layer) by a SiNx layer inserting between them, which insulated them at the cross over area where they meet to each other. While in cross section of ESD area, an obvious ruin can be observed in the Fig. 10. The ESD event has caused a junction breakdown which caused the metal melt together. The insulator and protection layer are both crack down in the ESD event. The microscope pictures further prove that the small black dot is ESD rather than floating particle.

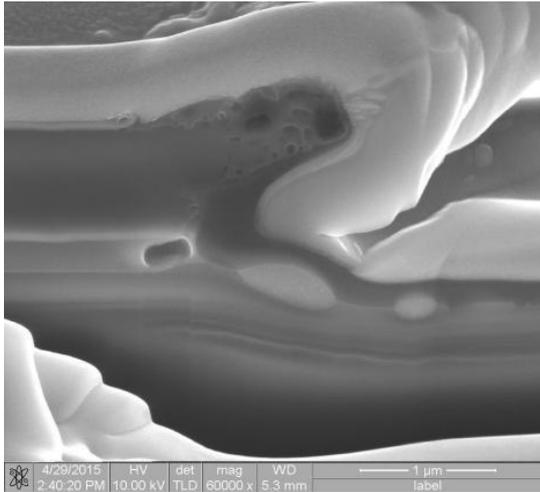


Figure 10. Cross section of ESD area

The theory is assumed as below: Taking the overlay area as a capacitor. So it can be deduced that:

$$C = \zeta S / 4\pi kd \quad (1)$$

$$U = Q / C \quad (2)$$

C: namely the capacitance of the capacitor;
 ζ : the dielectric constant of the insulator layer;
 S: the area of the overlap area of two lines;
 d: the thickness of the insulator layer;
 Q: the electric quantity of capacitor;
 U: the voltage between the two lines.

The S, ζ and the d are invariant, so the C is invariant.

There is no difference of overlay area (S) between the longer and shorter test lines. The test line is exposed to an open environment where electrons are floating anywhere. Electronics can deposit on the test line layer when hit the line. Because the longer test line is exposed to a more large area, the longer test line can accumulate more charge. With the charge accumulates more and more, namely that the Q rise more. Because the C is invariant, the U will rise higher when the Q rise higher. When the U exceeds the breakdown voltage of the capacitor, the ESD occurs. As is described in Fig. 11, the charge will discharge at the overlay area.

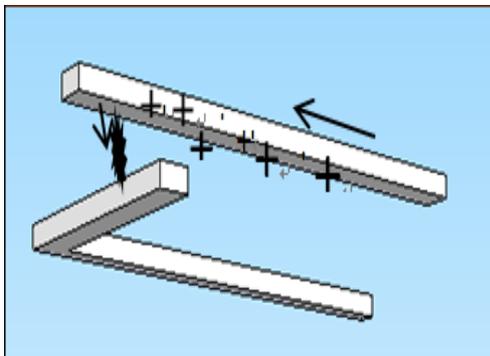


Figure 11. Electrons discharge at the cross area

According to the theory, the possibility of ESD goes directly with the charge quality, and the charge quality goes directly with the exposed test line area. Thus we can conclude that with the same test line length, the longer

the test line, the more easily the ESD will occur. In 8 inch products when the length difference is 11%, the ESD in shorter line is much rare than in longer line, while in 7 inch product when the length difference reaches 14%, the ESD overwhelming on the longer line (Table I).

TABLE I. ESD RATIO WITH DIFFERENT LENGTH DIFFERENCE

Product	Length difference	ESD @ long line	ESD @ short line
7 inch	14%	2.20%	0%
8 inch	11%	1.66%	0.04%

V. IMPACT & CONCLUSION

The factors which will enhance ESD were discussed. Take the two gate test line for comparing, experiments show that in the circuit of microelectronic device, with the same overlay shape and the same test line width, the longer the line is, the more easily ESD will occur. This rule is proven both in 7 inch product and in 8 inch product. And contrast between 7 inch and 8 inch in the difference of length show that when the longer line exceeds 14% than shorter line in length, the ESD would dominantly occurred on longer line. This will direct circuit design on how to avoid ESD, especially on avoid ESD by shorten functional line or adding a longer dummy line.

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Jingang Hao was born in July 1st, 1979 in China. He has gained bachelor degree from Chemistry College of Jilin University, Changchun, China in 2002 and master degree from Science College of Beijing Jiaotong University, Beijing, China in 2006. During his bachelor and master period, his main research was focused on OLED device and luminance efficiency, especially on doping system to generate white light.

He joined BOE Technology Group Co., Ltd. (Abbr. BOE) since 2006, and his main research focused on how to improve product yield. During the ten years' experience, accumulated rich experience in TFT array process control and panel yield up approaches. Yield up mainly focus on particle control, better uniformity and ESD prevention. The ESD prevention not only includes environment improving, but also contains optimizing design. He has applied many patents on TFT design and process, such as "A measurement of thinfilm thickness evaluation 201210129807.6 (2012-04-27)".