A 12-bit 2.88mW 50MHz SAR ADC in 0.18µm CMOS

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***Abstract*—In this paper a 12-bit 2.88mW 50MHz SAR ADC implemented in 180nm CMOS process is presented. A differential split CDAC is adopted which eliminates mismatch of the capacitors. A high-speed and high-resolution dynamic latch comparator is designed to save power. The key path of SA logic module is optimized, achieving 5 basic logic gates and only one DFF delay. The post-layout simulation achieves a SNDR of 60dB with a FOM of 56fJ/conv-step. The core occupies 0.4mm*0.6mm.**

***Index Terms*—analog-to-digital convertor, successive-approximation ADC, differential split charged-DAC, low power**

I. Introduction

ADC is an important module in a whole digital processing system getting information from nature world. SAR ADCs of medium sampling rate (10M-500M Hz) moderate resolution (6-12 bits) are wildly used, because SAR ADC has several advantages. Firstly, SAR can benefit from the development of scaled CMOS technology since it is no need for an amplifier included, which occupies smaller area to achieve the same performance than pipeline ADC and delta-sigma ADC. Secondly, SAR can achieve moderate speed for its linearity time consumption with resolution. Thirdly, when using CDAC, SAR ADC consumes lower power because the power of DAC is consumed only when the charge redistribution occurs. However, the speed of SAR is limited by charge redistribution and logic procedure. In order to accelerate, the CDAC and logic module need to be optimized.

In this paper, we rebuild the SA logic module to reduce the critical path delay so that it is possible for a SAR ADC to achieve 12-bit resolution with 50MHz sampling rate in 0.18µm process.

In Section II, the architecture of SAR is presented. In Section III, detailed circuits design is described. The DAC capacitor array and comparator are discussed. In Section IV, SAR logic design is explained. In Section V, the simulation results are shown and Section VI gives the conclusion.

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II. SAR Architecture

The SAR ADC architecture is designed as fully differential analog circuits combined with a digital SA logic module, as shown in Fig. 1 [1]. The analog circuits consists two main modules, which are a differential CDAC and a differential comparator. The CDAC is implemented as a split capacitor array with a bridge capacitor included to reduce the mismatch between different weighted capacitors. Bootstrap switch is applied in this architecture to improve the accuracy of the sampling process. The comparator is designed as a fully dynamic, simple and power-efficient one to save power and to reduce comparing time cost. The digital SA logic module is an asynchronous module, which is fine designed to reduce the number of data flip-flops in the critical control path, so as to cut the logic time down.

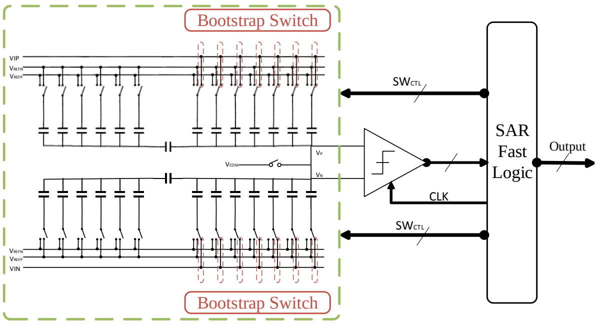

Figure 1. SAR architecture

III. Cirsuit Design

A. DAC Capacitor Array Design

The general view of CDAC is shown in Fig. 2. The CDAC consists two parts, positive part and negative part, each takes a bridge capacitor included. The differential architecture can eliminate even harmonics, while the bridge capacitor is designed for narrowing the capacity range and reducing the chip area. Without the bridge capacitor, to generate the demanding reference voltage

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according to the SAR logic, the capacity of each weighted capacitor should be set in a binary sequence. To meet the 12 bits demand, the ratio between the largest capacitor and the smallest one can be 2048 which is hard to be accurate when implemented in existed fabrication.

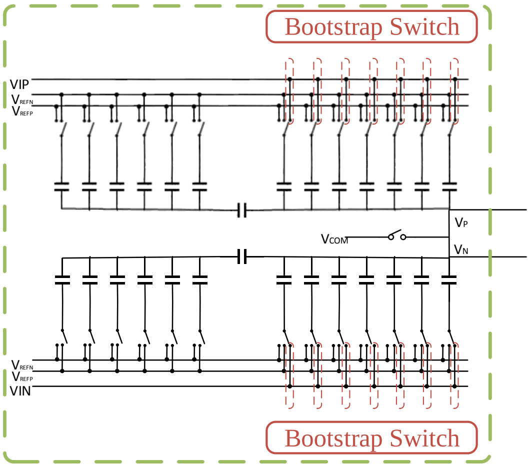

Figure 2. Split CDAC

We take bridge capacitors included. All the capacity of bridge capacitors is $2C_0$, and all the other capacitors' are C_0. Meanwhile an additional capacitor is included to adjust the weight of each capacitor.

During the sampling period, same as method two, the bottom plates connected to input, while the output nodes are connected to V_{cm}. The capacitor arrays are charged:

$$Q_P = (V_{COM} - V_{IP}) * 2C_0$$
$$Q_N = (V_{COM} - V_{IN}) * 2C_0$$

As the SA logic continues, the bottom plates are turned to connect either positive reference or negative reference according to the comparison result. The voltage of output node can be described as:

$$V_p = \Sigma_{i=0}^{12} V_{REFN} \bar{D}_i W_i + \Sigma_{i=0}^{12} V_{REFP} D_i W_i - V_{IP} + V_{COM}$$
$$V_N = \Sigma_{i=0}^{12} V_{REFP} \bar{D}_i W_i + \Sigma_{i=0}^{12} V_{REFN} D_i W_i - V_{IN} + V_{COM}$$

In this way the CDAC works correctly.

However, with the design above, the input capacitor is $2C_0$. As we know, the input capacity affects the thermal noise seriously. To meet the high resolution requirement, the input capacity should be large as C_d. The whole capacity of the CDAC array should be at least 17.5 C_d, which is too large in IC design. To solve this problem, we take a bridge capacitor include to divide the capacitor array into two parts, MSB-side (includes an extra basic capacitor) and LSB_side. In this design, LSB and MSB are designed in a 6 bits binary sequence, and the capacity of the bridge capacitor is equally designed as the unit capacitor of LSB and MSB. That is to say the ratio between the largest capacitor and the smallest one can be 32, which is much easier to meet the matching demand. Above we will describe the working principle of this CDAC to prove its correctness. During the sampling period, the bottom plates of MSB-side are connected to input, and the bottom plates of LSB-side are connected to V_{REFN} or V_{REFP} according to whether it is in positive terminal or not. While the output nodes are connected to V_{cm}, which is the common-mode voltage.

In the short hold period, before the successive approximation process starts, the bottom plates of positive MSB-side are connected to negative reference V_{REFN}, and negative MSB-side are connected to positive reference V_{REFP}. The electrical charge stored in output nodes of DAC is:

$$Q_P = (V_{COM} - V_{IP}) * 64C_0 + (V_{COM} - V_{REFN}) * \frac{63}{64} C_0$$

$$Q_N = (V_{COM} - V_{IN}) * 64C_0 + (V_{COM} - V_{REFP}) * \frac{63}{64} C_0$$

As the SA logic goes, the bottom plates are turned to connect either positive reference or negative reference according the comparison result, firstly. Then according to charge conservation, each MSB-bit can influence the first term while LSB-sides have effect on the second term of the equation, as:

$$Q_N = (V_{COM} - V_{IN}) * 64C_0 + (V_{COM} - V_{REFP}) * \frac{63}{64} C_0$$
$$= 64C_0(V_N - \Sigma_{i=0}^{6} V_{REFP} \bar{D}_i W_i - \Sigma_{i=0}^{6} V_{REFN} D_i W_i)$$
$$+ \frac{63}{64} C_0 (V_N - \Sigma_{i=7}^{12} V_{REFP} \bar{D}_i W_i - \Sigma_{i=7}^{12} V_{REFN} D_i W_i)$$

$$Q_P = (V_{COM} - V_{IP}) * 64C_0 + (V_{COM} - V_{REFN}) * \frac{63}{64} C_0$$
$$= 64C_0(V_P - \Sigma_{i=0}^{6} V_{REFN} \bar{D}_i W_i - \Sigma_{i=0}^{6} V_{REFP} D_i W_i)$$
$$+ \frac{63}{64} C_0 (V_P - \Sigma_{i=7}^{12} V_{REFN} \bar{D}_i W_i - \Sigma_{i=7}^{12} V_{REFP} D_i W_i)$$

where V_P and V_N stand for the output of DAC, D_i stands for the result of comparison, and $W_i = \frac{1}{2^i}$. So the output of DAC can be presented as follow:

$$V_P = V_{COM} + \frac{64[-V_{IP} + V_{REFN}(1 - \Sigma_{i=0}^{6} D_i W_i) + V_{REFP} \Sigma_{i=0}^{6} D_i W_i]}{64 + \frac{63}{64}}$$

$$V_N = V_{COM} + \frac{64[-V_{IN} + V_{REFP}(1 - \Sigma_{i=0}^{6} D_i W_i) + V_{REFN} \Sigma_{i=0}^{6} D_i W_i]}{64 + \frac{63}{64}}$$

A conclusion can get from the formula above: although the weight has changed to $\frac{64}{64+\frac{63}{64}} W_i$, instead of W_i, the relative weights are accurate, which can guarantee the CDAC's correctness. And in this way the input capacity is only needed to be larger than 2 C_d.

B. Comparator Design

The schematic of comparator is shown in Fig. 3. To use only one comparator in the whole architecture, the comparator is designed with a fully dynamic solution [2]. Without preamplifier, the comparator is simple to save power, while a pre-charging structure is applied to accelerate the module. When the clock signal is low, the circuit is reset: the output is set to high in both differential output terminal, during which time differential input CMOS pair doesn't work. When the clock signal changes to high, the differential input pair feeds currents into the cross-coupled CMOS regenerative pair. The cross-coupled CMOS pair amplifies the differential output of input pair into near the power supply voltage in a short time, and keeps the values. Two more CMOS transistors are included into the output and input of the cross-coupled CMOS pair, which are used to trigger the comparator itself.

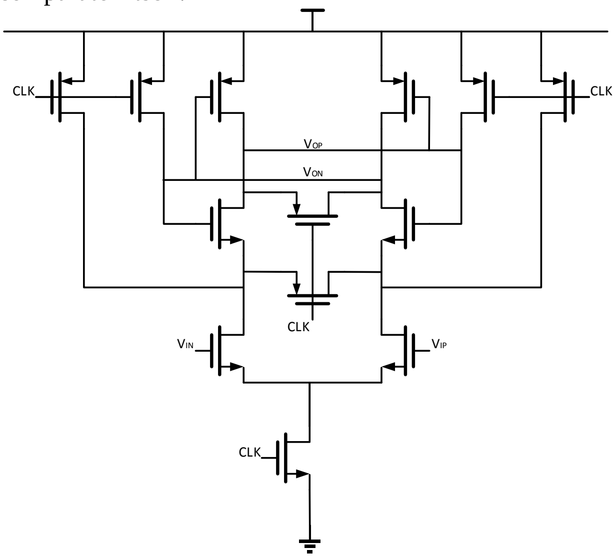

Figure 3. Comparator

IV. SAR Logic Design

The structure of SAR logic is shown in Fig. 4. Controlling sampling logic and making every bit decision in a single system period, SAR logic should control the CDAC and trigger the comparator in a high frequency. Sampling period is determined by RC constant which is influenced by CDAC's load capacitor and sampling switch. Where CDAC's load capacitor is determined by the precision of ADC and sampling switch is determined by the area and power consumption. In order to accelerate the whole circuits each bit decision cycle must be optimized. One bit decision cycle consists comparing period, logic operating period and CDAC redistributing period. Among these three factors, CDAC redistribution period is determined by CDAC load capacitor and logic controlled switch, which is hard to optimize. As the amplitude of input differential signal is different, the comparing period is variation. To avoid using fixed high frequency clock, the prototype SAR logic generates an internal clock in its system. Since the differential outputs of the comparator are both high during the reset period, but they are different after comparing, the SAR logic module XORs the outputs to generate its clock. The first comparing period is triggered by system clock. As the clock is generated based on comparator, each comparing period is identified from others, which can save time without the limit of longest period. With fixed structure, the logic operating time costs in each bit decision cycle are almost the same. To reduce the time cost from comparator to CDAC, a MUX is included. Fig. 5 shows the architecture of the MUX. The MUX is designed as a mealy machine, which is a finite states machine whose output is determined by both current stat and the input. The MUX is reset every system clock. Each bit decision cycle will change the stat to be ready for the next stat, and the output of the MUX is delayed by only one logic gate. The output signals of the MUX are used to drive a D-flip-flop latch array, in which the signal passes only one latch to trigger the CDAC. Because CDAC requires the control signal being kept during the comparing period. It takes no more than 4 basic logic gate delay to control the CDAC switch. As the load capacitor is proportional to bit's weight, the weightiest bit logic is special designed to reduce 2 basic logic gate delays. In all, one bit decision cycle only include one D-flip-flop and five basic logic gates. The D-flip-flop is optimized using dynamic logic design method to gain high speed, as shown in Fig. 6.

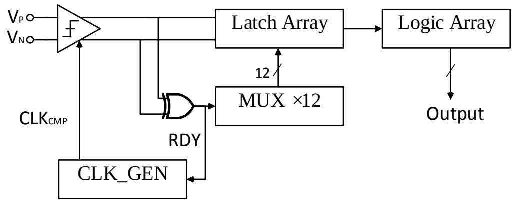

Figure 4. SAR Logic

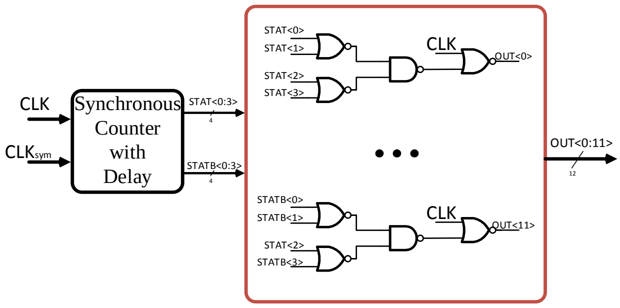

Figure 5. MUX

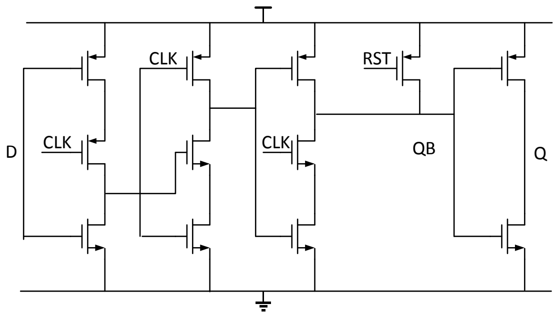

Figure 6. Dynamic logic D-flip-flop

V. Simulation Results

With the fabrication of 0.18μm 1P6M CMOS, the ADC core occupies 0.6mm×0.4mm. The layout of chip is shown in Fig. 7. The analog part is designed in the top part of the layout, and the digital part is implemented in the bottom part. The analog part and digital part is departed strictly, in order to reduce the effect of the clock signal. The arrangement of wire is carefully considered. All the wires which are used to transport important analog signal, are at least 1μm. The parallel signal paths are divided by a ground path in the same metal layer. Clocked at 50MHz and fed with a 21.2MHz sine wave, the prototype SAR ADC achieves peak SNDR of 60dB with 2.88mW power consumption under 1.8V supply, according to the post-layout simulation, as shown in Fig. 8. From the simulation result, it can be concluded that the thermal noise is in well controlled. According to the analysis of calibration algorithm and the simulation result, the mismatch of the CDAC array is not the most important factor of the design. So the mismatch of CDAC has been reduced effectively. Based on the definition of FOM (figure of merit), this ADC achieves an FOM of 56fJ/conversion-step. Performances of the ADC are summarized and compared to previous results in Table I.

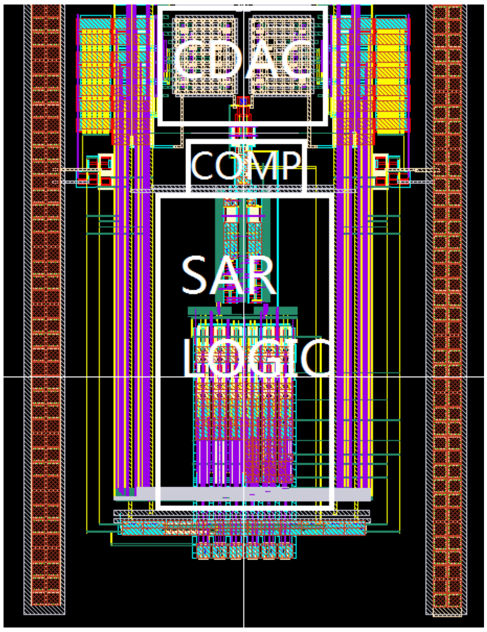

Figure 7. Layout

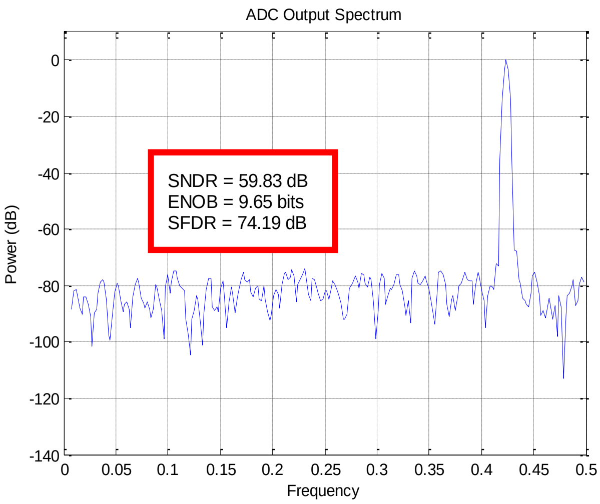

Figure 8. Post simulation

TABLE I. PERFORMANCES SUMMARY

Reference	[3]	[4]	[5]	Design
Resolution	67dB	65dB	49dB	60dB
Process	130nm	90nm	65nm	180nm
Sample Rate	45M	50M	100M	50M
FOM	41.9fJ	45fJ	45fJ	56fJ

VI. CONCLUSION

This paper presents a SAR ADC with a new method to optimize SA logic module. Proposed technique is confirmed by a 12-bit 50MHz SAR ADC fabricated in 0.18μm CMOS with 1.8V power supply. The post-layout simulation achieves a SNDR of 60dB with a FOM of 56fJ/conv-step. The ADC core occupies 0.6mm*0.4mm and consumes 2.88mW.

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