A Novel Charge-Protection Superjunction-Insulator VDMOS

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***Abstract*—A novel charge-protection Superjunction-Insulator (SJ-I) vertical double diffused MOSFET (SJ-VDMOSs) has been proposed. The proposed analytical-model of SJ-I drift layer is verified with the numerical simulation and compared with conventional SJ drift layer model. In the proposed device, we have inserted very thin (100*nm*) insulator pillar between two consecutive SJ pillars for charge protection and prohibit impurity inter diffusion. This method is optimized Charge Termination (CT) and covers less device area than conventional CT method. In proposed SJ-I devices, the Breakdown Voltage (BV) has been improved by more than 10% with identical area specific ON-resistance ($R_{on}A$) as compared to conventional SJ devices. Further, we have investigated transfer, output, maximum switching frequency and transient response of SJ-I device.**

***Index Terms*—superjunction, breakdown voltage, area specific ON-resistance, charge protection, charge termination**

I. Introduction

The invention of superjunction (SJ) devices is the milestone in power electronics [1]. The conventional siliconlimit (Si-limit) has been optimized by SJ devices [2]-[3]. Due to this, tradeoff between the Breakdown Voltage (BV) and area specific ON-resistance ($R_{on}A$) has been improved in power devices. However, the Charge Imbalance (CI), Charge Termination (CT) and impurity inter-diffusion are key issues in SJ devices [3]-[5]. Further, the separate high-*k* (HK) dielectric pillar in power devices was introduced to avoid impurity inter-diffusion, reduce $R_{on}A$ and improve BV [6]. But, some articles are reported that HK devices suffer from lower switching speed due to higher capacitance effect [7], [8]. The VDMOS reported in [9] with HK pillar describe that device BV increased and alleviates the CI issue. Nevertheless, these improvements are not much satisfying the design requirement of power electronics. Even previously reported models are very complex to optimize CT which requires extra padding of p-n pillar [10], so the device area has increased more than 50%.

In this paper, we have proposed novel SJ-insulator (SJ-I) device and its analytical model. The advantages of SJ-I devices are: - avoid impurity inter-diffusion, optimize CT with small increment in device area, transient and frequency response almost same as conventional SJ devices and increase BV without affecting *R*on*A*. In addition, for identical BV in SJ-I VDMOS $R_{on}A$ is 30% less than conventional SJ VDMOS.

II. Structure Description

The cross section view of the proposed SJ-I drift layer, conventional SJ drift layer [3], proposed SJ-I VDMOS and conventional SJ VDMOS are shown in Fig. 1(a-d). As compared to conventional SJ drift layer, the SJ-I drift layer is using very thin separate insulator-pillar (I-pillar) with integrated n-drift layer which is isolated two consecutive SJ pillar. This I-pillar prohibits impurity inter-diffusion within the SJ pillar and optimizes CT very nicely. Here, W_n, W_p, N_d and N_a are the widths and doping type of the n-pillar and p-pillar, respectively. In Fig, 2, we have shown, OFF state SJ-I drift layer, where, t_{epi} is the epitaxial layer and C_p is the cell pitch ($W_n + W_p$). E_x and E_y are lateral and vertical electric field, respectively. The resultant of E_x and E_y is critical electric field (E_c). As SJ-I drift layer can sustain maximum *BV* in OFF state, so it is design very precisely for SJ-I model.

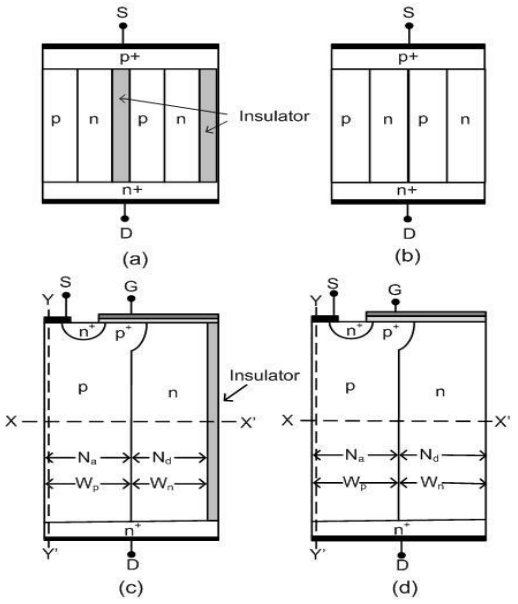

Figure 1. (a) Proposed novel charge-protection SJ-I. (b) Conventional SJ drift layer [3]. (c) Proposed Novel charge-protection SJ-I VDMOS. (d) Conventional SJ VDMOS.

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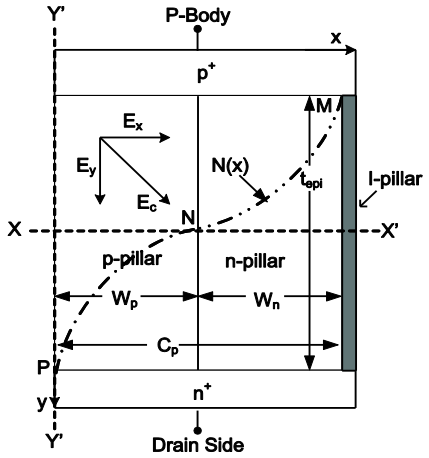

Figure 2. Electric field model of proposed SJ-I Drift layer.

III. Analytical Model

A. Electric Field

The SJ-I drift layer analytical model used Fulop [11] p-n junction. When the SJ-I device is in the reverse blocking mode a lateral depletion region formed across the n and p-pillar (across vertical junction). Further, two abrupt horizontal junctions are originated along the p^+n (region/pillar) and n^+p (region/pillar) interfaces. As the drain bias increases, both the lateral and vertical p-n junctions are depleted. The narrow pillar structure ($t_{epi}>>C_p$) of SJ drift layer fully depleted (lateral depletion) across vertical junction at a low drain bias. However, the two horizontal junctions have not fully depleted into the bulk of the drift region. When the drain bias is increasing continuously, then vertical depletion start along y-axis with drain bias and increases upto breakdown of electric field, i.e., E_c. For potential analysis, 2-D Poisson's potential function $\psi(x, y)$ can be written as:

$$\nabla^2\varphi(x,y) = \frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} = -\frac{qN(x)}{\varepsilon} \quad (1)$$

where, ψ potential function, q = charge, $N(x)$ = unitary step function for doping concentration and $\epsilon = \epsilon_r\epsilon_0$ permittivity, ϵ_r relative permittivity of material (for Si, ϵ_r = 11.97), ϵ_0 permittivity of vacuum.

For Fig. 2, $N(x)$ can be written as:

$$\mathrm{N(x)} = \frac{4N}{\pi}\cos\left(\frac{\pi x}{C_p}\right) \quad (2)$$

where,
$N > 0$, $0 < x < C_p/2$
$N = 0$, $x = C_p/2$
$N < 0$, $C_p/2 < x < C_p$

Here, the value of $N(x)$ depend upon the polarity of N, where $N > 0$ shows p-type doping (hole in majority), $N < 0$ shows n-type doping (electron in majority) and $N = 0$ shows charge neutrality in SJ-I structure.

We have put equation (2) into equation (1), hereafter solve for the boundary conditions are ($\psi = BV$, $y = t_{epi}$) and (ψ=0, y=0). For solution of these equations, we assume that once the p-n pillars are fully depleted by lateral and vertical junction. Further increase in the drain bias will not change the charge distribution within the unit cell of SJ-I drift layer. The solution of Poisson's equation is given as:

$$\varphi(x,y) = \frac{4qNC_p^2\cos\left(\frac{\pi x}{C_p}\right)\left[1-\frac{\cosh\left(\frac{\pi y}{C_p}\right)}{\cosh\left(\frac{\pi t_{epi}}{2C_p}\right)}\right]}{\varepsilon\pi^3} + \frac{BV}{t_{epi}}y \quad (3)$$

The x-component of the electric field $E_x = -\partial\varphi/\partial x$ is:

$$E_x = \frac{4qNC_p^2\sin\left(\frac{\pi x}{C_p}\right)\left[1-\frac{\cosh\left(\frac{\pi y}{C_p}\right)}{\cosh\left(\frac{\pi t_{epi}}{2C_p}\right)}\right]}{\varepsilon\pi^2} \quad (4)$$

Assume, SJ-I layer shown in Fig. 2 laterally fully depleted and the solution of equation (4) across $X - X'$ as shown in Fig. 3(a). For the boundary conditions are ($y = t_{epi}/2$) and ($0 \le x \le C_p$) at $x = C_p/2$, we have obtained $E_x = E_{x;max}$ as shown in Fig. 3(a). The x-component of the electric field $E_y = -\partial\varphi/\partial y$ is:

$$E_y = \frac{4qNC_p^2\cos\left(\frac{\pi x}{C_p}\right)\left[1-\frac{\cosh\left(\frac{\pi y}{C_p}\right)}{\cosh\left(\frac{\pi t_{epi}}{2C_p}\right)}\right]}{\varepsilon\pi^2} + \frac{BV}{t_{epi}} = E_{y0} + E_0 \quad (5)$$

here, the term E_{y0} defined in equation (5) is periodic in x-direction and anti-symmetric with respect to y-axis. E_{y0} is doping and geometry dependent. The second term on right-hand side of equation (5) is

$$E_0 = \frac{BV}{t_{epi}} \quad (6)$$

and this term is not subjected to doping of the semiconductor and location. We have assumed that SJ-I drift layer as shown in Fig. 2 vertically fully depleted and the solution of equation (5) across $Y - Y'$ shown in Fig. 3(b). For boundary conditions are (x = 0) and ($0 \le y \le tepi$) at $y = t_{epi}$, we have obtained $E_y = E_{y;max}$ as shown in Fig. 3(b).

B. Impact Ionization

The SJ-I devices is subjected to avalanche breakdown by impact ionization phenomena. So, it is necessary to incorporate the impact ionization in simulation, while designing power devices. When high enough reverse bias voltage is applied across Source-Drain terminal of device and this produced sufficient electric field for accelerating free carriers. These accelerated carriers collide with the atoms of crystal and excite the valance band electrons into conduction band. Then electron-hole ($e-h$) pairs are created in the depletion region. The chain-generation of $e-h$ pair is called impact ionization. Further, the rate of impact ionization approaches infinity and device undergo avalanche breakdown. The impact ionization is critical parameter for analyzing devices BV. The impact multiplication M_p is given as [12]

$$M_p = \frac{1}{1-\int_0^w \alpha_n exp\left[\int_x^w(\alpha_n-\alpha_p)\,dx'\right]dx} \quad (7)$$

where, w is depletion width and x is starting point of the depletion. Using the concepts of average ionization

coefficient, BV occurs at the ionization integral become unity and rearrange equation (7)

$$\int_0^w \alpha_n \, dx = 1 \quad (8)$$

here, α_n depends on electric field, given as for silicon is $1.38\times10^{-38}E^7$ by Fulop [11].

IV. Results and Discussions

The 2-D TCAD simulator (Silvaco-Atlas) has used to analyze the proposed SJ-I VDMOS and simulation results are confirmed by conventional SJ VDMOS. The comparison results between proposed SJ-I and conventional SJ have been discussed in this section. In simulation, the models are used Shockley-Read-Hall (SRH), carrier-dependent lifetime, high field saturation mobility and Selberherr impact ionization [13].

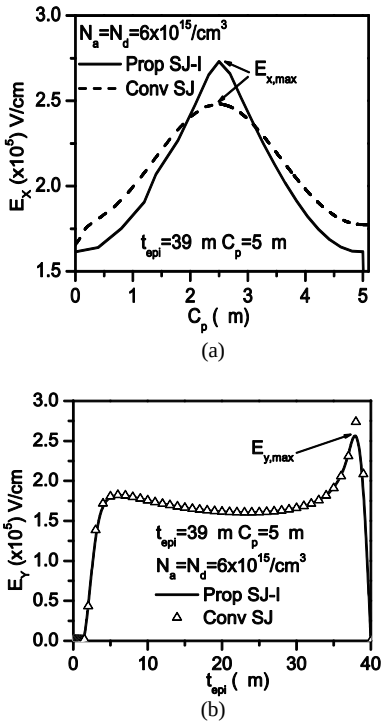

Figure 3. Numerical simulation result of electric field at BV (a) OFF-state Ex(@y = tepi=2) for SJ-I using Equation (4) and conventional SJ model given in [3]. (b) OFF-state Ey(@x = 0) for SJ-I using Equation (5) and conventional SJ model given in [3].

The 2-D electric field investigation of the balanced symmetric structure of SJ-I and SJ devices are performed across the cut-lines $X - X'$ and $Y - Y'$. These cut-lines are shown in Fig. 1(c, d). In Fig. 3(a, b) are showing off-state distribution of E_x and E_y across cut-line $X - X'$ and $Y - Y'$, respectively. Here, we have revealed that the E_x distribution along the X-X′ are not identical for both devices and large area under curve of E_x for SJ-I drift layer. As we have observed that the SJ-I and SJ devices have bidirectional electric field. To achieve premature BV both electric fields resultant should be equal to E_c [14]. Using the above analysis, we have predicted that the proposed SJ-I device achieved higher BV than conventional SJ devices as shown in Fig. 4.

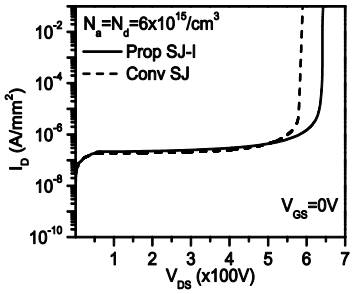

Figure 4. OFF-state leakage current and BV (For *tepi* = 39 μm, *Cp* = 5 μm).

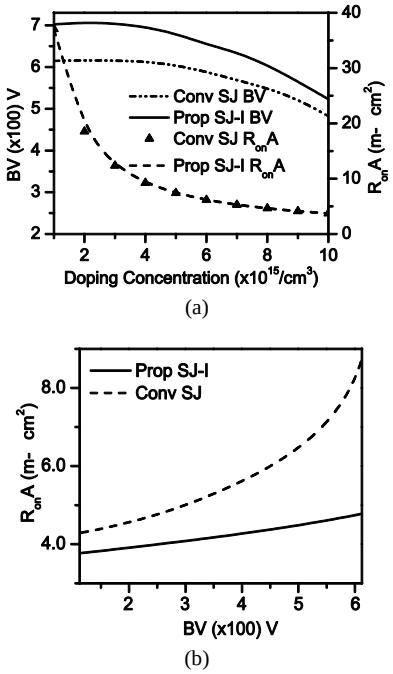

Figure 5. (a) R*on*A and BV versus pillar doping concentration (b) R*on*A comparison with respect to BV (For *tepi* = 39 μm, *Cp* = 5 μm).

The CT is responsible for BV degradation in SJ devices [10]. In the proposed SJ-I, we have used thin I-pillar to optimized CT. The effect of CT optimization in SJ-I devices BV are improved by more than 10% with identical device geometry, doping concentration and *RonA* as shown in Fig. 5(a). The $R_{on}A$ of SJ-I and SJ device can be calculated using relation $2t_{epi}/(q\mu_n N_d)$. The variations in $R_{on}A$ with respect to BV are as shown in Fig. 5(b). Here, we have observed that the increment of $R_{on}A$ almost flat for proposed SJ-I, whereas in conventional SJ devices $R_{on}A$ is linearly increased. The above investigations are performed under the perfect Charge Balance (CB) condition known as $N_aW_p = N_dW_n = Q_{SJ}$ to obtain maximum BV.

Transfer characteristics for both devices are shown in Fig. 6(a). These characteristics are obtained by device simulator at 300 K. Here, J_D is the current density of the drain. In Fig. 6(a), V_{GS} is increasing across the G and S terminal for various static values of V_{DS}. This shows for same value of V_{GS} with static increment of V_{DS}, J_D is increased. Here, we have observed that the transfer

characteristics are identical for both devices. The output characteristic of the SJ-I/SJ VDMOS is important for the switching when it is operated for Switch Mode Power Supply (SMPS) application. Fig. 6(b) shows ON-state output characteristics (i.e., linear and saturation region) are identical for both devices.

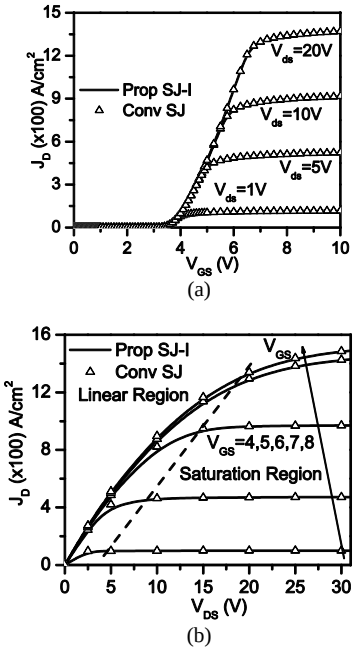

Figure 6. Vertical SJ power MOSFET (a) transfer characteristic (b) output characteristics

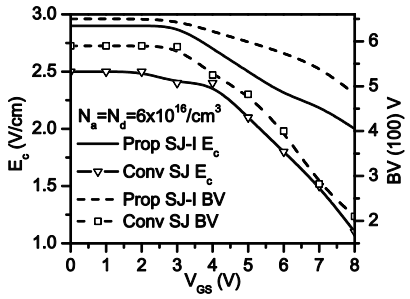

Figure 7. *EC* and BV versus V_{GS}

The ON-state E_C and BV versus V_{GS} are shown in Fig. 7. We have observed that the E_C and BV of both devices decreased with respect to V_{GS}. This causes, increase charge in the active channel and the drift region are increased which increased J_D. Hereafter, the negative charges of the moving electrons in the n-pillar cause some of the negative charges of the ionized acceptors in this condition very difficult to maintain CB in on-state. As we have observed that at the lowest values of V_{GS} the BV is highest. However, V_{GS} increases above the threshold voltage ($V_{th} \approx 3V$), so BV has been decreased and J_D increases gradually very high. Here, we have observed that in SJ-I devices the ON-state CI is less as compare to SJ device, this is due to optimized CT.

In Fig. 8(a), we have depicted frequency response of the vertical SJ power MOSFET with respect to V_{GS}, with the various static values of the V_{DS}. The variation in frequency response is the function of gate capacitance (C_G) and transconductance (g_m). Whereas, the g_m ($\partial I_D/\partial V_{GS}$) is strongly depend on I_D and V_{DS} strongly affect the overlap gate-drain capacitance (C_{GD}). The I_D is highly depending on the channel conductance and gate/drain bias. Here, we are using I-pillar in proposed SJ-I devices and permittivity of I-pillar is less than silicon pillar, so that we did not find any variation in frequency response between SJ and SJ-I devices.

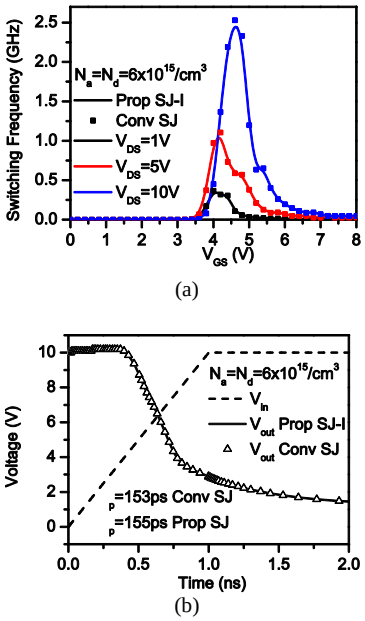

Figure 8. Vertical SJ power MOSFET (a) switching frequency response (b) transient response.

Transient responses of the both devices are shown in Fig. 8(b). The transient response is obtained using inverter circuit configuration. In this circuit, we have connected external 100KΩ R_L in series as the load of drain terminal and V_{DD} fixed at 10V-DC. Then V_{GS} is input supply with a ramp time of 1ns and voltage from 0-to-10V is applied to observe the transient response of the devices. The output voltage is measured across the drain and source terminal of the device. In order to observe accurate switching response, we have applied fixed V_{DS} = 10V-DC. The propagation delay (τ_p) of the conventional SJ device is 153ps and proposed SJ-I is 155ps. This analysis is validated by above discussed frequency response. Table I shows Comparisons between Proposed SJ-I And Conventional SJ Model Result For Pillar Doping $6x10^{15}cm^{-3}$.

TABLE I. COMPARISONS BETWEEN PROPOSED SJ-I AND CONVENTIONAL SJ MODEL RESULT FOR PILLAR DOPING $6x10^{15}CM^{-3}$

Parameter	Proposed SJ-I Model	Conventional SJ Model
t_{epi} (μm)	39	39
C_p (μm)	5	5
E_c (V/cm)	$3.1x10^5$	$2.9x10^5$
BV (V)	600	590
RonA ($m\Omega cm^2$)	6.16	6.16
t_p *(ps)*	155	153
f_T *(GHz)* (V_{DS} = *1V*)	*0.436*	*0.436*
f_T *(GHz)* (V_{DS} = *5V*)	*1.1*	1.1
f_T *(GHz)* (V_{DS} = *10V*)	*2.53*	*2.53*

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V. Conclusions

In this paper, a novel charge-protection SJ-I drift layer for VDMOS has been discussed. The proposed SJ-I drift layer compared with conventional SJ drift layer with identical devices dimension and improvement in BV more than 10% with identical $R_{on}A$ is observed. For doping $6\times10^{15}\ cm^{-3}$ and $t_{epi} = 39\mu m$ BV of SJ-I-VDMOS is 660V, whereas in conventional SJ VDMOS is only 590V. In addition, the proposed SJ-I devices $R_{on}A$ is 30% less than conventional SJ VDMOS without affecting the BV. We have revealed that a thin insulator between the two SJ layers do not affect the device on-state behavior significantly.

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