

Simulation and Experimental Validation of Common Mode Voltage in Three Phase Induction Motor Driven by Five Level Inverter Using PIC Microcontroller

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Abstract—The Induction Motor is considered to be a constant speed motor. Squirrel-cage induction motors are widely used in industrial applications. Due to the advancement in power electronics and in microprocessor technology the speed of the Induction Motor can be varied within certain limitations. There are many methods to control and run the induction motor in Variable speed drive applications. The speed of an induction motor can be varied by changing the frequency of the AC voltage applied on the stator. The amplitude of the AC voltage applied on the stator should be proportional to the frequency, to maintain a constant air gap flux. Speed of an induction motor can be controlled by maintaining the voltage to frequency ratio constant. The method of V/f control gives good performance under steady-state, which is sufficient for motor drive industrial applications. The basic method is 2-level inverter controlled by the microcontroller using the space vector modulation method. By this method the output of the inverter will be Non- sinusoidal and hence at the star point of the load there exists a Voltage with respect to ground and it is known as Common Mode Voltage, which produces electromagnetic interference. To lower the Common Mode Voltage a higher level of inverter can be used. By using the 5-level inverter the common mode voltage can be minimized when compared to 2-level and 3-level inverter. In this paper the authors have discussed the 5-level inverter driving the induction motor by simulation using MATLAB-Simulink and by Experiment. Fast Fourier transform has been done using the signal Analysis software and results are plotted with frequency versus voltage. The Common Mode Voltage is measured using Agilent make mixed signal oscilloscope. In the conclusion, the result of 5-level inverter common mode voltage is compared with 3-level and 2-level inverter values are compared with different operating frequencies of Induction Motor is shown in the table.

Index Terms—common mode voltage, induction motor, three phase voltage source 2/3/5-level inverter, pulse width modulation, space vector modulation

I. INTRODUCTION

The Common Mode Voltage (CMV) exists at the star point of the Induction Motor (IM) in three phase inverter using Space Vector Modulation (SVM) technique. The output of the Voltage Source Inverter (VSI) will be non-sinusoidal. The existence of CMV has been reported by B. Muralidhara [1], [2]. In addition, due to the asymmetrical flux through the arbour line loop induces CMV. A. Muetze [3] reports the High-Frequency (HF) component that exists at the CMV. Hence it is necessary to minimize the CMV within limits [4] so that there will be minimized Electromagnetic Interference (EMI) and the insulation problem of the winding.

In industrial applications the three phase 2-level and 3-level inverter is widely used in variable speed IM drive systems using VSI which produce three phase AC output voltage of desired amplitude and frequency from a fixed DC voltage source. In 2/3/5-level inverter, the output waveform of inverter is stepped square wave. The output waveform of an inverter should be sinusoidal for efficient operation. The complexity of circuit is more in higher level inverter. A. Nabae [5] in 1981 discussed the Multilevel Inverter (MLI) concept. The advantages are with low switching losses with reduced EMI and with better power quality. The drawbacks for higher level inverters are complexity in circuits, the number of switching devices and various DC voltage levels. The PIC microcontroller [6] has been used to generate gate pulses for the 5-level inverter as per the Hexagon of space vector modulation [7], [8]. The drive circuit is interfaced with necessary opto-isolation modules and three phase H-bridge circuit is used to drive the switching devices.

II. CMV IN INVERTER DRIVEN THREE PHASE IM

The CMV is represented in mathematical form, to analyze its characteristics among various types of source

and load combinations. In three phase AC loads, the phase to ground voltages can be written as the sum of the phase voltages and the voltage across the star point of the load to the common ground of the source power supply. The sum of all three phase-to-neutral voltages is zero in a three phase sinusoidal balanced system; the voltage from the star point of load to common ground can be defined in terms of phase to ground voltage as shown in Fig. 1 and (1)-(5).

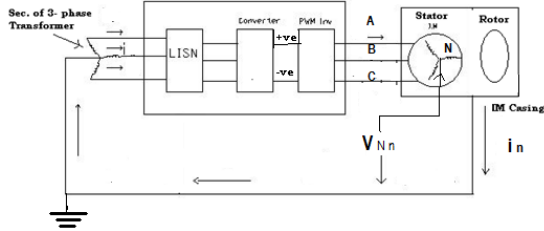


Figure 1. Inverter fed IM to measure common mode voltage.

$$V_{A-n} = V_{AN} + V_{N-n} \quad (1)$$

$$V_{B-n} = V_{BN} + V_{N-n} \quad (2)$$

$$V_{C-n} = V_{CN} + V_{N-n} \quad (3)$$

For balanced 3 phase system, $\Sigma V = 0$

$$V_{AN} + V_{BN} + V_{CN} = 0 \quad (4)$$

$$V_{N-n} = [(V_{A-n} + V_{B-n} + V_{C-n}) / 3] \quad (5)$$

III. SPACE VECTOR MODULATION

The experimental work uses the Space Vector Modulation (SVM) method, which produces the output voltage by using the three nearby output vectors. When one of the reference vector moves from one sector to another, results in an output vector abrupt change. In addition it is necessary to find the switching patterns and switching time of the states at each change of the reference voltage. The main advantages are to overcome the variation in DC bus voltage, the ratio V/f of IM is maintained constant by compensating for regulation in inverters. The three phase voltages are

$$V_a = V_m \sin \omega t \quad (6)$$

$$V_b = V_m \sin(\omega t - 2\pi/3) \quad (7)$$

$$V_c = V_m \sin(\omega t - 4\pi/3) \quad (8)$$

SVM is a better technique for generating a fundamental output ($\sim$ sine wave) that provides a higher output voltage to the three phase IM and less Total Harmonic Distortion (THD) when compared to sinusoidal PWM. The switching vectors Hexagon for 2/3/5-level are shown in the Fig. 2-Fig. 4.

The basic circuit of the 5-level Neutral Point Clamped (NPC) inverter is shown in Fig. 5. The switching state of each phase of the inverter is listed in Table I. The output space vector voltage is identified by the combination of switching states P2, P1, O, N1 or N2 of the three legs of Fig. 6. For example, in the case of P2, O, N1, the output terminals 'a', 'b' and 'c' have the potentials $V_{dc}/2$, 0, and

$-V_{dc}/4$ respectively. Since five types of switching states exist in each leg, a 5-level inverter has $5^3 = 125$ switching states, as indicated in the space vector diagram Shown in Fig. 6. The output voltage vector can assume only 61 discrete positions because some switches are redundant and create the same space vector [9]-[12]. Only the outer most space vector (24) is considered since all the other inner vectors are not considered due to redundancy.

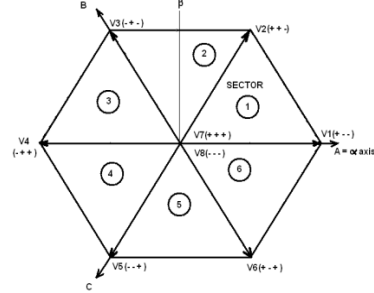


Figure 2. Switching vectors and sectors for 2-level inverter.

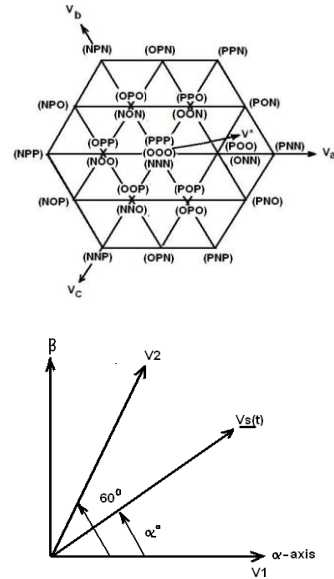


Figure 3. Switching vectors for 3-level inverter and Sampled reference vector in sector-1

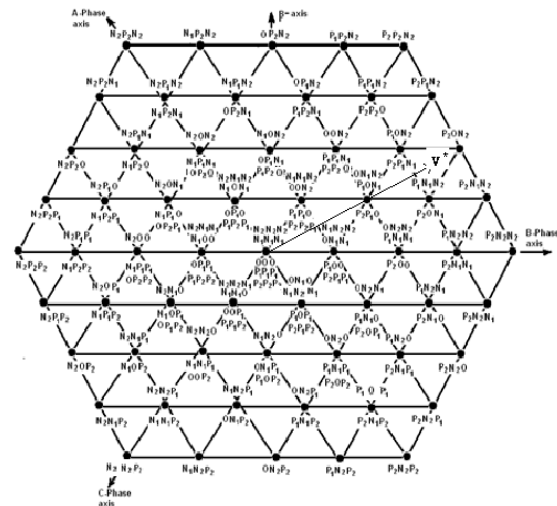


Figure 4. Switching vectors for 5-level inverter.

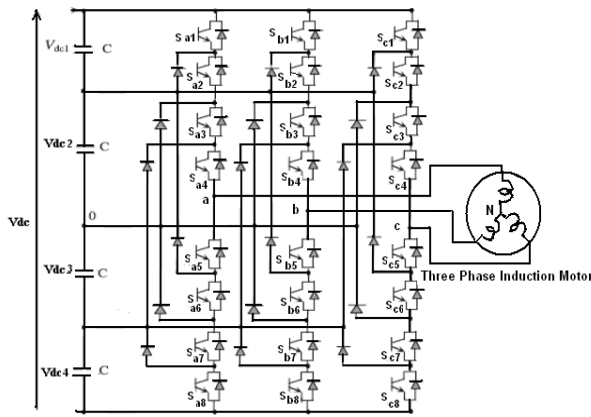


Figure 5. Circuit diagram of NPC 5-level inverter

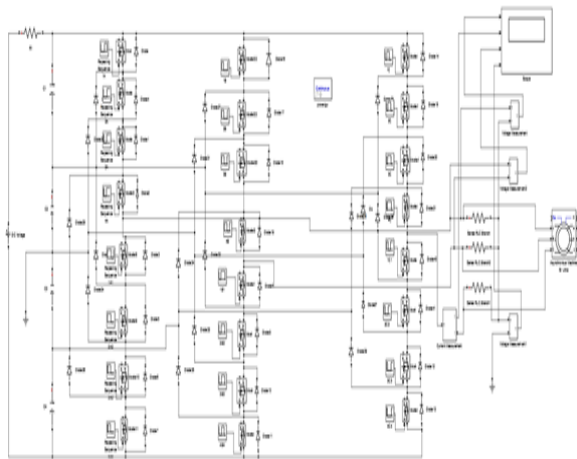


Figure 6. Simulation circuit of NPC 5-level inverter

The basic circuit of the 5-level NPC inverter [13] is shown in Fig. 5. The switching state of each phase of the inverter is listed in Table I. The output space vector voltage is identified by the combination of switching states P2, P1, O, N1 or N2 of the three legs of Fig. 4.

For example, in the case of P2, O, N1, the output terminals 'a', 'b' and 'c' have the potentials $V_{dc}/2$, 0, and $-V_{dc}/4$ respectively. Since five types of switching states exist in each leg, a 5-level inverter has $5^3 = 125$ switching states, as indicated in the space vector diagram shown in Fig. 4. The output voltage vector can assume only 61 discrete positions because some switches are redundant and create the same space vector [12]. Only the outer most space vector (24) is considered since all the other inner vectors are not considered due to redundancy.

TABLE I. SWITCHING STATES OF 5-LEVEL NPC INVERTER

MODE/ STATE	S1	S2	S3	S4	S1 ¹	S2 ¹	S3 ¹	S4 ¹	V _{OUT}
P2	1	1	1	1	0	0	0	0	$V_{DC}/2$
P1	0	1	1	1	1	0	0	0	$V_{DC}/4$
O	0	0	1	1	1	1	0	0	0
N1	0	0	0	1	1	1	1	0	$V_{DC}/4$
N2	0	0	0	0	1	1	1	1	$V_{DC}/2$

IV. PROPOSED WORK

Simulation circuit and experimental circuit of 5-level inverter shown in Fig. 5, Fig. 6 with 24 devices using SVM for the speed control of three phase IM is reported. The 2 and 3-level inverter results are taken from the published results [14], [15]. The CMV, phase voltage, line voltage, sum of phase current and phase current are measured using Agilent Mixed Signal Oscilloscope (MSO) associated with Hall sensor, Current probes etc., Simulation has done using MATLAB SimuLink.

A. Experimental Setup

In the experimental circuit uses MOSFET's (2SK962) as switching devices with high frequency anti parallel fast recovery diodes is used between drain and source of the MOSFET. The PIC-Microcontroller (16F877) is programmed to generate the gating pulses to the MOSFET's with proper opto-isolation circuits. 6N139 IC is used as an opto-isolator with isolated DC (+15V) power supply. The DC supply to the 5-level inverter is given using 3-phase Converter with filtering capacitor and Line Impedance Stabilization Network is used to block the unwanted noise signal voltage. DC link high voltage (1200V) capacitor (50 μ F) has been used. The necessary FFT analysis has done in simulation using MATLAB/ Simulink and for the experimental results using Origin Signal Analysis software. The CMV is analyzed for different frequencies (30Hz, 40Hz, 50Hz) for 5-level Inverter and compared with 2-level and 3-level inverter from earlier published [14], [15] results of the same authors.

V. SIMULATION AND EXPERIMENTAL RESULTS

The pic microcontroller is used for the generation of gating signals for the 5-level NPC inverter shown in Fig. 7. The simulated waveform results are shown in Fig. 8, the experimental results of CMV, Phase Voltage, Line Voltage, Phase Current are recorded using Agilent MSO (500MHz) shown in Fig. 9 to Fig. 11. In CMV, the harmonic frequencies are three times the fundamental frequency. Some harmonics will not produce useable torque, but produces opposing torque and heat, which are harmful to the insulation of IM. In Fig. 12 shows the Simulated FFT analysis of CMV using MATLAB Simulink and in the Fig. 13 shows the FFT analysis of Experimental results using Signal Analysis software for the 30Hz, 40Hz and 50Hz of Operation.

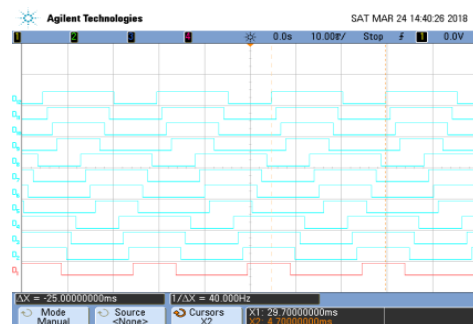


Figure 7. MSO recorded gating signals of 5-level NPC inverter, 40Hz.

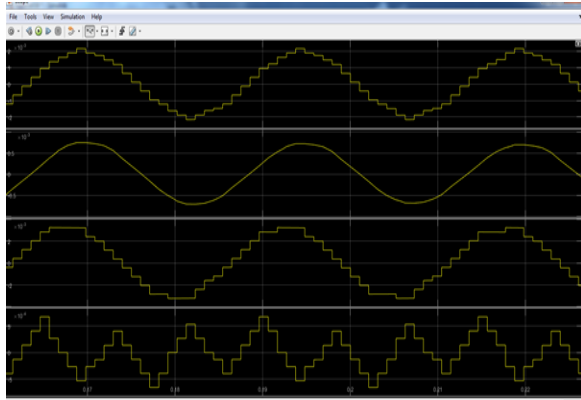


Figure 8. 40Hz simulated output waveforms of 5-level inverter. Top to bottom: Ch-1; phase voltage, Ch-2; line current, Ch-3; line voltage, Ch-4; common mode voltage.

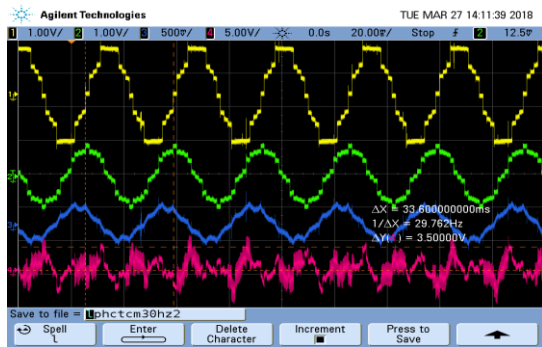


Figure 9. Exptl. 30Hz experimental output waveforms of 5-level inverter

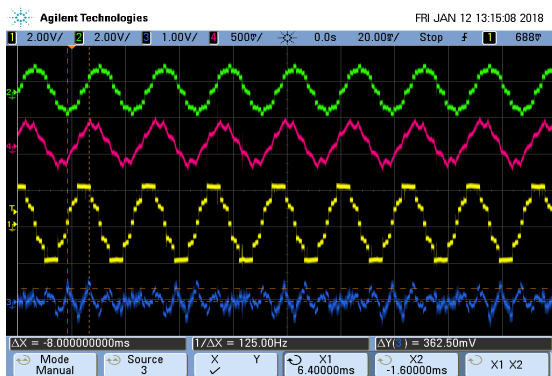


Figure 10. Exptl. 40Hz experimental output waveforms of 5-level inverter

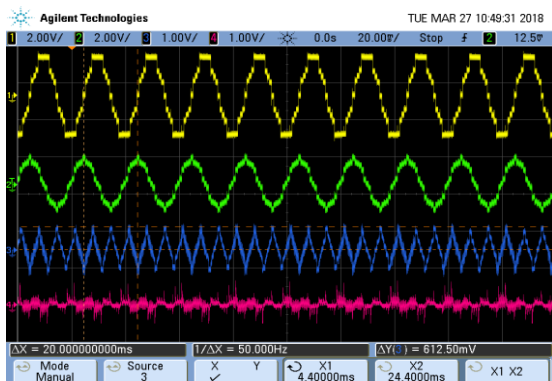
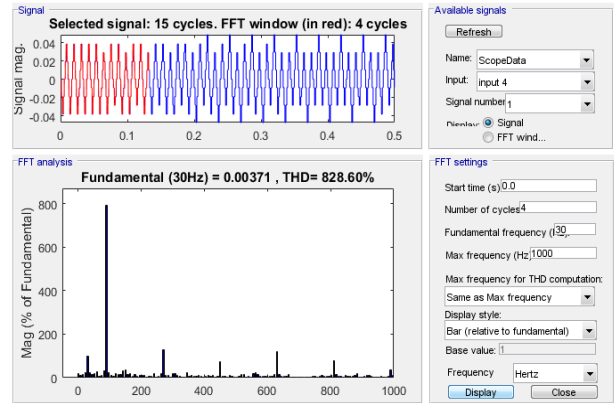


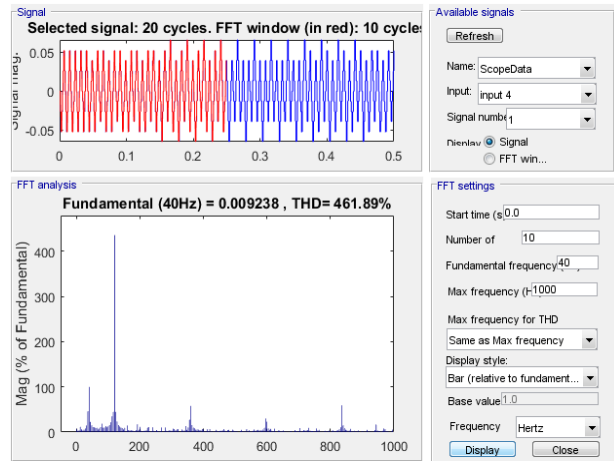
Figure 11. Exptl. 50Hz experimental output waveforms of 5-level inverter

Note: For exptl. Fig. 9-Fig. 11), top to bottom: Ch-1; line voltage [200:1], Ch-2; phase voltage [200:1], Ch-3; common mode voltage [200:1], Ch-4; line current [1:1]

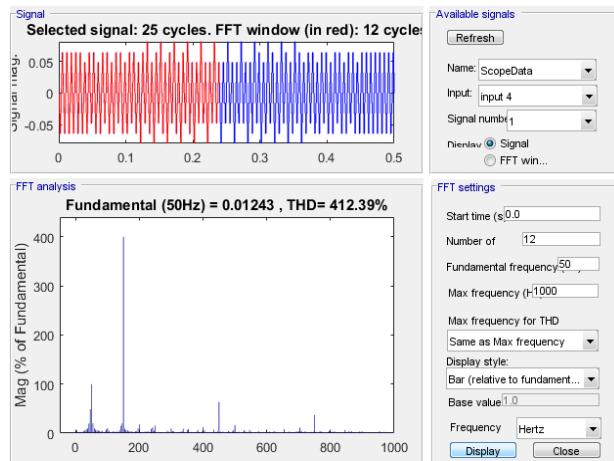
A. FFT Analysis



(a) 30Hz



(b) 40Hz



(c) 50Hz

Figure 12. (a-c) Simulation, FFT analysis of CMV

VI. CONCLUSION

The 5-level Neutral Point Clamped (NPC) inverter is designed, fabricated and tested for the 3-phase IM as load. The phase voltage, line voltage and the CM voltage are measured using Agilent make MSO. By referring the Table II, it is observed that the Experimental CMV

amplitude in 2-level [14], 3-level [15] and 5-level inverter (Fig. 11) is found to be $160V_{\text{Peak}}$, $142.5V_{\text{Peak}}$ and $122.5V_{\text{Peak}}$ respectively for 50Hz of operation.

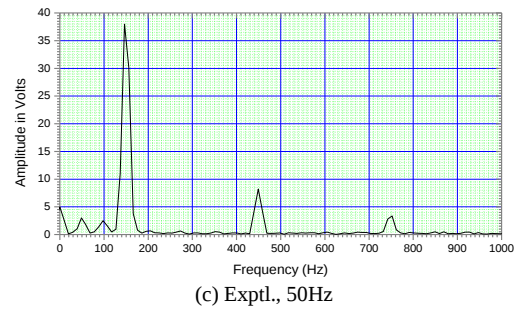
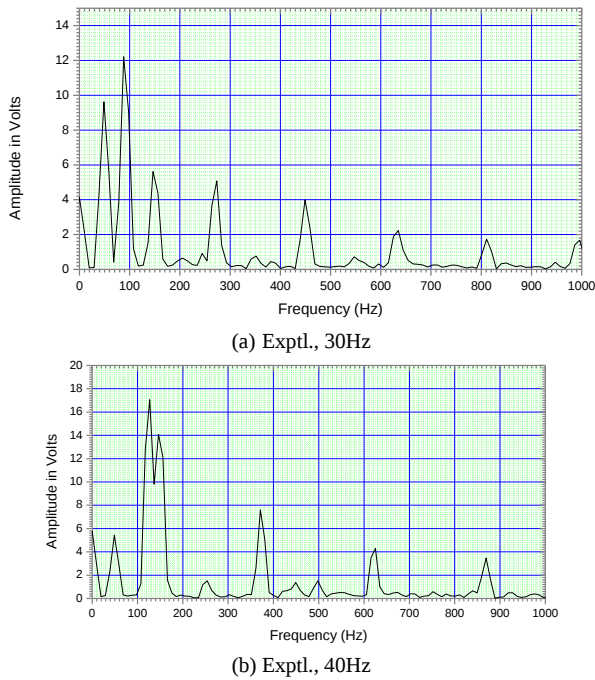


Figure 13. (a-c) FFT analysis of CMV

Similarly, the FFT analysis of CMV in the experiment for 2-level [14], 3-level [15] and the 5-level inverter is found to be around 45V, 25V and 17V respectively for 40Hz of operation as per the Fig. 13b. Comparing the FFT plots of CMV of the 5-level inverter shows less CMV as per the graph in the Fig. 13a-c. Table II gives the comparison of CMV by simulation and Experimentation for 2, 3 and 5-level inverter. It is found that the 5-level inverter CMV is less when compared to 2 and 3-level inverter. Hence it is concluded that as the number of level increases, the CMV is reduced. In addition, as the number of level increases there will be more number of devices in series, hence the voltage stress on the switching devices gets reduced.

TABLE II. COMPARISON OF RESULTS FOR 2, 3 AND 5-LEVEL NPC INVERTER FED INDUCTION MOTOR DRIVE AT DIFFERENT FREQUENCY

parameters	2-level (6 devices)[14]			3-level (9 devices)[15]			5-level inverter (24 devices)		
Frequency	30Hz	40Hz	50Hz	30Hz	40Hz	50Hz	30Hz	40Hz	50Hz
CMV(Simulation)	150V	155V	162V	130V	140V	150V	100V	110V	130V
CMV(Exptl.)	140V	151.5V	160V	120V	132V	142.5V	70V	87.5V	122.5V

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