Reduce Mistrimming of Voltage Offset for Programmable Gain Amplifier (PGA)

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***Abstract*—Commonly the voltage offset of an operational amplifier is only measured and specified in the datasheet but for this device, it is the first device to implement the trimming of the voltage offset that will provide a more accurate output across different gain settings. With the implementation, there were problems encountered particularly the mistrimming of the voltage offset wherein it should be within the datasheet specification and it is in uV range. Even though the Automated Test Equipment (ATE) is capable of measuring uV, there are other contributors that are causing the mistrimming. And in this research, it aims to show the root cause using circuit simulations, develop/implement a proposed solution, and prove that proposed solution will solve the mistrimming issue.**

***Index Terms*—PGA, Vos, mistrimming, ATE**

I. Introduction

As part of the New Product Development, the Test Engineer is tasked to provide a robust test program and hardware (will be referred in this research as test solution) to manufacturing as swiftly as possible to get a market share. To do this, the test solution will be subjected to several verifications and qualifications with one of these qualifications is simulating a manufacturing setup with the use of a handler and a test system that will test several fresh or untested parts under the supervision of the Test Engineer. At this time, the Test Engineer can debug and optimize the test solution in case there will be issues encountered like low yield or unable to test the parts. The simulation of a manufacturing setup is next to the last step of qualification as it will provide information to the Test Engineer of how well the test solution will perform and what issues that will need further improvement. Once the results are satisfactory, the test solution can be endorsed to manufacturing but if not, the issues should be addressed so that it will not delay completion of the development project. The simulation is done by testing fresh parts using PD and QC Test program. The criteria for passing are the yield should be greater than 95% for PD and 100% for QC with using the passing units from PD. And in our case, we yielded 86.7% for PD and 85.2% for QC with the top failure of PGA Vos with a failure rate of 8.57%. In Fig. 1, The plot of the PGA Vos in PD (red) and QC (blue) where PD is centered in the limits (+/-250uV) while QC goes beyond the limits which signify there is a problem with the trimming because the expectation is that it will be the same with PD. The failures exceeding the limits were verified on the bench and found to be valid.

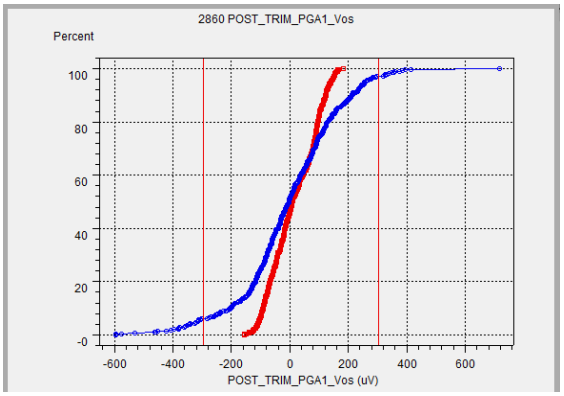

Figure 1. PGA Vos PD and QC plots.

This is a first device that implemented the trimming of the voltage offset of the PGA as most of the available operational amplifier or PGA voltage offset are only measured and checked against the datasheet specifications. Other studies provide solutions for DC offset cancellation rather than reduction or elimination of the mistrimming. The PGA voltage offset is specified in the datasheet to be a maximum of 0.5mV across the temperature range of -40°C to 125°C.

The main purpose of the study is to reduce the failure rate of mistrimming of the voltage offset of the PGA to < 1% and yield to be 85% to 90%, To do this, the following specific objectives must be done: to simulate the current test setup and determine the possible cause of an increase in voltage offset: to formulate a new circuit and program code; to implement the new circuit and program code to the existing test software and hardware; lastly to verify if the mistrimming is reduced.

This research will provide another approach on how to reduce the PGA voltage offset mistrimming. Because a higher voltage offset will need an additional circuit to cancel it out and thus lead to additional cost to the customer. And this defeats the feature of the device which is to be connected directly to an external meter or instrument. And lastly, will prevent the occurrence of customer returns.

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The scope of this study is limited only on the PGA block of the device and the design aspect could not be covered as it will take time to implement and validate.

II. Review of Related Literature

This is the first device to implement the trimming of the PGA Voltage Offset as most of the available op amps and PGAs provides the voltage offset value and are not trimmed. Below are the related literatures.

A. A Low-Power PGA with DC Offset Cancellation in 65nm CMOS Process

A related research by Qianqian Li provided a solution for DC offset cancellation to cancel out the DC offset voltage introduced by the mismatch presented in the circuits [1] but does not provide a solution for the mistrimming.

B. A 60-dB DR PGA with DC Offset Calibration for Short-Distance Wireless Receiver [2]

A related research by Xiaokun Zhao also provided a solution for DC offset cancellation which is the same as the above literature that does not provide a solution for the mistrimming.

C. A dB-linear Switched-Resistor CMOS Programmable Gain Amplifier with DC Offset Cancellation [3]

A related research by Ye Mao provides a DC offset cancellation function block for a 0.18um CMOS process which will not apply to this research as the design is a delimitation.

D. Low-Power CMOS Programmable Gain Amplifier with a DC-Offset Cancellation for a Direct Conversion Receiver

A related research by Cheol-Hwan Kim provides a DC-offset cancellation for a direct conversion (DCR) to reduce chip area, cost, and power [4]. This involves changing the design which is not applicable as the design is a delimitation.

E. Noise Analysis and Optimization of Programmable Gain Amplifier with DC Offset Cancelation

A related research by Li Ma that provides s DC offset cancellation circuit by analyzing the noise and improve the noise performance [5] but does not apply to this research as the objective is reducing mistrimming voltage offset and not improve noise performance.

F. Servo Loop

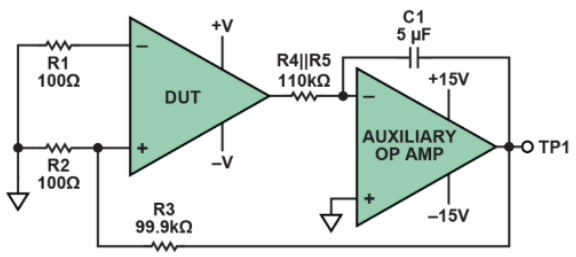

Figure 2. Servo loop circuit.

As shown in Fig. 2, it is a circuit that is used to measure the PGA's voltage offset by forcing 0V or null at the inputs. It employs an auxiliary op amp as an integrator to establish a stable loop with very high dc open-loop gain. [6] This minimized most of the measurement errors and permits accurate measurement of a large number of dc and a few ac parameters.

G. An Accurate dB-Linear Programmable Gain Amplifier with Temperature Robust Characteristic [7]

This research presents a programmable gain amplifier with the aforementioned features but does not provide a solution to the mistrimming.

H. A High-Performance Switch-capacitor Programmable Gain Amplifier Design in 0.18um CMOS Technology [8]

This research presents a programmable gain amplifier with a switch-capacitor to improve accuracy and sampling rate of an image sensor but does not provide a solution to mistrimming.

I. A 64 dB Dynamic Range Programmable Gain Amplifier for Dual Band WLAN 802.11abg IF Receiver in 0.18 µm CMOS Technology [9]

This research presents a programmable gain architecture and discusses internal circuits for offset cancellation which in this research would not be applicable as the design is a delimitation.

J. Programmable Gain Amplifier

Programmable Gain Amplifier (PGA) is an operational amplifier where the gain can be controlled digitally or analog signals. In this research, the gain is digitally programmed using I2C communication.

K. Automated Test Equipment

Automated Test Equipment (ATE) is the generic name for the inspection and test equipment used in electronics manufacture. [10] In the case of this research, the Teradyne MicroFlexHP was used.

L. Synthesis and Justification

The voltage offset for operational amplifiers is a key specification that should be as small as possible so that the output would not accumulate the same voltage offset error. With regards to programmable gain amplifiers, the voltage offset error will be multiplied by the gain where it is programmed and so it is vital to keep the voltage offset trimmed to the smallest value or nearest 0V. In this research, the existing test solution produces mistrimmed parts and would cause customer returns which will lead to loss of revenue.

III. Research Methodology

A. Conceptual FrameWork

From Fig. 3 Conceptual Framework, reviewing the datalogs from the current test setup can provide clues on the possible cause of the mistrimming and whether another test parameter affects the PGA vos. This will be

done by using graphs or plots to get a visual representation of the data. Also, the current test setup and methodology will be verified with the use of a simulation program to speed up the debug as adding wires and taking actual measurements is very tedious and will take time. Once the cause is found, a new test setup will be generated and simulated to verify if it is feasible of reducing the mistrimming. If successful, it will be implemented to the existing Test HW and SW will be revised accordingly.

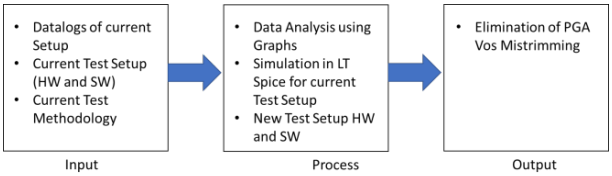

Figure 3. Conceptual framework.

The current setup involves the PGA block with the pins connected DC source, meter, and ground or GND as shown below. The EINx represents the input and correspondingly the EOUTx is the output. The VCOM and RCOM are connected to GND. The yellow-orange broken line box is the DUT (device-under-test) and a broken line from the voltage meter signifies that it can be connected to the input to measure it. The test method is as follows:

1) Set the PGA Gain to 1x.
2) Set the EINx to -50mV and measure the EOUTx.
3) Calculate the Vos as EOUTx + EINx
4) If the Vos > +/- 250uV, adjust the trim code. The target is 0.

The voltage meter used is a high precision voltmeter that has an accuracy of less than 100uV.

Fig. 4 is the PGA Block Test setup that will be simulated in LT Spice Simulator Program..

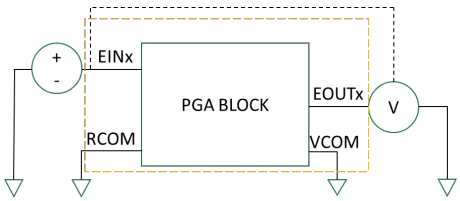

Figure 4. PGA block test setup.

B. Simulation of the Current Test Setup

From Fig. 5, the current Test Setup is simulated using the LT Spice simulator program and then each node (input, output, and ground) will be checked for potential voltage increase that could cause the increase of the Vos. Different conditions will be introduced like adding a resistor or capacitor between the DUT and DC source or meter if it will have any effect and also at the ground pin. The resistor will represent the contact resistance and the capacitance will be the board parasitic capacitance. If there will be any voltage increase, then that is the root cause and will generate or add canceling circuits or components to formulate the new Test setup. Fig. 6 is the screenshot of the LT Spice Simulator Program.

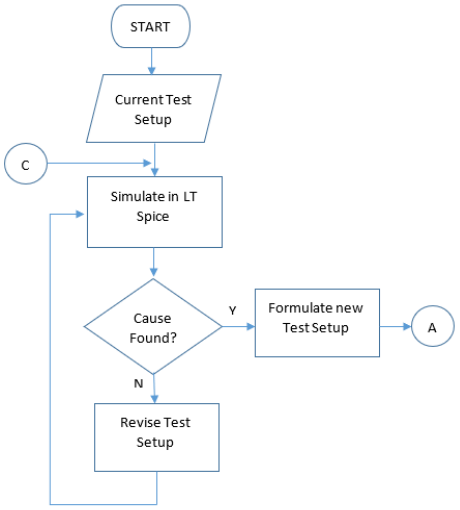

Figure 5. Simulation of current test setup flow chart.

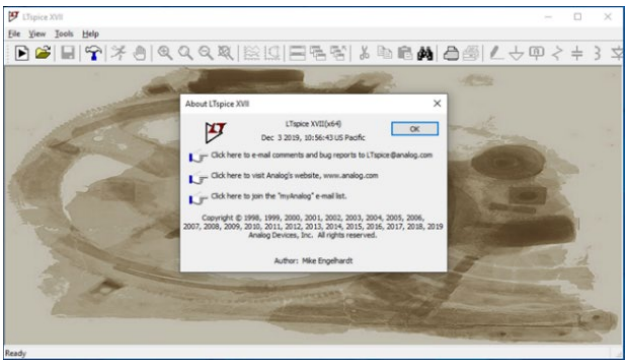

Figure 6. Simulation of current test setup flow chart.

C. Simulate the New Test Setup

From Fig. 7, the formulated or proposed Test setup will also be simulated using LT Spice and similar to the current Test Setup, each node will be measured to check if there will be any increased voltage that will affect the Vos measurement. If there still and increase, the circuit will be revised either adding components to cancel out the increase but if there is no increase, the circuit will be adapted to the existing Test hardware.

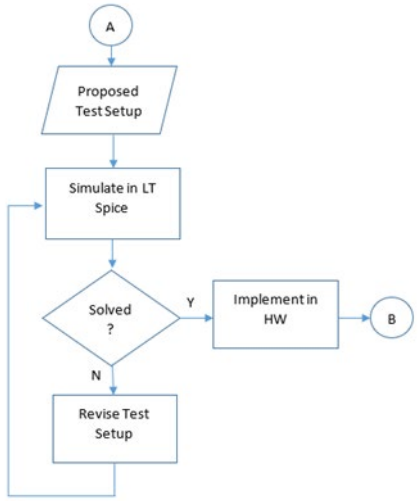

Figure 7. Simulation of new test setup flow chart.

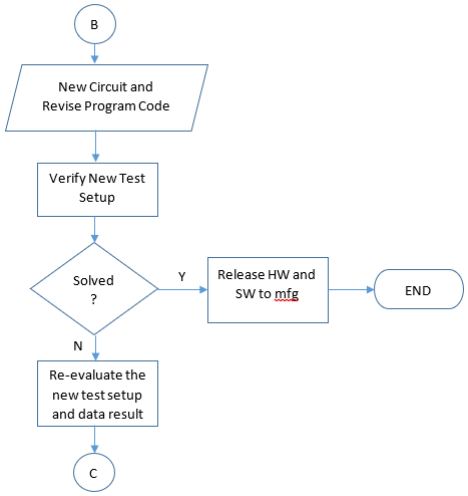

Figure 8. Implementation of the new test setup flow chart.

From Fig. 8, after the implementation of the new Test Setup to the existing Test hardware, it will be verified by running 100 pcs of fresh units on both PD and QC program and if Vos is within the +/- 250 uV and QC is 100% passing, then the test hardware and software can be endorsed to manufacturing but if not, the data and test circuit will have to be re-evaluated and redo the simulation. The Table I will be used to evaluate the PGA Vos of the PD and QC runs by plotting them against each other using Fig. 9 and they should be the same or within the +/-250uV.

TABLE I. NEW CIRCUIT AND PROGRAM CODE PGA VOS

Unit #	PD Vos Value(uV)	QC Vos Value (uV)
1	-47.74501801	-42.71968842
2	-57.18484497	-76.53859711
3	-63.1556015	-54.15014267
4	74.13986206	69.00904083
5	80.6754303	47.60280609
6	-85.47029114	-69.33061218
7	-23.69779396	-9.5105896
8	101.7334061	82.74829865
9	-115.2289505	-145.3701019
10	75.55599213	84.44264221

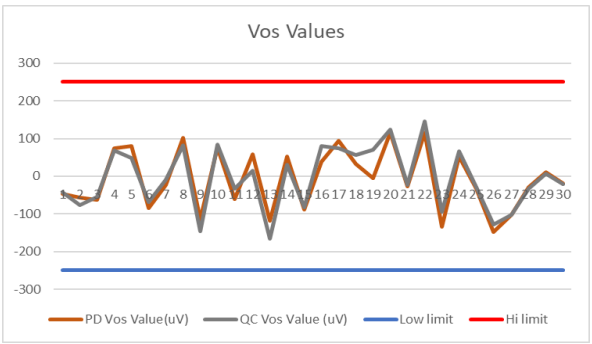

Figure 9. New circuit and program code PGA Vos plot.

The Table I is populated with the PGA Vos measurement of each unit for both PD and QC runs. And Fig. 9 shows the plots of the PD and QC PGA Vos are within the +/- 250uV limit.

Another 100 pcs will be tested using the old circuit and program code of PD and passing units using QC program. Evaluate the PGA Vos of the PD and QC runs by plotting them against each other and the same criteria as above. Since we have the same setup as before we will get a low yield and QC PGA Vos will exceed the +/-250uV specs. The Table I and Fig. 9 will again be used.

Using the mean of the QC run and the new and old setup, it will be evaluated using the t-test statistical hypothesis test where the null hypothesis is, "Both means are the same". Table II is the table to be used.

TABLE II. NEW AND OLD QC RUN

Unit #	New Test Setup (x)	Old Test Setup (y)	x - y	(x-y)^2
1	-42.7197	130.2548	172.9744	29920.1601
2	-76.5386	-119.7060	-43.1674	1863.4228
3	-54.1501	-153.4502	-99.3001	9860.5035
4	69.0090	-100.8293	-169.8383	28845.0568
5	47.6028	-25.6598	-73.2626	5367.4119
6	-69.3306	-116.9722	-47.6416	2269.7200
7	-9.5106	149.5332	159.0438	25294.9183
8	82.7483	68.0538	-14.6945	215.9284
9	-145.3701	293.8925	439.2626	192951.6753
10	84.4426	136.5222	52.0796	2712.2821

Calculate the t-score using (1).

$$t = \frac{(\sum D)/N}{\sqrt{\frac{\sum D^2 - \left(\frac{(\sum D)^2}{N}\right)}{(N-1)(N)}}} \quad (1)$$

Table II is populated with the New Test Setup PGA Vos measurement and the Old Test Setup PGA Vos measurement. This will be used to calculate the t-score as $\sum D = \sum(x - y)$ s and the $\sum D^2 = \sum(x - y)^2$ and $N = 30$.

IV. RESULTS AND DISCUSSION

TINA-TI was used for the simulations as LT Spice does not have a variable resistor to represent the contact resistance. Fig. 10 is the equivalent circuit of the current test setup.

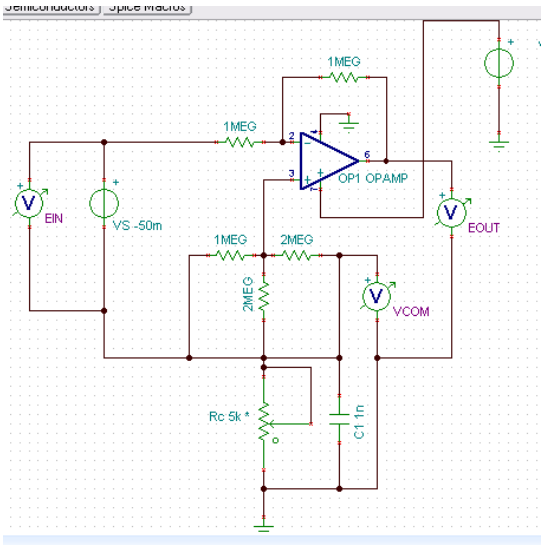

Figure 10. Current test setup circuit equivalent.

From Fig. 10, the circuit enclosed in the red box is the PGA block where the resistor values are not the actual values but in proportions as what the designer specified. The Rc and C1 are the contact resistance and the parasitic capacitance respectively. Just for the sake of simulation, the Rc has a maximum value of 5 Kohm but in the production environment, it will have a value lower than 5 ohms. Fig. 11 is the result of the simulation, where the contact resistance is varied from 0% to 100%

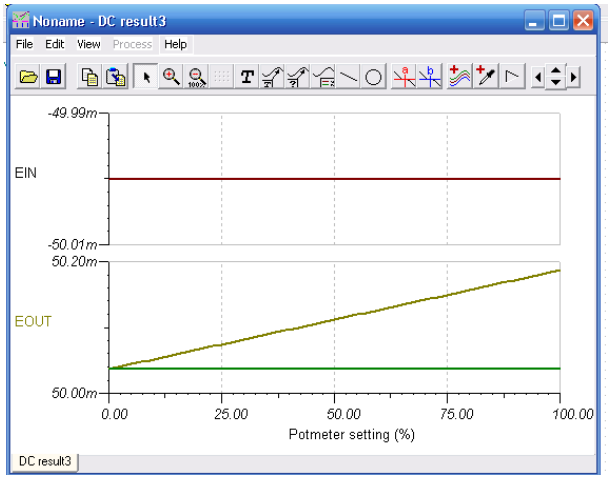

Figure 11. Simulation result of the current test setup.

When the contact resistance is at 0%, the EOUT is 50.04mV and increases as the contact resistance increases (yellow-green line). This means, the contact resistance influences the EOUT measurement and will lead to mistrimming since the vos trimming depends on the EOUT measurement. On the other hand, the parasitic capacitance does not affect since this is a DC test. From Fig. 10, there is a VCOM meter that can be used to measure the contact resistance voltage drop and so the test program was revised to implement VCOM measurement and Fig. 12 is the result.

Fig. 12 shows the PGA Vos (orange plot) is following the trend of the VCOM (blue plot) which validates the simulation that the contact resistance affects the PGA Vos measurement.

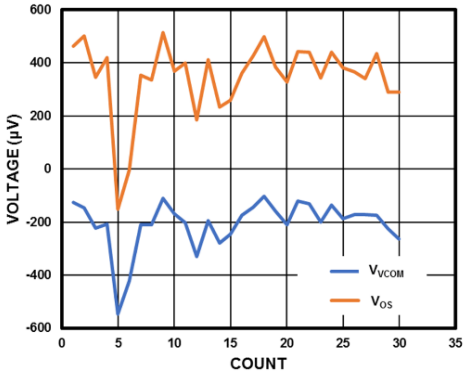

Figure 12. PGA Vos and VCOM plot.

Several trials were done and the Fig. 13 circuit shows that the contact resistance will not have any effect on the EOUT measurement.

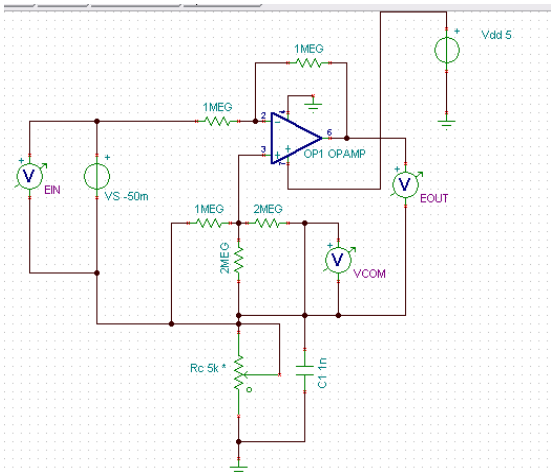

Figure 13. New test setup circuit.

From Fig. 13, the reference connection of the EOUT meter was transferred from GND to the same reference point of EIN. Below is the result of the simulation where the contact resistance is varied from 0% to 100%.

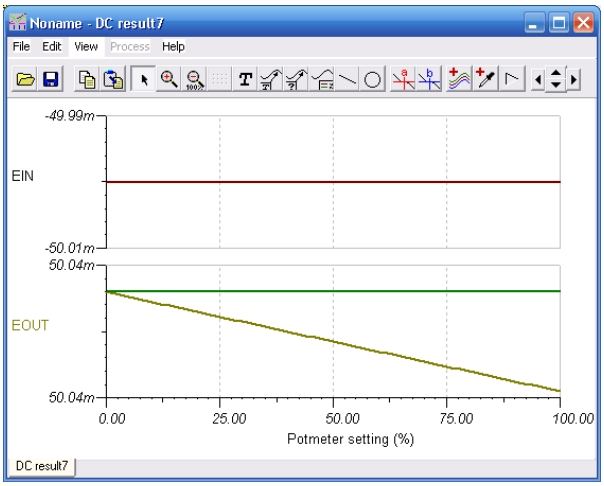

Figure 14. Simulation result of new test setup.

From Fig. 14, EOUT remains at 50.04mV even as Rc was varied from 0% to 100%.

Since there is a need to change the EOUT meter reference, the current HW schematic was checked and unfortunately, there is no way to revise the connection even with rewiring and cutting some traces. The traces are in the layers as the HW is a multilayered PCB.

Looking back at the current test setup, the VCOM value is measured across the contact resistance and this can be used to adjust the EOUT value but since the circuit is not the exact equivalent, the designers provided the formula as shown in (2):

$$EOUT = (EIN \times GAIN) - Vos + 1.5 \times VCOM \text{ or}$$

$$Vos = (EOUT - 1.5 \times VCOM) - (EIN \times GAIN) \quad (2)$$

The Gain is 1 as it is the programmed gain and as stated in the test method. Fig. 15 is the snapshot of the program code where the VCOM is measured and multiplied by 1.5. The trimming routine of the PGA Vos is done after this but cannot be shown as it is a

proprietary test code. Fig. 16 is the sample test program output of the PGA Vos where T#1799 shows the VCOM voltage and T#2860 is the PGA Vos.

```
    .DifferentialVoltMeterLowSide = tlPLMeterVRefVSrc
    .VoltageRange = 5 '0.1 * v
    .Measurement.Filter = tlPLMeterFilter500
    .Measurement.SampleSize = 250
    .Measurement.SampleRate = 100000
  End With
  theHdw.wait 5 * ms
'   TheHdw.PLMeter.Pins("VCOM_PVM").VoltageRange = 50 * mV 'coarse measurement
'   TheHdw.wait 10 * ms
  vcom_meas = theHdw.PLMeter("VCOM_PVM").Measurement.read("vcom_meas", tlStrobe)

    Call TheExec.Flow.TestLimit(vcom_meas, ForceResults:=tlForceFlow)  ' Datalog nominal Vos
vcom_meas = vcom_meas.Math.Multiply(1.5)
```

Figure 15. Test program VCOM measurement.

<Trim_PGA1234_Vos1pt>

1799	1	PGA_VCOM	vcom_pvm	12.c15	-344.1921 uV	-142.5758 uV	0.0000 uV	0.0000 u
1800	1	PGA1_Target	eout1_pvm	12.c15	N/A	50.0853 mV	N/A	0.0000 m
1801	1	PGA2_Target	eout3_pvm	12.a13	N/A	50.1030 mV	N/A	0.0000 m
1802	1	PGA3_Target	eout3_pvm	12.d6	N/A	50.0837 mV	N/A	0.0000 m
1803	1	PGA4_Target	eout4_pvm	12.b4	N/A	50.1124 mV	N/A	0.0000 m
1804	1	PGA1_EIN	eout1_pvm	12.c15	N/A	-50.0853 mV	N/A	0.0000 m
1805	1	PGA2_EIN	eout2_pvm	12.a13	N/A	-50.1030 mV	N/A	0.0000 m
1806	1	PGA3_EIN	eout3_pvm	12.d6	N/A	-50.0837 mV	N/A	0.0000 m
1807	1	PGA4_EIN	eout4_pvm	12.b4	N/A	-50.1124 mV	N/A	0.0000 m
1808	1	PRETRIM_PGA1_EOUT_Nom	eout1_pvm	12.c15	N/A	48.9854 mV	N/A	0.0000 m
1809	1	PRETRIM_PGA2_EOUT_Nom	eout2_pvm	12.a13	N/A	52.2769 mV	N/A	0.0000 m
1810	1	PRETRIM_PGA3_EOUT_Nom	eout3_pvm	12.d6	N/A	50.8402 mV	N/A	0.0000 m
1811	1	PRETRIM_PGA4_EOUT_Nom	eout4_pvm	12.b4	N/A	51.0480 mV	N/A	0.0000 m
2837	1	PGA1_Vos_Index		-1	0.0000 D	68.0000 D	255.0000 D	0.0000
2838	1	PGA1_Vos_BEST_TRIM_Code		-1	0.0000 D	4.0000 D	255.0000 D	0.0000
2839	1	POST_TRIM_PGA1_Vos_Sim		-1	49.5000 mV	50.0662 mV	50.7500 mV	0.0000 m
2841	1	PGA2_Vos_Index		-1	0.0000 D	55.0000 D	255.0000 D	0.0000
2842	1	PGA2_Vos_BEST_TRIM_Code		-1	0.0000 D	72.0000 D	255.0000 D	0.0000
2843	1	POST_TRIM_PGA2_Vos_Sim		-1	49.5000 mV	50.1814 mV	50.7500 mV	0.0000 m
2845	1	PGA3_Vos_Index		-1	0.0000 D	60.0000 D	255.0000 D	0.0000
2846	1	PGA3_Vos_BEST_TRIM_Code		-1	0.0000 D	67.0000 D	255.0000 D	0.0000
2847	1	POST_TRIM_PGA3_Vos_Sim		-1	49.5000 mV	50.0163 mV	50.7500 mV	0.0000 m
2849	1	PGA4_Vos_Index		-1	0.0000 D	59.0000 D	255.0000 D	0.0000
2850	1	PGA4_Vos_BEST_TRIM_Code		-1	0.0000 D	68.0000 D	255.0000 D	0.0000
2851	1	POST_TRIM_PGA4_Vos_Sim		-1	49.5000 mV	50.0102 mV	50.7500 mV	0.0000 m
2852	1	POST_TRIM_PGA1_EOUT_Trim	eout1_pvm	12.c15	49.5400 mV	50.0521 mV	50.7500 mV	0.0000 m
2853	1	POST_TRIM_PGA2_EOUT_Trim	eout2_pvm	12.a13	49.5400 mV	50.1728 mV	50.7500 mV	0.0000 m
2854	1	POST_TRIM_PGA3_EOUT_Trim	eout3_pvm	12.d6	49.5400 mV	50.0197 mV	50.7500 mV	0.0000 m
2855	1	POST_TRIM_PGA4_EOUT_Trim	eout4_pvm	12.b4	49.5400 mV	50.0133 mV	50.7500 mV	0.0000 m
2856	1	POST_TRIM_PGA1_EIN_Trim	eout1_pvm	12.c15	-50.8000 mV	-50.0998 mV	-49.7000 mV	0.0000 m
2857	1	POST_TRIM_PGA2_EIN_Trim	eout2_pvm	12.a13	-50.8000 mV	-50.1133 mV	-49.7000 mV	0.0000 m
2858	1	POST_TRIM_PGA3_EIN_Trim	eout3_pvm	12.d6	-50.8000 mV	-50.0892 mV	-49.7000 mV	0.0000 m
2859	1	POST_TRIM_PGA4_EIN_Trim	eout4_pvm	12.b4	-50.8000 mV	-50.1168 mV	-49.7000 mV	0.0000 m
2860	1	POST_TRIM_PGA1_Vos	eout1_pvm	12.c15	-250.0000 uV	-47.7450 uV	250.0000 uV	0.0000 u
2861	1	POST_TRIM_PGA2_Vos	eout2_pvm	12.a13	-250.0000 uV	59.4807 uV	250.0000 uV	0.0000 u
2862	1	POST_TRIM_PGA3_Vos	eout3_pvm	12.d6	-250.0000 uV	-69.5406 uV	250.0000 uV	0.0000 u
2863	1	POST_TRIM_PGA4_Vos	eout4_pvm	12.b4	-250.0000 uV	-103.4525 uV	250.0000 uV	0.0000 u

Figure 16. Sample test program output of the PGA Vos trimming.

Validating the above formula was done by testing 30 pcs on PD and QC and Fig. 17 is the result.

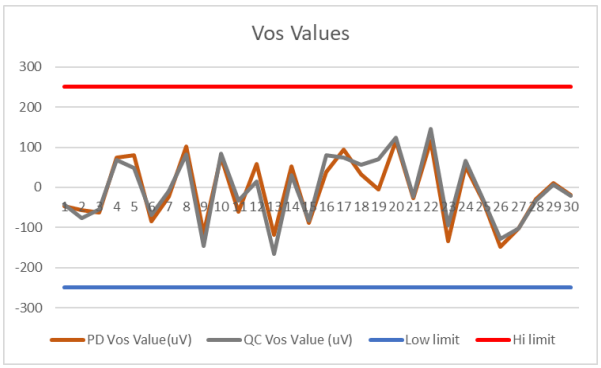

Figure 17. New test setup PGA Vos result.

From Fig. 17, the PD Vos value average is -8.369uV and the QC Vos value average is -5.2557uV. The data also does not go beyond the lo and hi-limit of +/- 250uV and Table I will show the raw data of the graph.

Using the Table II data and (1), the old and new Test setup is evaluated using the t-test statistical hypothesis test where the null hypothesis is, “Both means are the same.” Equation (3) is the calculation of the t-score using the formula and the result is 4.025 which is greater than the t-value of 2.045 with an alpha of 0.05 and df of 29. Therefore, we reject the null hypothesis that both means are the same.

$$t = \frac{3308.4025/30}{\sqrt{\frac{1017639.8666 - \frac{(3308.4025)^2}{30}}{(30-1)(30)}}} \quad (3)$$

V. Results and Discussion

Simulating the current test setup was able to show that the contact resistance, measured by VCOM, causes the voltage offset and therefore is causing the mistrimming. The contact resistance has a direct effect on the EOUT because as the contact resistance was increased the EOUT also increased. On the other hand, the parasitic capacitance, C1 does not have any effect as the test is DC.

Knowing that the contact resistance is the cause, the current test setup was modified to come up with a new test setup circuit to reduce the effect of the contact resistance. Based on the simulation, the EOUT remains at 50.04mV even at 100% value of the contact resistance. Unfortunately, the current HW cannot be revised as there are traces inside the layer and so from Fig. 11, the VCOM value can be used as it measures the voltage drop at the contact resistance. With the help of the designers, Fig. 16 was used and translated to program code.

Validation was done by using the t-test statistical hypothesis test on the data gathered from the 30 pcs tested using the current test setup and the new test setup. The t-score result is 4.025 which is above the t-value and therefore the null hypothesis is rejected such that "Both means are not the same".

To prove that using the new calculation for the PGA Vos will reduce the mistrimming, the data in Table II will be used to calculate the Cpk or process capability index which is in manufacturing terms, is a way to measure or estimate the future process performance. The Cpk is calculated as follows:

$$Cpk = min[\frac{USL-\mu}{3\sigma}, \frac{\mu-LSL}{3\sigma}] \quad (4)$$

The USL and LSL are 250 and -250 respectively which are the specification limits. The μ is the mean of the data and the σ is the standard deviation. Equation (5) shows the new test setup Cpk calculation.

$$Cpk = min[\frac{250-(-5.25)}{3(81.55)}, \frac{(-5.25)-(-250)}{3(81.55)}] \quad (5)$$

$$Cpk = min[1.0433, 1.003]$$

$$Cpk = 1.003$$

TABLE III. Cpk Table

C_{pk}	Process Yield
0.5	86.8%
0.8	98.4%
1.0	99.7%
1.2	99.97%
1.33	99.99%

Referring to the Table III, a Cpk of 1.003 will result to a yield of 99.7% and this would equate to a 0.3% failure rate, therefore, PGA Vos will be < 1%. Equation (5) shows the old test setup Cpk calculation.

$$Cpk = min[\frac{USL-\mu}{3\delta}, \frac{\mu-LSL}{3\delta}] \quad (6)$$

$$Cpk = \min[\frac{250 - (105.02)}{3(119.84)}, \frac{(105.02) - (-250)}{3(119.84)}]$$

$$Cpk = \min[0.4032, 0.9875]$$

$$Cpk = 0.4032$$

Referring to Table III, the New Test Setup Cpk is 1.003 will result to a yield of 99.7% and this would equate to a 0.3% failure rate therefore PGA Vos will be < 1% while the Old Test Setup Cpk is 0.4032 will result to a below 86.8% and would equate to 13.2% failure rate of the PGA Vos. In addition, the yield of 85 – 90% is achievable as the New Test Setup Cpk shows a 99.7% yield process performance and even with a sample size of 30, the future process performance can be determined using the Cpk analysis.

VI. Conclusion

For future research, the authors would like to recommend to implement the new test circuit in the new hardware build and research the design of the device for the PGA Vos trimming to further reduce the vos to below 0.5mV.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Sherell Dynn conducted the research, analyzed the data and wrote the paper. Glenn advised on the methodology and statistical process/approach to use to arrive to the conclusion. Both the authors have approved the final version.

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