Hot-Swap Circuit Implementation

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***Abstract*—Purpose of this paper is to describe the hardware design implementation of hot-swap controller. The Hot-swap circuit protects load, minimizes inrush current and safely shutdown in the event of a fault. The programmable fault current threshold starts the fault timer while allowing the current to pass to the load uninhibited. The programmable current limit threshold sets the maximum current allowed into the load, for both inrush and severe load faults. Both events use the programmable timer which inhibits all current to the load when it expires. The fault and power good out puts are used for improved system management and sequencing control.**

***Index Terms*—hot-swap controller, inrush current, power good pin, MOSFET.**

I. INTRODUCTION

The Hot-Swap capability is crucial in many modern electronic devices. The Hot-swap refers to the action of replacing a system component while the system continues to run, whilst maintaining normal operation. It is a complex operation due to the high level of variability introduced by human and mechanical factors, which must be considered during the design and test phases. A typical device will output signals to a host system given a combination of valid input signals from that host. During a hot-plug operation the pins in a connector system do not all mate at the same time, microscopic differences in pin lengths and contact bounce will result in some signals connecting before others. This behavior may lead to undesirable system operation and must be properly tested to ensure reliable device operation. Hot-Swappable components of moderate size must employ some means of pre-charge circuitry to limit inrush current on connection. The un-charged capacitance of a 'cold' device appears as an electrical short circuit to a host system on first contact, this may cause the host system power rails to dip out of regulation or in some cases lead to complete system failure due to over-current shutdown at the power supply.

II. DESIGN OPTIONS

Designers use a number of methods to mitigate the effects of hot-plugging a device.

A. Pre-Charge Circuitry

A long pin and current limiting resistor (Fig. 1) may be used to limit inrush current to a device. The long pin mates first; the current limit must be set so that the host system power rails stay within specification, but the device charges up adequately before the power and signal pins make connection. Care must be taken when choosing a pre-charge resistor value, the following scenarios show some common problems: If the pre-charge resistor value is too small, the device will still draw too much current on insertion, causing the system power rails to drop out of regulation. If the pre-charge resistor value is too large, the device capacitance is still not adequately charged before the power pins mate, causing the system power rails to drop out of regulation.

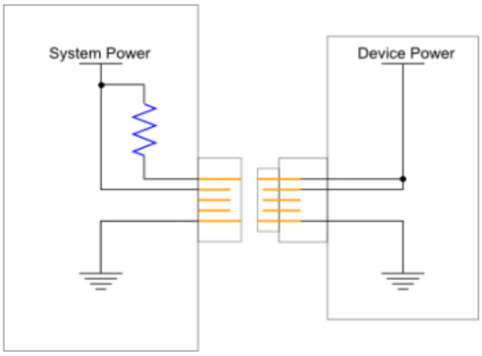

Figure 1. Circuit with limiting resistor

B. Hot-Swap Controller

A hot swap controller IC (Fig. 2) controls inrush current [1] to a device. Hot swap controllers typically incorporate electronic fusing, and in high current applications it may be difficult to distinguish between inrush current and a short circuit. The components are more expensive than pre-charge resistors and in some cases the use of more active components in the system may introduce reliability concerns.

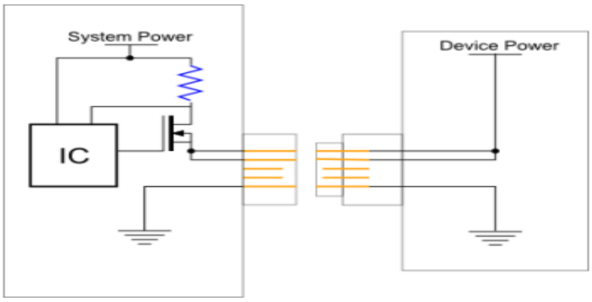

Figure 2. Circuit with hot-swap controller

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III. HOT-SWAP CONTROLLER IC

The TPS2420 [1] provides highly integrated load protection for 3-V to 20-V applications. This device can be programmed to either latch-off orretry [2] in the event of a fault.

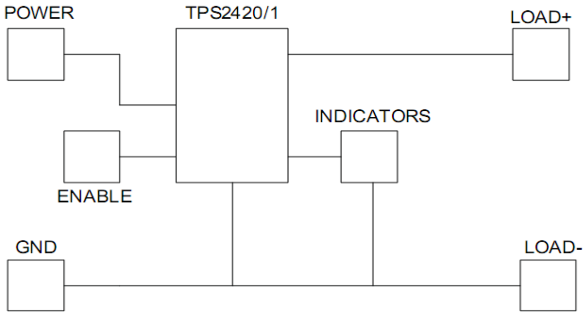

Figure 3. Block diagram hot-swap controller circuit

A. *PIN Description*

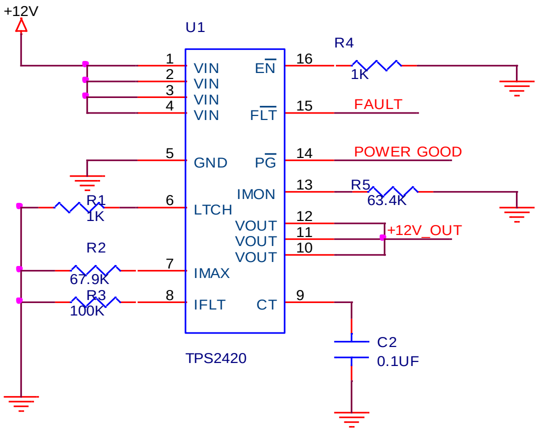

Figure 4. Circuit diagram hot-swap controller circuit

Device (Fig. 4) is enabled when enable pin is pulled low. VIN is power in and control supply voltage. If LTCH is low, the TPS2420 will attempt to restart after an overcurrent fault. If floating (high) the device will latch off after an overcurrent fault and will not attempt to restart until EN or VIN is cycled off and on. IMAX pin with a resistor to ground sets the current limit level. IFLT pin with a resistor to ground sets the fault current level. A capacitor is connected between CT pin and ground to set the fault time. IMON pin indicates scaled down current through the device. VOUT is the Output voltage to the load. Power Good low represents the output voltage is within 300 mV of the input voltage. Fault low indicated the fault time has expired and the internal FET is switched off.

B. *DESIGN Consideration*

Formula [1] used for calculating design parameters and design parameters are summarized in Table I.

$$Rflt = (200Kohm/Ifault)$$

$$Rmax = (\frac{201Kohm}{Imax})$$

$$Cct = (Tfault/38.9x10^3)$$

$$Ifault = \frac{200Kohm}{100Kohm} = 2.0\ Amp$$

$$Imax = \frac{201Kohm}{67.9Kohm} = 2.96\ Amp$$

TABLE I. DESIGN PARAMETERS

IFAULT (A)	RIFLT (KΩ)	IMAX (A)	RMAX (KΩ)	CCT (µF)	TFAULT (ms)	ILOAD (MAX)
2	100	2.96	67.9	0.3	11.67	2

IV. TEST RESULT

To get maximum load, a rheostat was connected externally to the output of hot swap circuit (Table II). From Fig. 5 the load variation matches the device behaviour.

A. *Load Regulation*

TABLE II. VOLTAGES VS LOAD CURRENT

voltages		Load(A)
HOT SWAP input voltage(V)	HOT SWAP output voltage(V)	
13.38	13.31	0.920
13.38	13.31	0.980
13.37	13.29	1.08
13.37	13.27	1.17
13.37	13.27	1.27
13.37	13.25	1.37
13.36	13.24	1.48
13.35	13.23	1.56
13.35	13.21	1.70
13.34	13.20	1.83
13.34	0	1.890
13.34	0	0
13.34	0	0
13.34	13.20	1.85

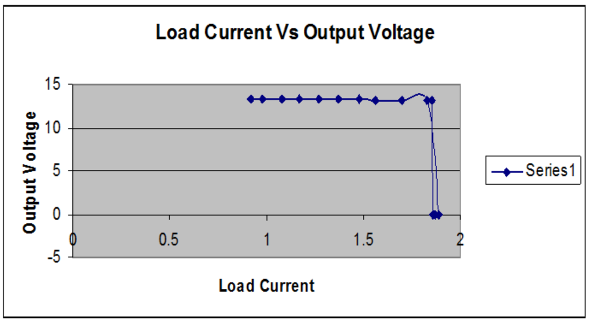

Figure 5. Graph for load current vs voltage

B. *Line Regulation*

Input voltage was varied at Maximum load=1.89A and corresponding output voltage was measured (Table 3).

TABLE III. VOLTAGES VS LOAD CURRENT

i/p voltage(V)	o/p voltage(V)
20.00	19.96
18.07	18.04
16.09	16.05
13.97	13.93
12.16	12.12
10.06	10.01
8.02	7.99
6.05	6.00
4.03	4.01
2.74	0

Fig. 6 represents the line regulation curve as expected from the device [1].

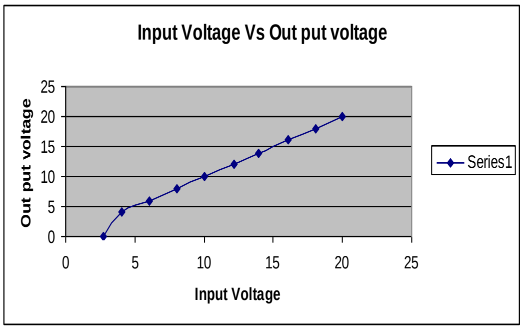

Figure 6. Variation input voltage vs output voltage

C. Voltage Level at Different Pins of TPS2420

TABLE IV. VOLTAGE LEVEL AT DIFFERENT PINS

PIN name & No.	Voltage (hot swap is OFF)	Voltage (hot swap is ON)	When fault occur (Load exceeds 2A)
ENABLE PIN(16)	13.36V	0.002V	0.002V
FAULT PIN(15)	13.36V	13.36V	0.001V
POWER GOOD PIN(14)	13.36V	0.131V	11.31V
LATCH PIN(6)	0.00	0.00	0.00
CT PIN(9)	1.4V	0.20	1.4---0.20

Voltage level at different pins are shown in Table IV. All voltages are within range.

D. Behavior of CT Pin

A capacitor is connected from CT to GND to set the fault time [3]. The fault time starts when the fault current threshold is exceeded, charging the capacitor with 36 μA from GND towards upper threshold of 1.4V. If the capacitor reachesthe upper threshold the internal pass MOSFET is turned off. The MOSFET [1] will stay off until EN# is cycled if latching version is used. If an auto retry version is used the capacitor will discharge at 5 μA to 0.2 V and then re-enable the pass MOSFET. When the device is disabled. CT is pulled to GND through a 100 k ohm resistor. The timer period must be chosen long enough to allow the external load capacitance to charge.

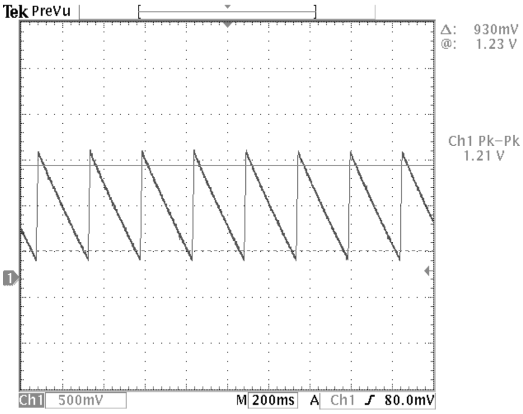

Figure 7. Voltage variation at CT pin

From above figure voltage variation at CT pin is within the range.

E. Behavior of Power Good Pin

Some combination of loading and current limit settings exceeds the 5W power limit of the internal MOSFET [4].The output voltage will not turn on regardless of the fault time setting. One way to work with the physical limits that create this problem is to allow the power manager to charge only the capacitive component of the load and use the POWER GOOD (PG#) signal to turn on the resistive component(Figure 8).This is common usage in DC-DC converters and other electrical equipment with power good inputs. In general POWER GOOD signal is connected to the enable pin of DC-DC converter.

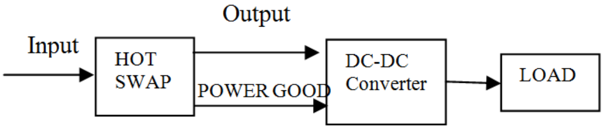

Figure 8. Test circuit for POWER GOOD pin

TABLE V. LOAD VS. OUTPUT VOLTAGE

Load current(A)	Output voltage(v)
0.227	11.97
0.347	11.96
0.545	11.90
0.772	11.89
1.229	11.88
1.562	11.86
2.014	0
Decreasing load	0
1.974	11.85

Here Input voltage is 12V. POWER GOOD pin of TPS2420 is connected to the enable pin of DC-DC converter. The load is first is increased up to maximum and then decreased. The load current and output voltages are tabulated (Table V). The load is first is increased up to maximum and then decreased (Fig. 9).

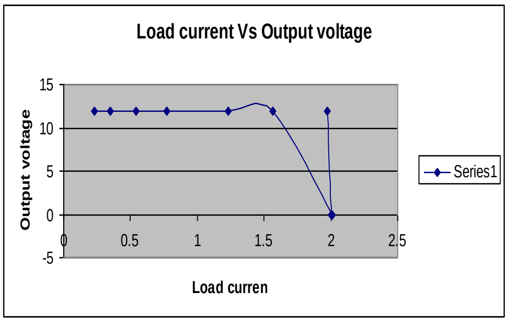

Figure 9. Load vs output voltage

While decreasing the load, it gives output instantly to the required value. So for good design one must use POWER GOOD pin [5].

F. *Inrush Current Measurement*

Experimental set up for measurement of inrush current is shown in the Fig. 10. Voltage across R=0.1 Ω is measured immediately during switch on condition and voltage is captured by scope (Fig. 10).

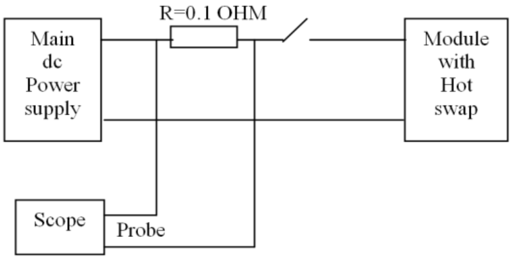

Figure 10. Set up for inrush current measurement

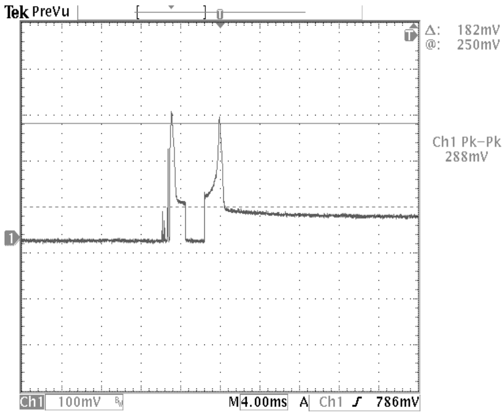

Figure 11. Measurement of inrush current at 0.5Amp load

V. CONCLUSION

From inrush current measurement figures (Fig. 11 and Fig. 12) it is clear that Inrush current decrease with increment of load [6]. It is also clear that there are two peaks- one is for Hot swap controller and another is for main module connected to hot swap controller. The primary reason for inconsistencies between hot-plugs is the human factor, it is practically impossible for a human to insert or remove a device with the same velocity and force in a repeatable manner. Differences in the time between pin's mating has a huge effect on the power up profile of a device, making it impossible to reliably test a hot-pluggable device over all its likely operating conditions. Hot-swap circuit removes all the inconveniences made by mechanical variables and manufacturing tolerances.

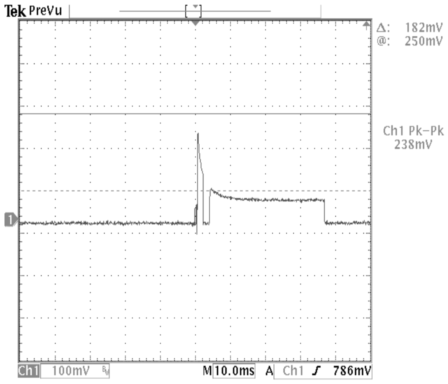

Figure 12. Measurement of inrush current at 2 Amp load

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