

12-Bit Pipeline ADC Implemented in 0.09-um Digital CMOS Technology for Powerline Alliance

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Abstract—This paper presented its own design of 12-bit pipeline ADC which has an operating frequency of 8 MHz and consists of 4 stages only. This design is a pipelined ADC with four 3-bit stages (each stage resolves two bits). By doing so, the chip area can be decreased along with minimized power dissipation. In the study's design, V_{IN} is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to three bits. The 3-bit output is then fed to a 3-bit DAC (accurate to about 12 bits), and the analog output is subtracted from the input. This "residue" is then gained up by a factor of four and fed to the next stage. This gained-up residue continues through the pipeline, providing three bits per stage until it reaches the 4-bit flash ADC, which resolves the last 4LSB bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers.

Index Terms—pipeline ADC, time alignment, shift registers, multiplying DAC, flash ADCs, full adder, half adder, delay

I. INTRODUCTION

Power Line Communication (PLC) represents an exceptionally promising alternative for high-speed internet access and data networking. PLC is one of today's outstanding technology for communication systems that allows data transfer over existing power cables. [1] This means that, with just power cables running to an electronic device (for example), one can power it up and at the same time control and retrieve data from it in a half-duplex manner. Powerline alliance is made possible by high-speed analog-to-digital converters (ADC). ADCs translate analog quantities, which are characteristic of most phenomena in the "real world," to digital language, used in information processing, computing, data transmission, and control systems. [2]

Pipeline analog-to-digital-converters offer a wide range of advantages compared to other topologies, notably optimum balance of size, speed and resolution. A pipelined ADC employs a parallel structure in which each stage works on one to a few bits of successive samples

concurrently. Pipeline ADCs have become increasingly attractive to major data-converter manufacturers and their designers provide an optimum balance of size, speed, resolution, power dissipation, and analog design effort [3].

For this study, the researchers have decided to use pipelined architecture for the ADC to be used. Pipeline ADCs are very similar to flash converters and it consists of several cascaded stages, each with a low resolution ADC. The aim of this study is to implement a 12-bit pipeline ADC with an operating frequency of 8 MHz in 0.09- μ m CMOS technology using Synopsys Galaxy Custom Designer.

Today's rapidly changing trend in CMOS technology demands for greater digital capacity, lower power and basically, smaller area. Thus, this study strives to effectively implement a 12-bit pipeline ADC in 0.09 μ m digital CMOS technology. There are several variations of the designs of pipeline ADCs but the researchers of this study propose to design a 12-bit pipeline ADC with only four stages. This is made possible by having a 3-bit output per stage. By doing so, the area will consequently decrease; thus, power consumption will also be reduced [4].

While the power in analog circuits tends to grow linearly with the desired speed, the link to precision requirements is far more complex. From a general perspective, precision can be subdivided into three main components. The first and most fundamental limit in accuracy is given by the thermal noise of circuit elements. For example, the available signal headroom and the so-called "kT/C noise" [5] determine the dynamic range in an analog sampled data circuit. Reducing the standard deviation of the noise by a factor of two requires quadrupling the effective capacitance in the circuit. At constant speed, this necessitates a fourfold increase in transconductance, and hence a 4x increase in power dissipation [6].

In circuits that are limited by component matching, increasing the precision also translates into a power penalty. To first order, matching accuracy is inversely proportional to component area [7]. Therefore, additional precision requires larger components with larger capacitance and a resulting net increase in power dissipation.

Manuscript received November 14, 2013; revised March 1, 2014.

This work was supported by ERDT (Engineering Research and Development Technology) under Department of Science of Technology.

In addition to the ever-growing demands in conversion bandwidth, low power dissipation and compatibility with deep-submicron technology have emerged as important metrics in state-of-the-art analog-to-digital converter designs. For the most part, this trend is explained by the increasing demand for portability, as well as recent efforts in system-on-chip (SoC) integration. In SoC implementations, data converters are embedded on the same chip with powerful fine-line digital signal processing, resulting in a limited budget for their total heat and power dissipation. [8].

This paper is arranged as follows: Section II describes the pipeline ADC overall system and its operation. In Section III, describes various circuits used in the design. Section IV discusses the prototype chip implementation and shows experimental results. Section V concludes this paper with a summary.

II. OVERALL SYSTEM ARCHITECTURE

A. Pipeline ADC Overall System

Fig. 1 shows the entirety of this study's 12-bit pipeline ADC design. In this schematic, the analog input, V_{IN} , is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to three bits.

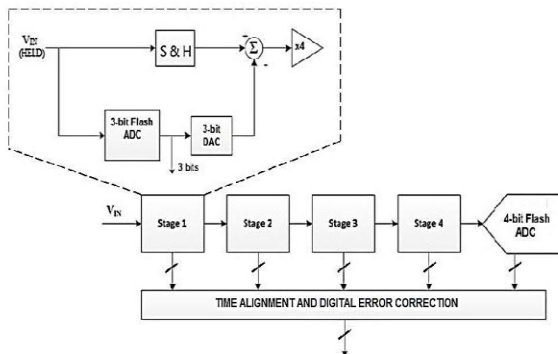


Figure 1. Overall block diagram of a 12-bit pipeline

The 3-bit output is then fed to a 3-bit DAC (accurate to about 12 bits), and the analog output is subtracted from the input. This "residue" is then gained up by a factor of four and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing three bits per stage until it reaches the 4-bit flash ADC, which resolves the last 4LSB bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers. [9] It should be noted that when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput. It should be noted that V_{IN} for this study is 3.3V.

B. MATLAB Behavioral Simulation

The simulations made in this study include a considerable amount of complex computation and

message passing between system components, which makes it important to optimize the performance of a single node and the communication across nodes. To address both of these challenges, behavioral simulations are made in another interactive computing environment and the researchers have decided to use MATLAB for this particular study. This has helped the researchers come up with better visualization and analysis of the desired output.

A sample Matlab behavioral simulation block for each stage is presented in Fig. 2.

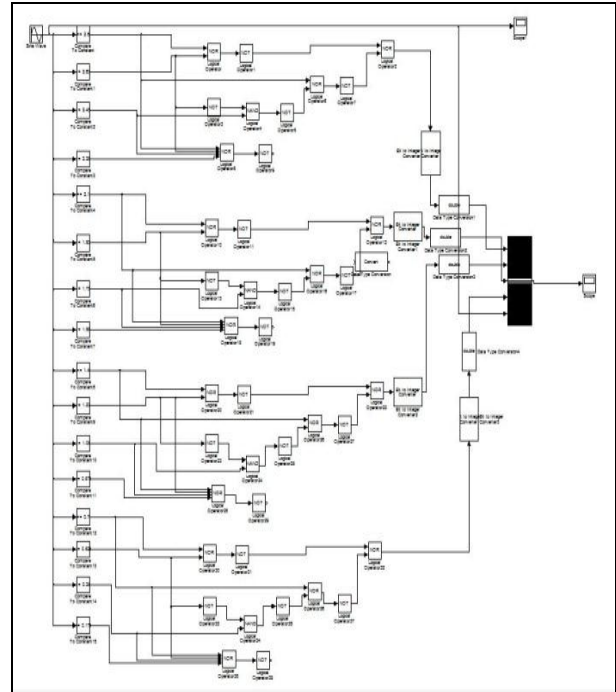


Figure 2. Matlab behavioral simulation of each cascaded stage

III. SYSTEM ARCHITECTURES

A. 3-Bit Flash ADC

Flash ADCs work comparing the input voltage (in this case, the analog input signal) to a reference voltage, which would be the maximum value that can be achieved by the analog signal [10]. The voltage reference is lowered through a resistor network and other comparators added, so the input voltage can be compared to other values. For this study's design, the comparison is done through a hysteresis comparator. The design also features different resistor values in order to obtain non-linear output—this simply means that one value would represent a different voltage step from other values.

This study has designed a 3-bit flash ADC in Fig. 3 which is primarily made up of 7 comparators (2N-1 comparators required) whose output will be the sampled input value and can be read in thermometer-code from the encoder. Before the output from the comparator would reach the encoder, it is highly necessary to insert a voltage level shifter because the comparators operate with 3.3Vdc while the encoder operates with 1.2 Vdc.

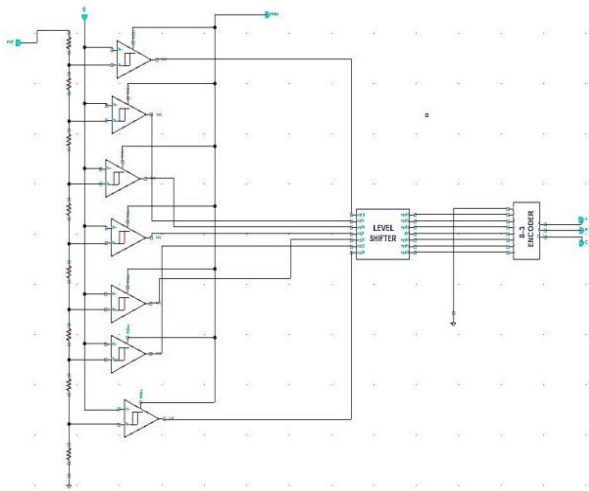


Figure 3. 3-bit flash ADC architecture

B. Hysteresis Comparator

Comparators with hysteresis are advantageous compared with those without hysteresis when used in applications where the inputs of the comparators contain high-frequency disturbances [11].

In Fig. 4, a design of a hysteresis comparator is shown which is composed of a differential amplifier for receiving the input signal, an output inverter circuit for switching the output between high and low voltage levels in response to the signal received at the input of the differential amplifier and an internal current feedback network for introducing a prescribed offset unbalance in the differential amplifier to obtain hysteresis.

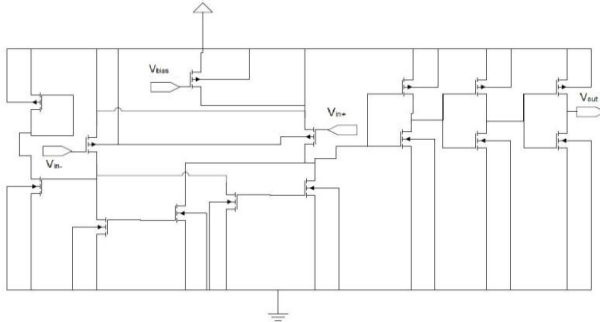


Figure 4. Hysteresis comparator schematic

Also, referring to Fig. 4, it can be seen that the negative input pin of the comparator is connected to V_{IN} while its positive input pin is linked to V_{REF} . The used bias is a resistor network which is precision voltage divider architecture, dividing V_{REF} into equal voltage increments to the positive input pin of the comparator. When V_{IN} exceeds V_{REF} , the output is logic high. If V_{IN} is less than V_{REF} , then the output is 0.

C. Voltage Level Shifter

Due to the fact that the set of comparators and the encoder which consist the entire 3-bit flash ADC system are operating at different voltage levels, a voltage level shifter is needed in order to match each design. It should be noted that the inverter used is analog, which means

that it operates at 3.3 V while the transistors use are at 1.2 V only.

The schematic diagram of the level shifter shown in Fig. 5 consists of an analog inverter which operates at 3.3V, parallel to the operating voltage of the input and the output of the comparator networks. The CMOS gates operate at 1.2 V, equivalent to the voltage level of the time alignment and digital error correction blocks. This design is considered more preferable simply because it consumes lesser number of transistors and therefore saves chip area during fabrication.

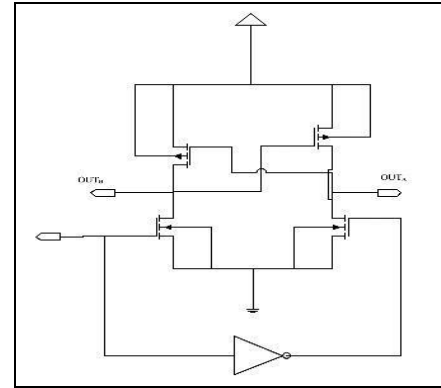


Figure 5. Level shifter

D. 4-Bit Flash Analog-to-Digital Converter (ADC)

Basically, this study's design for a 4-bit flash ADC is very much similar to its 3-bit equivalent. It is still made up of $2N-1$ hysteresis comparators – with $N = 4$, the 4-bit flash ADC consists a total of 15 comparators - a level shifter and an encoder. Two major differences can be distinguished: increased number of comparators and the encoder design used. Fig. 6 depicts the new encoder design.

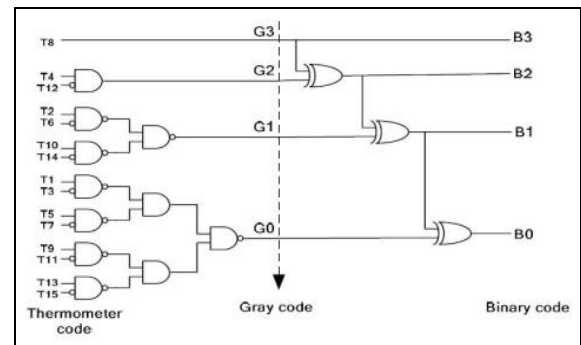


Figure 6. 8-3 binary encoder schematic diagram

Equivalent to logic equations:

$$G_3 = T_8 \quad (1)$$

$$G_2 = T_4 \overline{T_{12}} \quad (2)$$

$$G_1 = T_2 \overline{T_6} + T_{10} \overline{T_{14}} \quad (3)$$

$$G_0 = T_1 \overline{T_3} + T_5 \overline{T_7} + T_9 \overline{T_{11}} + T_{13} \overline{T_{15}} \quad (4)$$

$$B_3 = G_3 \quad (5)$$

$$B_2 = G_2 \oplus B_3 \quad (6)$$

$$B_1 = G_1 \oplus B_2 \quad (7)$$

$$B_0 = G_0 \oplus B_1 \quad (8)$$

E. Multiplying Digital-to-Analog Converter (MDAC)

Ultimately, this block is a simplified and compact version of the four major components in the study's overall block diagram shown in Fig. 7. As can be seen below, MDAC is the equivalent component of all the blocks contained within the perimeter of the in-frame polygon. The primary advantage of using this design is that it can apply a high-resolution digitally set gain to a varying wideband analog signal

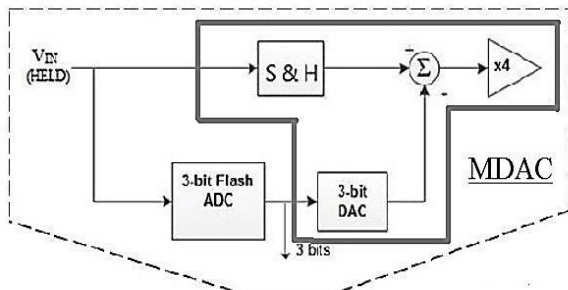


Figure 7. Functional block diagram of MDAC

A multiplying digital-to-analog converter (DAC) differs from the conventional fixed reference DAC by having the ability to operate with an arbitrary or ac reference signal. This application note details the basic theory behind current output multiplying DACs, and why these DACs are so suitable for ac voltage and arbitrary voltage conditioning. [5] And for the design implementation, it composes of a complex network of 70 CMOS gates and an operational amplifier.

Choosing this design over the individual blocks offers an edge when it comes to cost and chip layout. It offers the same functionality and boasts a massive amount of cost and chip layout conservation.

IV. TIME ALIGNMENT AND DIGITAL CALIBRATION

Each of stages shown in the preceding sections of this chapter was sampled in a pipelined manner. The residual analog signal of each stage is then sent to the next stage in the pipeline to be sampled and converted. Finally, all bits, generated at different time, are aligned by the time alignment circuit.

It should be noted that each sampled input has to propagate through the entire pipelined stage before all bits are available and fed to time alignment logic. The schematic diagram of this study's time alignment block is shown in Fig. 8.

The key advantage of the digital calibration is that the errors at the carry transitions are directly measured under the same condition as during the normal conversion. Another important aspect of calibration is that it is performed in the digital domain, so no extra analog circuitry, such as weighted capacitor arrays, is needed and no extra clock cycles are necessary during the conversion. The nominal offsets of the op amp and comparator are reduced by standard offset cancellation and subsequently eliminated by digital calibration.

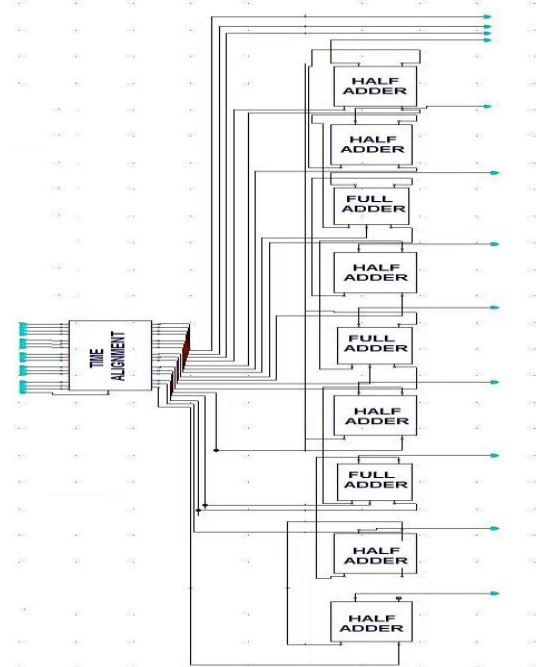


Figure 8. Schematic diagram of the entire time alignment and digital error correction block

A. Time Alignment

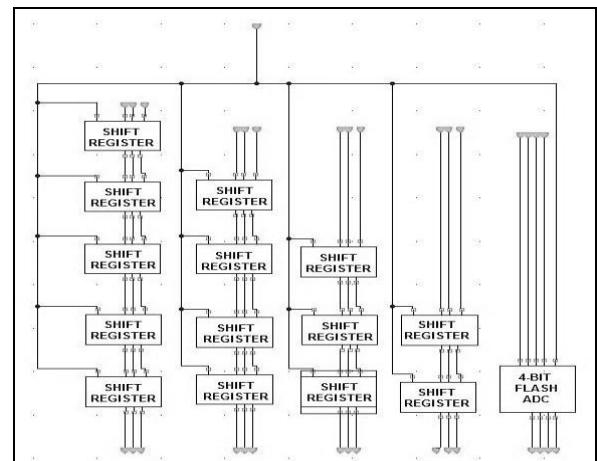


Figure 9. Internal structure of the time alignment block

As represented in Fig. 9, the block for time alignment is made up of shift registers. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events.

Shift registers produce a discrete delay of a digital signal or waveform. A waveform synchronized to a clock, a repeating square wave, is delayed by "n" discrete clock times, and where "n" is the number of shift register stages. Thus, a four stage shift register delays "data in" by four clocks to "data out". There are various types of shift registers but the ones used in this study are serial in/serial out shift register. This structure accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. In Fig.

10, you can see a basic serial in, serial out shift register which is composed of 4 stages.

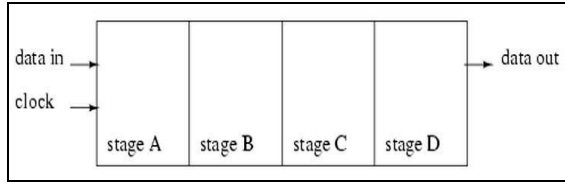


Figure 10. Serial in, serial out shift register with 4 stages

B. Digital Error Correction

The two differential comparators have threshold values from the positive and negative inputs. The result is then decoded by some digital logic which selects one of three values for the differential DAC output. The output is also gated by the sampling clock, such that the DAC output presents a high-impedance until the gain stage is in the hold phase. The data bits MSB and LSB are then fed to set of latches. These latches align all the bits from all the stages in time.

For the digital error correction scheme of this research, the design made use of a specialized combination of adders, both half and full. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit. The Sum out (SOUT) of a full adder is the XOR of input operand bits A, B and the Carry in (CIN) bit.

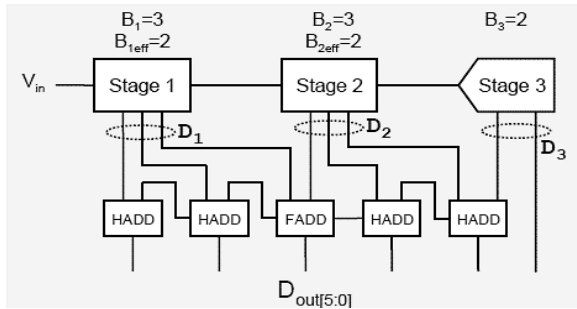


Figure 11. Visual representation of the bit overlap issue

In the time alignment and digital error correction block, bits normally overlap – that is why it is necessary to bring each of the bits into its correct and appropriate position. This is where the need for adders arises. To understand this dilemma better, Fig. 11 depicts a visual representation of the issue.

In mathematical terms, this can be represented in these equations:

$$D_{out} = D_1 + \frac{1}{2^{B1eff}} D_2 + \frac{1}{2^{B1eff} \cdot 2^{B2eff}} D_3 \quad (9)$$

$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3 \quad (10)$$

V. SIMULATION RESULTS

The simulations made in this study include a considerable amount of complex computation and message passing between system components, which

makes it important to optimize the performance of a single node and the communication across nodes.

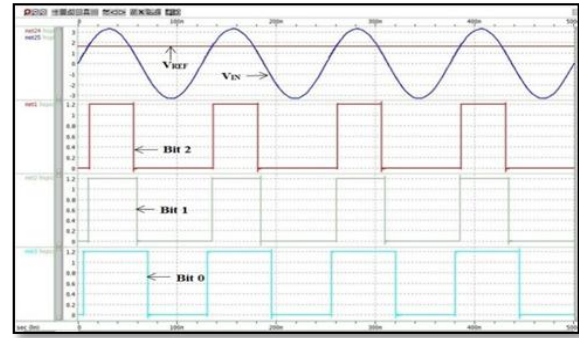


Figure 12. 3-bit flash ADC output in synopsys

From the results shown Fig. 12 the reconstructed ADC blocks, together with whole system output as shown from Pre-simulation (Fig. 13), and Post simulation (Fig. 14), it can be seen that the overall output is logically correct and are the expected output from a pipeline ADC. To check if the bits output are correct is simply measuring the output pulse width. The pulse width should be decreasing starting from the most significant bit.

Each bit's pulse width is very close to each other but using the cursor, the researchers have found out the distinct distance between each succeeding pulse. It can be observed that there is a considerable amount of gap between each pulse. Some may be almost identical to each other, but never the same.

After producing the correct waveform for the schematic design, the researchers immediately started the layout process for the overall architecture. To simplify the whole process, each corresponding component starting from the fundamental logic gates such as inverter, NAND, NOR, and XNOR were designed first. Next, blocks like the encoder, comparator and operational amplifier then followed. When these had been done, the flash ADCs and MDAC layout were also initiated. Finally, the individual blocks were put together to come up with an integrated layout with the subsequent output waveforms.

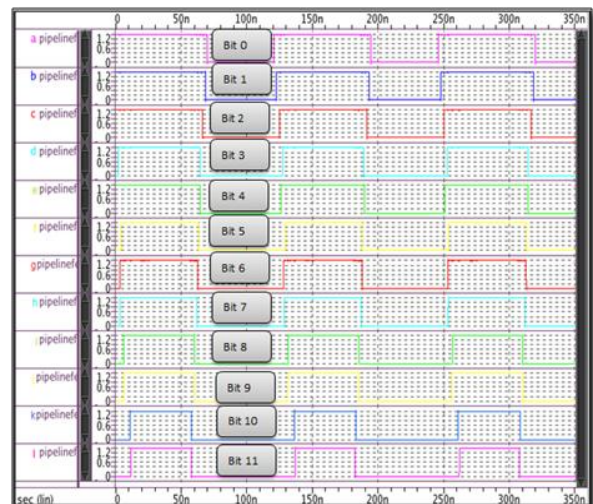


Figure 13. Pre-simulation of 12-bit pipeline ADC output

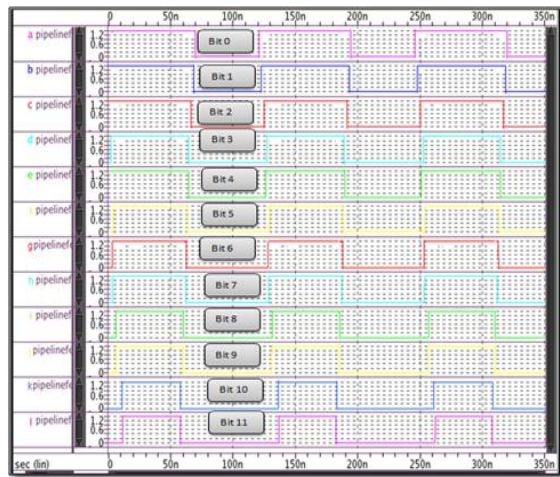


Figure 14. Post simulation output waveforms of 12-bit pipeline ADC

TABLE I. DESIGN SPECIFICATIONS SUMMARY

Parameters	Proposed Limit Values
Architecture	Pipeline
Resolution	12 bits
Technology	0.09 μm CMOS (SAED)
Operating Frequency	8 MHz
Operating Voltages	3.3 V/1.2 V
Total Area	0.2766 mm^2

TABLE II. COMPARISON WITH OTHER PIPELINE ADC

Parameters	Published Journal ^[9]	Published Journal ^[12]	Published Journal ^[6]	Proposed Architecture
Architecture	Pipeline	Pipeline	Pipeline	Pipeline
Resolution	12 bits	12 bits	10 bits	12 bits
Technology	0.18 μm CMOS	Not reflected	0.35 μm CMOS	0.09 μm CMOS
Operating Frequency	5 MHz	5 MHz	6 MHz	8 MHz
Nominal Voltage Supply	1.8 V	2.5 V	2V	1.2 V
Total Area	0.86 mm^2	Not reflected	0.87 mm^2	0.2766 mm^2
Power Consumption	97 mW	47.7 mW	40 mW	32.6 mW

The above results show that the architecture of this study offers many significant advantages like smaller area, lower nominal voltage, and lower power consumption with the same resolution as compared to other published research.

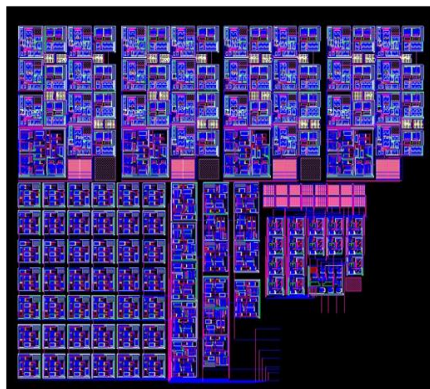


Figure 15. Entire pipeline ADC layout

VI. CONCLUSION

This paper presents a methodical and systematic research study of a 12-bit pipeline ADC implemented in 0.09- μm CMOS technology. The design presented consists of 4 stages with a 3-bit output for every stage. The entire process started with the behavioral simulation in MATLAB followed by design implementation using Synopsys Galaxy Custom Designer. Numerous trial-and-error experiments were done before the desired waveforms had been achieved. The final step was to create the layout and perform post-simulation experiments.

The pre-simulation and post-simulation waveforms were almost identical to each other. Hence, the objective of the study to produce an analog-to-digital converter through pipelining action has been successfully achieved. Analog input signal was effectively converted to a 12-bit digital signal. The design also features reduced chip size due to the cutting down of the number of stages to only 4.

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satellite.

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