Voltage Mode Quadrature Oscillator Employing Single Differential Voltage Current Controlled Conveyor Transconductance Amplifier

S. Maiti and R. R. Pal
Department of Physics and Technophysics, Vidyasagar University, Midnapore 721102, West Bengal, India
Email: saikat_physics@yahoo.com, rrpal@mail.vidyasagar.ac.in

***Abstract*—This paper presents a second order voltage mode quadrature sinusoidal oscillator using a recently reported active building block, namely the differential voltage current controlled conveyor transconductance amplifier. The circuit proposed here employs single differential voltage current controlled conveyor transconductance amplifier, two grounded resistors and two grounded capacitors. The use of grounded capacitors makes the circuit suitable for monolithic circuit implementation. The proposed circuit enjoys the advantage of the independent control of the condition of oscillation and the frequency of oscillation. Also the condition of oscillation and the frequency of oscillation can be tuned electronically by the use of separate bias currents. The non ideal analysis and the sensitivity analysis of the proposed oscillator circuit have been carried out. This shows that the circuit exhibits low active and passive sensitivities. PSpice simulation results have been included which verify the workability of the proposed circuit.**

***Index Terms*—quadrature oscillator (QO), differential voltage current controlled conveyor transconductance amplifier (DVCCCTA), voltage mode, condition of oscillation (CO), frequency of oscillation (FO)**

I. Introduction

The sinusoidal oscillators have become very important building elements for analog systems and are frequently used in electrical and electronics engineering works. Among them the quadrature sinusoidal oscillators have become very important circuit for various communication applications wherein there is a requirement of multiple sinusoids which are 90 ° phase shifted and are frequently used in telecommunications for quadrature mixers, for measurement purposes in vector generators or selective voltmeters and in single sideband modulations [1], [2]. At the present time designing electronic circuits which can operate from low voltages has been gaining increasing interests because the battery operated portable devices require low power dissipation to increase battery life.

Several realizations of sinusoidal oscillators based on various active building blocks (ABBs) like second generation current conveyor (CCII) [3], [4], current feedback amplifier (CFA) [5], current differencing buffered amplifier (CDBA) [6]-[9], differential difference current conveyor (DDCC) [10], [11], differential voltage current conveyor (DVCC) [12]-[14], current differencing transconductance amplifier (CDTA) [15], [16] and recently by the current controlled current conveyor transconductance amplifier (CCCCTA) [17], [18] have received considerable attention. But a careful study of these reported works reveals that several circuits suffer from one or more of the following drawbacks:

(i) The oscillators reported in [3]-[6], [9], [10], [13] use two or more active blocks and at least five passive components.
(ii) The oscillators proposed in [16] do not provide inherent control to the frequency of oscillation and the condition of oscillation.
(iii) The oscillator realizations in [3]-[14] do not provide any electronic control of either the frequency of oscillation or the condition of oscillation.
(iv) Moreover, the oscillator realizations in [11], [12], [14], [15], [17] can not provide quadrature voltage or current outputs directly.
(v) The circuits proposed in [5], [11], [15] employ floating capacitors which are not suitable for monolithic circuit implementation.
(vi) Also in the circuit proposed in [12] one of the DVCC has one of its input Y terminal grounded while in the circuit proposed in [10] one of the DDCC has two of its input Y terminal grounded.

In 2009, a new active element called the differential voltage current conveyor transconductance amplifier (DVCCTA) has been proposed [19]. Several voltage mode and current mode quadrature oscillator using DVCCTA and DVCCCTA have been proposed [20]-[22]. The oscillator proposed in [22] consists of two first order voltage mode all pass filters in cascade. Also the second DVCCTA has one of its input Y terminal (Y_2) grounded.

The motivation of this paper is to present a low voltage second order voltage mode quadrature oscillator using the differential voltage current controlled conveyor transconductance amplifier. The circuit employs single differential voltage current controlled conveyor transconductance amplifier, two grounded capacitors and two grounded resistors. The proposed quadrature oscillator circuit provides the following advantages: First, the condition of oscillation and the frequency of

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oscillation are independently adjustable by the use of separate bias currents. The second reason is that the use of grounded capacitors makes the circuit suitable for monolithic implementation because the grounded capacitors can compensate for the stray capacitances at their nodes [23]. The third reason arises due to the transconductance stage because the transconductance amplifier provides the feature of electronic tuning to the circuit parameters. The circuit also offers low active and passive sensitivities.

II. Differential Voltage Current Controlled Conveyor Transconductance Amplifier

The differential voltage current controlled conveyor transconductance amplifier [21] is an active building block which consists of two principal building blocks, a differential voltage current controlled conveyor at the front end and operational transconductance amplifiers at the rear end. The DVCCCTA has all the advantages of both differential voltage current controlled conveyor and operational transconductance amplifiers. The circuit symbol and the equivalent circuit of the DVCCCTA are shown in Fig. 1 and Fig. 2 respectively, where Y_1 and Y_2 are the input terminals and Z_-, O_{1+} and O_{2+} are the output terminals. The DVCCCTA is characterized by the following equations

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z-} \\ I_{O1+} \\ I_{O2+} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_x & 1 & -1 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & +g_{m1} \\ 0 & 0 & 0 & +g_{m2} \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z-} \end{pmatrix} \quad (1)$$

where R_x represents the finite parasitic resistance at the X input terminal, g_{m1} and g_{m2} represent the transconductance gains of the first and second OTAs.

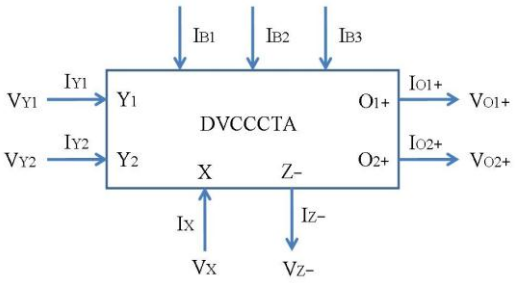

Figure 1. The schematic symbol of the DVCCCTA.

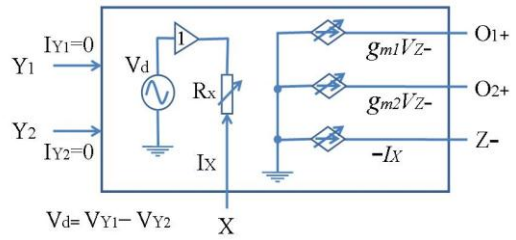

Figure 2. Equivalent circuit of the DVCCCTA.

A possible bipolar implementation of the proposed DVCCCTA is shown in Fig. 3. For this case the values of the parameters can be expressed as

$$R_x = \frac{V_T}{2I_{B1}}, \quad g_{m1} = \frac{I_{B2}}{2V_T}, \quad g_{m2} = \frac{I_{B3}}{2V_T} \quad (2)$$

where I_{B1}, I_{B2} and I_{B3} are the bias currents and V_T is the thermal voltage whose value is 26mV at 27 ℃. For large value of I_{B1} the effect of R_x could be neglected.

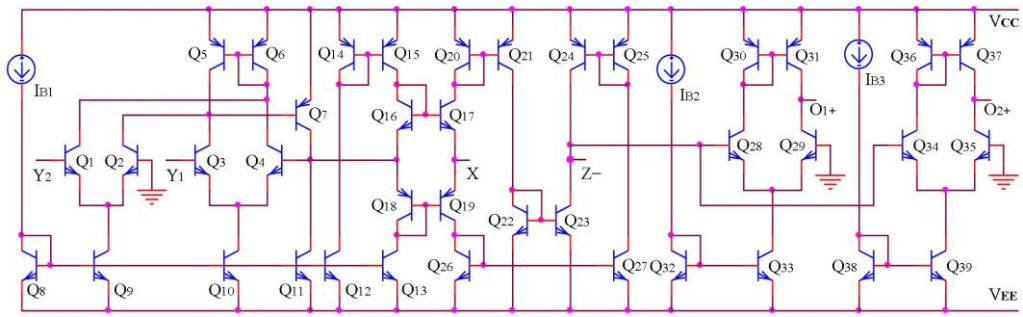

Figure 3. A possible bipolar implementation of the DVCCCTA.

III. Proposed Quadrature Oscillator Circuit

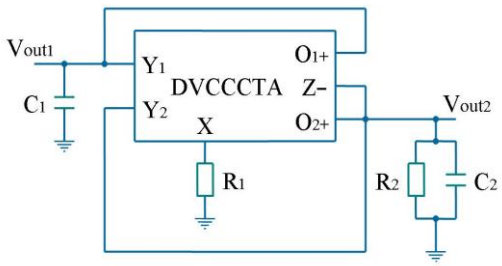

Figure 4. Proposed quadrature oscillator circuit using DVCCCTA.

The proposed quadrature oscillator circuit employing single DVCCCTA is shown in Fig. 4. The circuit employs two grounded capacitors and two grounded resistors. The proposed quadrature oscillator circuit is derived from [20]. Using (1) and doing routine circuit analysis, the characteristic equation can be written as

$$s^2C_1C_2R_1R_2 + sC_1\left(R_1 - R_2 - R_1R_2g_{m2}\right) + g_{m1}R_2 = 0 \quad (3)$$

It is seen from (3) that the condition of oscillation (CO) and the frequency of oscillation (FO) can be expressed as

$$CO: g_{m2} \geq \frac{1}{R_2} - \frac{1}{R_1} \quad (4)$$

$$FO: f_{osc} = \frac{1}{2\pi}\sqrt{\frac{g_{m1}}{C_1 C_2 R_1}} \quad (5)$$

Therefore the condition of oscillation can be adjusted by g_{m2} and the frequency of oscillation can be adjusted by g_{m1} i.e., they are independently adjustable by the separate bias currents I_{B3} and I_{B2}, respectively. The two marked quadrature voltages in Fig. 4 are related as

$$V_{out2} = jkV_{out1} \text{ where } k = \frac{\omega_o C_1}{g_{m1}} \quad (6)$$

It is evident that the quadrature outputs would have equal magnitude for k=1. It is clear from (6) that k depends on the oscillation frequency i.e. on the transconductance gain g_{m1} and therefore it is temperature dependent term. Thus the changing of the oscillation frequency by g_{m1} simultaneously changes the ratio of the magnitudes of quadrature voltages. Also the circuit provides output voltages from high impedance port. Therefore for explicit utilization voltage buffers would be required.

IV. Non Ideal Analysis and Sensitivity Analysis

The non ideal DVCCCTA can be characterized by the following equations [21]

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z-} \\ I_{O1+} \\ I_{O2+} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_x & \alpha_1 & -\alpha_2 & 0 \\ -\beta & 0 & 0 & 0 \\ 0 & 0 & 0 & +\gamma_1 g_{m1} \\ 0 & 0 & 0 & +\gamma_2 g_{m2} \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z-} \end{pmatrix} \quad (7)$$

where α_1 and α_2 represent the voltage transfer gains from Y_1 and Y_2 terminal to the X terminal, β represents the current transfer gain from X to Z_- terminal and γ_1 and γ_2 are the current transfer gains from Z_- terminal to O_{1+} and O_{2+} terminals, respectively. They depend on the frequency of operation, transistor parameters and temperature. In practical, $\alpha_1=1-\varepsilon_1$, $\alpha_2=1-\varepsilon_2$, $\beta=1-\varepsilon_3$, $\gamma_1=1-\varepsilon_4$ and $\gamma_2=1-\varepsilon_5$. The parameters ε_1 and ε_2 ($|\varepsilon_1|$, $|\varepsilon_2| \ll 1$) are the voltage tracking errors of the voltage inverting stages and ε_3, ε_4 and ε_5 ($|\varepsilon_3|$, $\varepsilon_4|$, $|\varepsilon_5| \ll 1$) denote the current tracking errors of the current inverting stages of the DVCCCTA. These gains are ideally equal to unity.

The input parasitic resistance R_x appears in series with the external resistor R_1. Therefore this parasitic resistance increases the external resistor R_1 as $R_1=R_1+R_x$. The parasitic resistances R_{Z-}, R_{O1+}, R_{O2+} and parasitic capacitance C_{Z-}, C_{O1+} and C_{O2+} appear between the high output impedance terminals Z_-, O_{1+}, O_{2+} and ground. Since the values of R_{Z-} and R_{O2+} are in the order of MΩ, therefore an external resistor R_2 should be connected at this terminal so that $R_{Z-}||R_{O2+}||R_2 \approx R_2$. The parasitic capacitances C_{O1+} and $(C_{Z-}+C_{O2+})$ are absorbed into the external capacitors C_1 and C_2, respectively, as they appear in shunt with them. Therefore the original capacitances C_1 and C_2 are increased to C_1 and C_2, where $C_1=C_1+C_{O1+}$ and $C_2=C_2+C_{Z-}+C_{O2+}$.

Taking into account the following non idealities the modified expression of the condition of oscillation (CO) and the frequency of oscillation (FO) can be expressed as

$$CO: g_{m2} \geq \frac{1}{\gamma_2 R_2} - \frac{\alpha_2 \beta}{\gamma_2 (R_1 + R_x)} \quad (8)$$

$$FO: f_{osc} = \frac{\sqrt{\frac{\alpha_1 \beta \gamma_1 g_{m1}}{(C_1 + C_{O1+})(C_2 + C_{Z-} + C_{O2+})(R_1 + R_x)}}}{2\pi} \quad (9)$$

The active and passive sensitivities of the oscillation frequency are given as

$$S_{\alpha_1}^{f_{osc}} = S_{\beta}^{f_{osc}} = S_{\gamma_1}^{f_{osc}} = S_{g_{m1}}^{f_{osc}} = \frac{1}{2} \quad (10)$$

$$S_{C_1}^{f_{osc}} = -\frac{C_1}{2(C_1 + C_{O1+})} \quad (11)$$

$$S_{C_{O1+}}^{f_{osc}} = -\frac{C_{O1+}}{2(C_1 + C_{O1+})} \quad (12)$$

$$S_{C_2}^{f_{osc}} = -\frac{C_2}{2(C_2 + C_{Z-} + C_{O2+})} \quad (13)$$

$$S_{C_{Z-}}^{f_{osc}} = -\frac{C_{Z-}}{2(C_2 + C_{Z-} + C_{O2+})} \quad (14)$$

$$S_{C_{O2+}}^{f_{osc}} = -\frac{C_{O2+}}{2(C_2 + C_{Z-} + C_{O2+})} \quad (15)$$

$$S_{R_1}^{f_{osc}} = -\frac{R_1}{2(R_1 + R_x)} \quad (16)$$

$$S_{R_x}^{f_{osc}} = -\frac{R_x}{2(R_1 + R_x)} \quad (17)$$

Therefore the circuit exhibits low active and passive sensitivities.

V. Simulation Results

To verify the theoretical prediction, the proposed quadrature oscillator circuit has been simulated using PSpice simulation program using the bipolar implementation of the DVCCCTA as shown in Fig. 3. The supply voltages were chosen as $V_{CC}=-V_{EE}=1.5$V. The quadrature oscillator was designed by using the following set of passive elements: $C_1=680$pF, $C_2=680$pF, $R_1=2$kΩ and $R_2=1$kΩ. The bias currents were chosen as $I_{B1}=50$μA ($R_x=260$Ω), $I_{B2}=50$μA ($g_{m1}=0.96$mS) and $I_{B3}=25$μA ($g_{m2}=0.48$mS). With these values, the condition of oscillation is satisfied. The simulated startup of oscillations for both the quadrature voltages V_{out1} and V_{out2} is shown in Fig. 5. The steady state is reached approximately within 300μs. The simulated output waveforms in steady state are shown in Fig. 6. This yields the oscillation frequency of 110kHz. Fig. 7 shows the simulated frequency spectrums of V_{out1} and V_{out2}. The total harmonic distortions (THD) at both the outputs are less than 1%. The total power consumption is approximately 1.46mW.

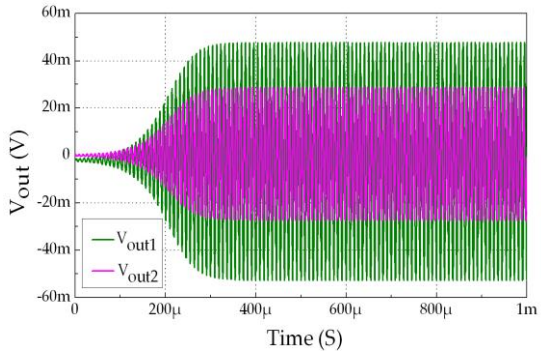

Figure 5. The Simulated output waveforms of the proposed quadrature oscillator at transient stage.

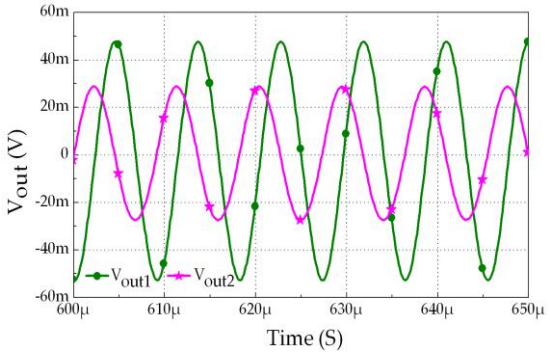

Figure 6. The steady state waveforms of the quadrature voltages.

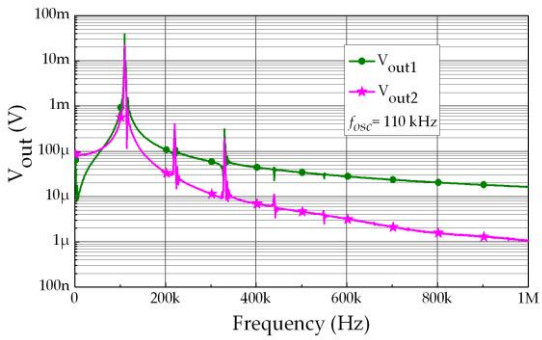

Figure 7. The simulated FFT spectrum of the quadrature voltages.

VI. Conclusion

In this paper, a new quadrature oscillator topology working in the voltage mode has been presented. The proposed circuit employs single differential voltage current controlled conveyor transconductance amplifier, two grounded capacitors and two grounded resistors. The use of grounded capacitors makes the circuit suitable for monolithic implementation. The oscillator circuit proposed in this paper provides non-interactive control of the condition of oscillation and the frequency of oscillation. Also the condition of oscillation and the frequency of oscillation can be tuned electronically by the separate bias currents. The non ideal analysis and the sensitivity analysis of the oscillator circuit have been provided. The magnitudes of the active and passive sensitivities are not more than unity. PSpice simulation results have been included that confirmed the workability of the proposed quadrature oscillator circuit.

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Saikat Maiti was born in 1984 in West Bengal, India. He received his B.Sc. and M.Sc. degrees in Physics from Vidyasagar University, Midnapore, West Bengal, India in 2005 and 2007 respectively. He is currently pursuing the Ph.D. degree at the Department of Physics and Technophysics, Vidyasagar University. His research interests include low voltage and low power analog circuit design, analog signal processing and mixed–mode circuit design.

Radha R. Pal was born in 1967 in West Bengal, India. He passed his B.Sc. and M.Sc. degrees in Physics from Burdwan University, India in the years 1986 and 1988 respectively and topped the list in both the examinations. He got his Ph.D. degree from Indian Institute of Technology, Kharagpur, India in the year 1996. His Ph.D. topic was "Studies on Voltage/Current controlled oscillators using Complementary Bipolar Inverter Cells".

He joined Bengal Engineering College (Deemed University) (now Bengal Engineering and Science University) as a Lecturer in Physics in the year 1995. Presently he is working as a Professor in Physics in the Vidyasagar University, Midnapore, India. His research interest is Low voltage/low power integrated circuit design, VCO and PLL design and simulation. The designs are based on both CMOS and bipolar devices. Some other topics of interest are– MEMS pressure sensor design, design of the interfacing circuits of MEMS based on low voltage/low power topology, generation of shock waves under water, etc.